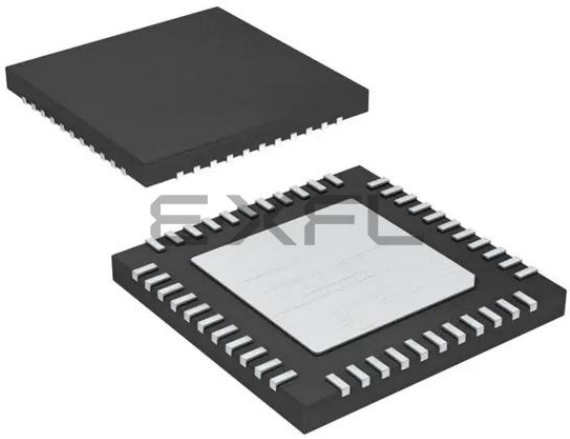

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf45k42-e-ml

TABLE 1-1: DEVICE FEATURES

Features	PIC18(L)F26K42	PIC18(L)F27K42	PIC18(L)F45K42	PIC18(L)F46K42	PIC18(L)F47K42	PIC18(L)F55K42	PIC18(L)F56K42	PIC18(L)F57K42
Program Memory (Bytes)	65536	131072	32768	65536	131072	32768	65536	131072
Program Memory (Instructions)	32768	65536	16384	32768	65536	16384	32768	65536
Data Memory (Bytes)	4096	8192	2048	4096	8192	2048	4096	8192
Data EEPROM Memory (Bytes)	1024	1024	256	1024	1024	256	1024	1024
Packages	28-pin SPDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin SPDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	48-pin TQFP 48-pin UQFN	48-pin TQFP 48-pin UQFN	48-pin TQFP 48-pin UQFN
I/O Ports	A,B,C,E(1)	A,B,C,E(1)	A,B,C,D, E(1)	A,B,C,D, E(1)	A,B,C,D, E(1)	A,B,C,D, E(1), F	A,B,C,D, E(1), F	A,B,C,D, E(1), F
12-Bit Analog-to-Digital Conversion Module (ADC^2) with Computation Accelerator	5 internal 24 external	5 internal 24 external	5 internal 35 external	5 internal 35 external	5 internal 35 external	5 internal 43 external	5 internal 43 external	5 internal 43 external
Capture/Compare/ PWM Modules (CCP)	4							
10-Bit Pulse-Width Modulator (PWM)	4							
Timers (16-/8-bit)	4/3							
Serial Communications	1 UART, 1 UART with DMX/DALI/LIN, 2 I^2C, 1 SPI							
Complementary Waveform Generator (CWG)	3							
Zero-Cross Detect (ZCD)	1							
Data Signal Modulator (DSM)	1							
Signal Measurement Timer (SMT)	1							
5-bit Digital to Analog Converter (DAC)	1							
Numerically Controlled Oscillator (NCO)	1							

3.0 PIC18 CPU

This family of devices contains a PIC18 8-bit CPU core based on the modified Harvard architecture. The PIC18 CPU supports:

- System Arbitration, which decides memory access allocation depending on user priorities
- Vectored Interrupt capability with automatic two level deep context saving
- 31-level deep hardware stack with overflow and underflow reset capabilities
- Support Direct, Indirect, and Relative Addressing modes
- 8x8 Hardware Multiplier

7.2.2.6 Oscillator Status and Manual Enable

The Ready status of each oscillator (including the ADCRC oscillator) is displayed in OSCSTAT (Register 7-4). The oscillators (but not the PLL) may be explicitly enabled through OSCEN (Register 7-7).

7.2.2.7 HFOR and MFOR Bits

The HFOR and MFOR bits indicate that the HFINTOSC and MFINTOSC is ready. These clocks are always valid for use at all times, but only accurate after they are ready.

When a new value is loaded into the OSCFRQ register, the HFOR and MFOR bits will clear, and set again when the oscillator is ready. During pending OSCFRQ changes the MFINTOSC clock will stall at a high or a low state, until the HFINTOSC resumes operation.

7.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source (NOSC) bits of the OSCCON1 register. The following clock sources can be selected using the following:

- External oscillator
- Internal Oscillator Block (INTOSC)

Note:	The Clock Switch Enable bit in Configuration Word 1 can be used to enable or disable the clock switching capability. When cleared, the NOSC and NDIV bits cannot be changed by user software. When set, writing to NOSC and NDIV is allowed and would switch the clock frequency.

7.3.1 NEW OSCILLATOR SOURCE (NOSC) AND NEW DIVIDER SELECTION REQUEST (NDIV) BITS

The New Oscillator Source (NOSC) and New Divider Selection Request (NDIV) bits of the OSCCON1 register select the system clock source and frequency that are used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, so the old source will be ready immediately. The device may enter Sleep while waiting for the switch as described in **Section 7.3.2 "Clock Switch and Sleep"**.

When the new oscillator is ready, the New Oscillator Ready (NOSCR) bit of OSCCON3 and the Clock Switch Interrupt Flag (CSWIF) bit of the respective PIR register are set. If Clock Switch Interrupts are enabled (CSWIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

Note:	The CSWIF interrupt will not wake the system from Sleep.

If the Clock Switch Hold (CSWHOLD) bit of OSCCON3 is clear, the oscillator switch will occur when the New Oscillator is Ready bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

- Set CSWHOLD = 0 so the switch can complete, or
- Copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (i.e., changing FOSC from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock source will already be active, so the switch is relatively quick. CSWHOLD must be clear (CSWHOLD = 0) for the switch to complete.

The current COSC and CDIV are indicated in the OSCCON2 register up to the moment when the switch actually occurs, at which time OSCCON2 is updated and ORDY is set. NOSCR is cleared by hardware to indicate that the switch is complete.

REGISTER 7-6: OSCTUNE: HFINTOSC TUNING REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** HFINTOSC Frequency Tuning bits

01 1111 = Maximum frequency

•

•

•

00 0000 = Center frequency. Oscillator module is running at the calibrated frequency (default value).

•

•

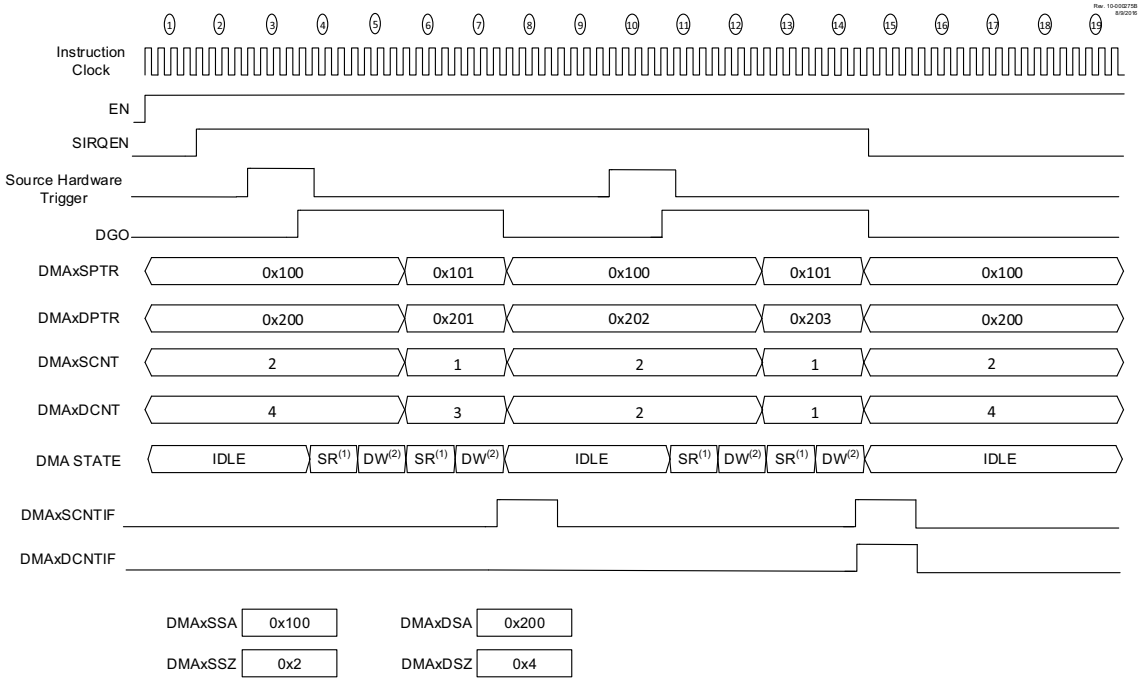
•

10 0000 = Minimum frequency

15.9.2 DESTINATION STOP

When the Destination Stop bit is set (DSTP = 1) and the DMAxDCNT register reloads, the DMA clears the SIRQEN bit to stop receiving new start interrupt request signals and sets the DMAxDCNTIF flag.

FIGURE 15-6: GPR-GPR TRANSACTIONS WITH HARDWARE TRIGGERS, DSTP = 1



Note 1: SR - Source Read

2: DW - Destination Write

REGISTER 17-3: PPSLOCK: PPS LOCK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	PPSLOCKED
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **PPSLOCKED:** PPS Locked bit

1 = PPS is locked.

0 = PPS is not locked. PPS selections can be changed.

TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
PPSLOCK	—	—	—	—	—	—	—	PPSLOCKED	283
INT0PPS	—	—	—	INT0PPS<4:0>					277
INT1PPS	—	—	—	INT1PPS<4:0>					277
INT2PPS	—	—	—	INT2PPS<4:0>					277
T0CKIPPS	—	—	—	T0CKIPPS<4:0>					277
T1CKIPPS	—	—	—	T1CKIPPS<4:0>					277
T1GPPS	—	—	—	T1GPPS<4:0>					277
T3CKIPPS	—	—	—	T3CKIPPS<4:0>					277
T3GPPS	—	—	—	T3GPPS<4:0>					277
T5CKIPPS	—	—	—	T5CKIPPS<4:0>					277
T5GPPS	—	—	—	T5GPPS<4:0>					277
T2INPPS	—	—	—	T2INPPS<4:0>					277
T4INPPS	—	—	—	T4INPPS<4:0>					277
T6INPPS	—	—	—	T6INPPS<4:0>					277
CCP1PPS	—	—	—	CCP1PPS<4:0>					277
CCP2PPS	—	—	—	CCP2PPS<4:0>					277
CCP3PPS	—	—	—	CCP3PPS<4:0>					277
CCP4PPS	—	—	—	CCP4PPS<4:0>					277
SMT1WINPPS	—	—	—	SMT1WINPPS<4:0>					277
SMT1SIGPPS	—	—	—	SMT1SIGPPS<4:0>					277
CWG1PPS	—	—	—	CWG1PPS<4:0>					277
CWG2PPS	—	—	—	CWG2PPS<4:0>					277
CWG3PPS	—	—	—	CWG3PPS<4:0>					277
MD1CARLPPS	—	—	—	MDCARLPPS<4:0>					277
MD1CARHPPS	—	—	—	MDCARHPPS<4:0>					277
MD1SRCPPS	—	—	—	MDSRCPPS<4:0>					277
CLCIN0PPS	—	—	—	CLCIN0PPS<4:0>					277
CLCIN1PPS	—	—	—	CLCIN1PPS<4:0>					277
CLCIN2PPS	—	—	—	CLCIN2PPS<4:0>					277
CLCIN3PPS	—	—	—	CLCIN3PPS<4:0>					277
ADACTPPS	—	—	—	ADACTPPS<4:0>					277
SPI1SCKPPS	—	—	—	SPI1SCKPPS<4:0>					277
SPI1SDIPPS	—	—	—	SPI1SDIPPS<4:0>					277
SPI1SSPPS	—	—	—	SPI1SSPPS<4:0>					277
I2C1SCLPPS	—	—	—	I2C1SCLPPS<4:0>					277
I2C1SDAPPS	—	—	—	I2C1SDAPPS<4:0>					277
I2C2SCLPPS	—	—	—	I2C2SCLPPS<4:0>					277
I2C2SDAPPS	—	—	—	I2C2SDAPPS<4:0>					277
U1RXPPS	—	—	—	U1RXPPS<4:0>					277
U1CTSPPS	—	—	—	U1CTSPPS<4:0>					277
U2RXPPS	—	—	—	U2RXPPS<4:0>					277
U2CTSPPS	—	—	—	U2CTPPS<4:0>					277
RxyPPS	—	—	—	RxyPPS<4:0>					280

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PPS module.

REGISTER 23-3: CCPxCAP: CAPTURE INPUT SELECTION MULTIPLEXER REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/x	R/W-0/x	R/W-0/x
—	—	—	—	—	CTS<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **CTS<2:0>:** Capture Trigger Input Selection bits

CTS<1:0>	**Connection**			
	CCP1	**CCP2**	**CCP3**	**CCP4**
111	CLC4_out			
110	CLC3_out			
101	CLC2_out			
100	CLC1_out			
011	IOC_Interrupt			
010	CMP2_output			
001	CMP1_output			
000	Pin selected by CCP1PPS	Pin selected by CCP2PPS	Pin selected by CCP3PPS	Pin selected by CCP4PPS

REGISTER 23-4: CCPRxL: CCPx REGISTER LOW BYTE

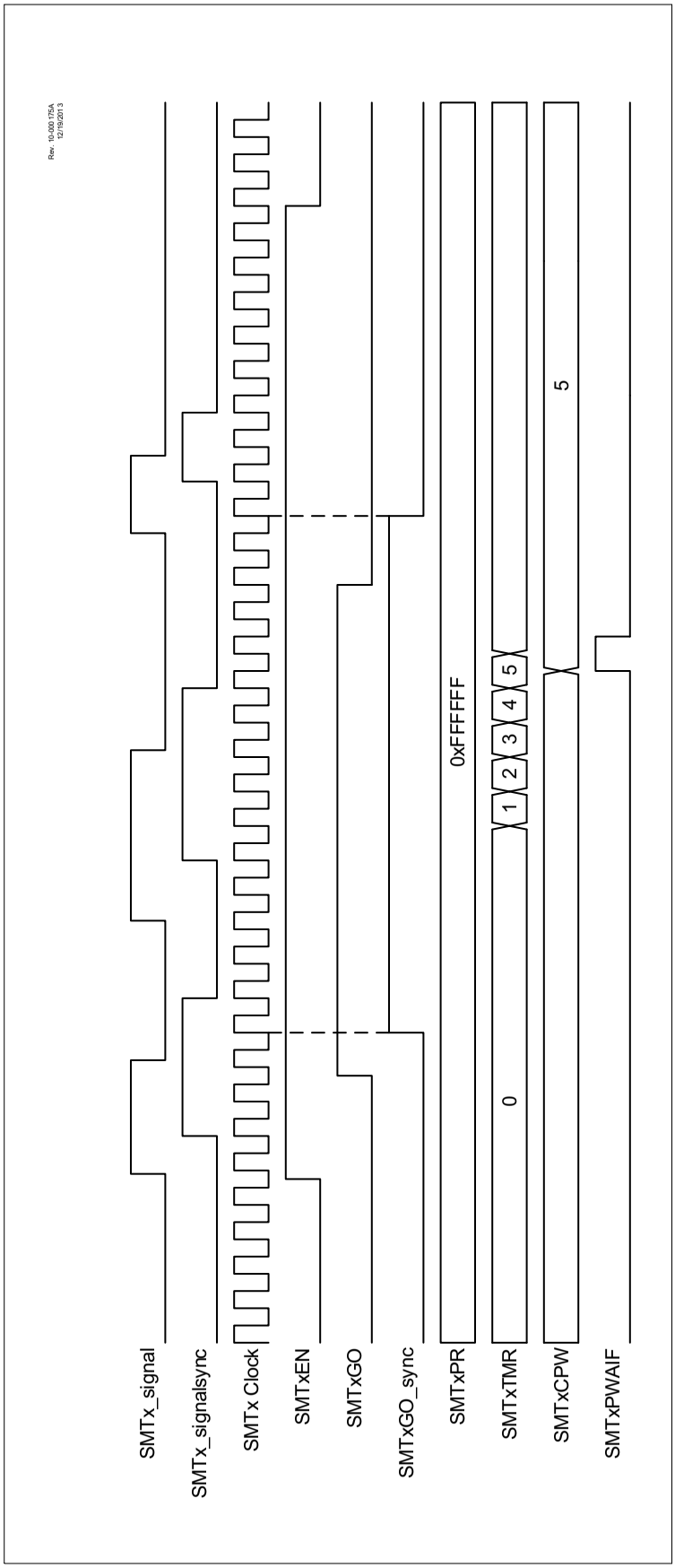
R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
RL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0

MODE = Capture Mode:
RL<7:0>: LSB of captured TMR1 value
MODE = Compare Mode:
RL<7:0>: LSB compared to TMR1 value
MODE = PWM Mode && FMT = 0:
RL<7:0>: CCPW<7:0> – Pulse-Width LS 8 bits
MODE = PWM Mode && FMT = 1:
RL<7:6>: CCPW<1:0> – Pulse-Width LS 2 bits
RL<5:0>: Not used

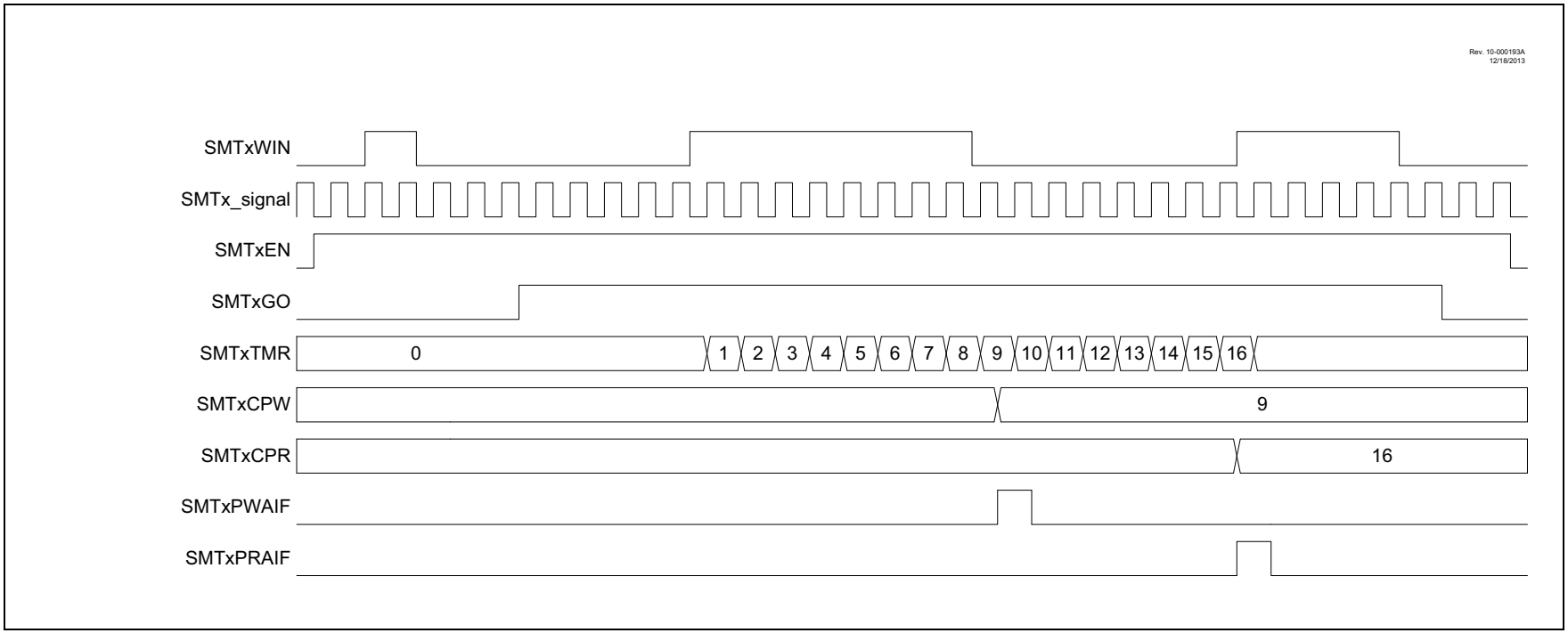
FIGURE 25-5: GATED TIMER MODE SINGLE ACQUISITION TIMING DIAGRAM



25.6.3 PERIOD AND DUTY CYCLE MODE

In Duty Cycle mode, either the duty cycle or period (depending on polarity) of the SMT1_signal can be acquired relative to the SMT clock. The CPW register is updated on a falling edge of the signal, and the CPR register is updated on a rising edge of the signal, along with the SMT1TMR resetting to 0x0001. In addition, the GO bit is reset on a rising edge when the SMT is in Single Acquisition mode. See Figure 25-6 and Figure 25-7.

FIGURE 25-22: WINDOWED COUNTER MODE SINGLE ACQUISITION TIMING DIAGRAM



25.8 Register Definitions: SMT Control

Long bit name prefixes for the Signal Measurement Timer peripherals are shown in **Section 1.3 "Register and Bit naming conventions"**.

TABLE 25-2: LONG BIT NAMES PREFIXES FOR SMT PERIPHERALS

Peripheral	Bit Name Prefix
SMT1	SMT1

REGISTER 25-1: SMT1CON0: SMT CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN(1)	—	STP	WPOL	SPOL	CPOL	PS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** SMT Enable bit(1)
1 = SMT is enabled
0 = SMT is disabled; internal states are reset, clock requests are disabled

bit 6 **Unimplemented**: Read as '0'

bit 5 **STP:** SMT Counter Halt Enable bit
When SMT1TMR = SMT1PR:
1 = Counter remains SMT1PR; period match interrupt occurs when clocked
0 = Counter resets to 24'h000000; period match interrupt occurs when clocked

bit 4 **WPOL:** SMT1WIN Input Polarity Control bit
1 = SMT1WIN signal is active-low/falling edge enabled
0 = SMT1WIN signal is active-high/rising edge enabled

bit 3 **SPOL:** SMT1SIG Input Polarity Control bit
1 = SMT1_signal is active-low/falling edge enabled
0 = SMT1_signal is active-high/rising edge enabled

bit 2 **CPOL:** SMT Clock Input Polarity Control bit
1 = SMT1TMR increments on the falling edge of the selected clock signal
0 = SMT1TMR increments on the rising edge of the selected clock signal

bit 1-0 **PS<1:0>:** SMT Prescale Select bits
11 = Prescaler = 1:8
10 = Prescaler = 1:4
01 = Prescaler = 1:2
00 = Prescaler = 1:1

Note 1: Setting EN to '0' does not affect the register contents.

27.7 Register Definitions: CLC Control

REGISTER 27-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	INTP	INTN	MODE<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **EN:** Configurable Logic Cell Enable bit
1 = Configurable logic cell is enabled and mixing input signals
0 = Configurable logic cell is disabled and has logic zero output

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **OUT:** Configurable Logic Cell Data Output bit
Read-only: logic cell output data, after LCPOL; sampled from CLCxOUT

bit 4 **INTP:** Configurable Logic Cell Positive Edge Going Interrupt Enable bit
1 = CLCxIF will be set when a rising edge occurs on CLCxOUT
0 = CLCxIF will not be set

bit 3 **INTN:** Configurable Logic Cell Negative Edge Going Interrupt Enable bit
1 = CLCxIF will be set when a falling edge occurs on CLCxOUT
0 = CLCxIF will not be set

bit 2-0 **MODE<2:0>:** Configurable Logic Cell Functional Mode bits
111 = Cell is 1-input transparent latch with S and R
110 = Cell is J-K flip-flop with R
101 = Cell is 2-input D flip-flop with R
100 = Cell is 1-input D flip-flop with S and R
011 = Cell is S-R latch
010 = Cell is 4-input AND
001 = Cell is OR-XOR
000 = Cell is AND-OR

28.0 NUMERICALLY CONTROLLED OSCILLATOR (NCO) MODULE

The Numerically Controlled Oscillator (NCO) module is a timer that uses overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the output frequency resolution does not vary with the divider value. The NCO is most useful for applications that require frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCO include:

- 20-bit Increment Function
- Fixed Duty Cycle mode (FDC) mode
- Pulse Frequency (PF) mode
- Output Pulse-Width Control
- Multiple Clock Input Sources
- Output Polarity Control
- Interrupt Capability

Figure 28-1 is a simplified block diagram of the NCO module.

32.3.3 TRANSMIT AND RECEIVE FIFOS

The transmission and reception of data from the SPI module is handled by two FIFOs, one for reception and one for transmission (addressed by the SFRs SPIxRXB and SPIxTXB, respectively.). The TXFIFO is written by software and is read by the SPI module to shift the data onto the SDO pin. The RXFIFO is written by the SPI module as it shifts in the data from the SDI pin and is read by software. Setting the CLRBF bit of SPIxSTATUS resets the occupancy for both FIFOs, emptying both buffers. The FIFOs are also reset by disabling the SPI module.

Note:	TXFIFO occupancy and RXFIFO occupancy simply refer to the number of bytes that are currently being stored in each FIFO. These values are used in this chapter to illustrate the function of these FIFOs and are not directly accessible through software.

The SPIxRXB register addresses the receive FIFO and is read-only. Reading from this register will read from the first FIFO location that was written to by hardware and decrease the RXFIFO occupancy. If the FIFO is empty, reading from this register will instead return a value of zero and set the RXRE (Receive Buffer Read Error) bit of the SPIxSTATUS register. The RXRE bit must then be cleared in software in order to properly reflect the status of the read error. When RXFIFO is full, the RXBF bit of the SPIxSTATUS register will be set. When the device receives data on the SDI pin, the receive FIFO may be written to by hardware and the occupancy increased, depending on the mode and receiver settings, as summarized in Table 32-1.

The SPIxTXB register addresses the transmit FIFO and is write-only. Writing to the register will write to the first empty FIFO location and increase the occupancy. If the FIFO is full, writing to this register will not affect the data and will set the TXWE bit of the SPIxSTATUS register. When the TXFIFO is empty, the TXBE bit of SPIxSTATUS will be set. When a data transfer occurs, data may be read from the first FIFO location written to and the occupancy decreases, depending on mode and transmitter settings, as summarized in Table 32-1 and **Section 32.6.1 "Slave Mode Transmit options"**.

32.3.4 LSB VS. MSB-FIRST OPERATION

Typically, SPI communication is output Most-Significant bit first, but some devices/buses may not conform to this standard. In this case, the LSBF bit may be used to alter the order in which bits are shifted out during the data exchange. In both Master and Slave mode, the LSBF bit of SPIxCON0 controls if data is shifted MSb or LSb first. Clearing the bit (default) configures the data to transfer MSb first, which is traditional SPI operation, while setting the bit configures the data to transfer LSb first.

32.3.5 INPUT AND OUTPUT POLARITY BITS

SPIxCON1 has three bits that control the polarity of the SPI inputs and outputs. The SDIP bit controls the polarity of the SDI input, the SDOP bit controls the polarity of the SDO output, and the SSP bit controls the polarity of both the slave $\overline{SS}$ input and the master SS output. For all three bits, when the bit is clear, the input or output is active-high, and when the bit is set, the input or output is active-low. When the EN bit of SPIxCON0 is cleared, SS(out) and SCK(out) both revert to the inactive state dictated by their polarity bits. The SDO output state when the EN bit of SPIxCON0 is cleared is determined by several factors.

- When the associated TRIS bit for the SDO pin is cleared, and the SPI goes idle after a transmission, the SDO output will remain at the last bit level. The SDO pin will revert to the Idle state if EN is cleared.
- When the associated TRIS bit for the SDO pin is set, behavior varies in Slave and Master mode.
  - In Slave mode, the SDO pin tri-states when:
  - Slave Select is inactive,
  - the EN bit of SPIxCON0 is cleared, or when
  - the TXR bit of SPIxCON2 is cleared.
  - In Master mode, the SDO pin tri-states when TXR = 0. When TXR = 1 and the SPI goes idle after a transmission, the SDO output will remain at the last bit level. The SDO pin will revert to the Idle state if EN is cleared.

38.13 Register Definitions: Comparator Control

Long bit name prefixes for the Comparators are shown in Table 38-2. Refer to **Section 1.3.2.2 "Long Bit Names"** for more information.

TABLE 38-2:

Peripheral	Bit Name Prefix
C1	C1
C2	C2

REGISTER 38-1: CMxCON0: COMPARATOR x CONTROL REGISTER 0

R/W-0/0	R-0/0	U-0	R/W-0/0	U-0	U-1	R/W-0/0	R/W-0/0
EN	OUT	—	POL	—	—	HYS	SYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Comparator Enable bit
- 1 = Comparator is enabled
- 0 = Comparator is disabled and consumes no active power

bit 6 **OUT:** Comparator Output bit

If POL = 0 (noninverted polarity):
- 1 = CxVP > CxVN
- 0 = CxVP < CxVN

If POL = 1 (inverted polarity):
- 1 = CxVP < CxVN
- 0 = CxVP > CxVN

bit 5 **Unimplemented:** Read as '0'

bit 4 **POL:** Comparator Output Polarity Select bit
- 1 = Comparator output is inverted
- 0 = Comparator output is not inverted

bit 3 **Unimplemented:** Read as '0'

bit 2 **Unimplemented:** Read as '1'

bit 1 **HYS:** Comparator Hysteresis Enable bit
- 1 = Comparator hysteresis enabled
- 0 = Comparator hysteresis disabled

bit 0 **SYNC:** Comparator Output Synchronous Mode bit
- 1 = Comparator output to Timer1/3/5 and I/O pin is synchronous to changes on Timer1 clock source.
- 0 = Comparator output to Timer1/3/5 and I/O pin is asynchronous
  Output updated on the falling edge of Timer1/3/5 clock source.

MULLW **Multiply literal with W**

Syntax: MULLW k

Operands: $0 \le k \le 255$

Operation: (W) x k → PRODH:PRODL

Status Affected: None

Encoding:

0000	1101	kkkk	kkkk

Description: An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in the PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged.
None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write registers PRODH: PRODL

Example: `MULLW 0C4h`

Before Instruction
W = E2h
PRODH = ?
PRODL = ?
After Instruction
W = E2h
PRODH = ADh
PRODL = 08h

MULWF **Multiply W with f**

Syntax: MULWF f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (W) x (f) → PRODH:PRODL

Status Affected: None

Encoding:

0000	001a	ffff	ffff

Description: An unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged.
None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 41.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write registers PRODH: PRODL

Example: `MULWF REG, 1`

Before Instruction
W = C4h
REG = B5h
PRODH = ?
PRODL = ?
After Instruction
W = C4h
REG = B5h
PRODH = 8Ah
PRODL = 94h

TABLE 42-1: REGISTER FILE SUMMARY FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

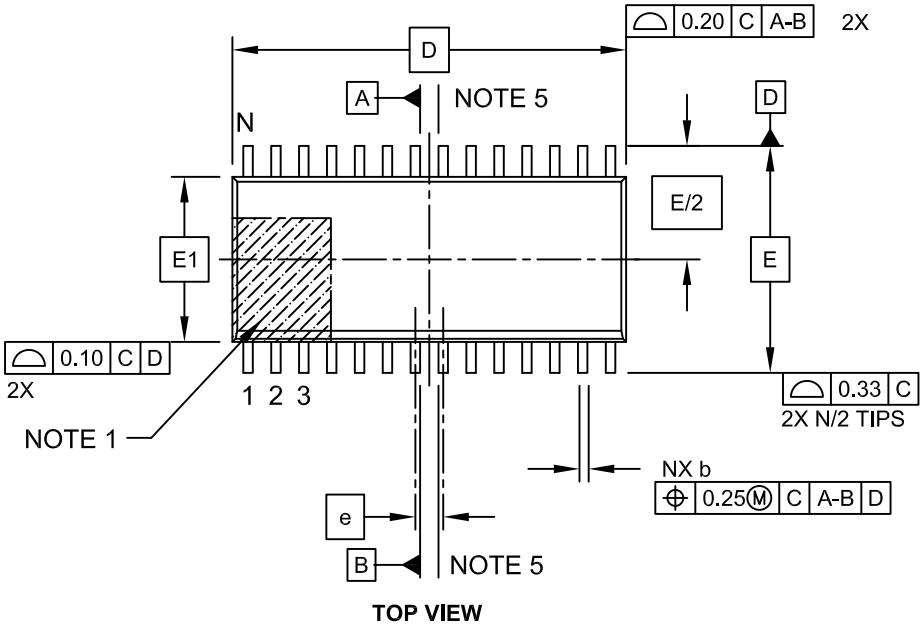
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
3BC8h - 3AEBh	—	Unimplemented								
3AEAh	U2CTSPPS	—	—	—	U2CTSPPS					277
3AE8h	U2RXPPS	—	—	—	U2RXPPS					277
3AE7h	U1CTSPPS	—	—	—	U1CTSPPS					277
3AE5h	U1RXPPS	—	—	—	U1RXPPS					277
3AE4h	I2C2SDAPPS	—	—	—	I2C2SDAPPS					277
3AE3h	I2C2SCLPPS	—	—	—	I2C2SCLPPS					277
3AE2h	I2C1SDAPPS	—	—	—	I2C1SDAPPS					277
3AE1h	I2C1SCLPPS	—	—	—	I2C1SCLPPS					277
3AE0h	SPI1SSPPS	—	—	—	SPI1SSPPS					277
3ADFh	SPI1SDIPPS	—	—	—	SPI1SDIPPS					277
3ADEh	SPI1SCKPPS	—	—	—	SPI1SCKPPS					277
3ADDh	ADACTPPS	—	—	—	ADACTPPS					277
3ADCh	CLCIN3PPS	—	—	—	CLCIN3PPS					277
3ADBh	CLCIN2PPS	—	—	—	CLCIN2PPS					277
3ADAh	CLCIN1PPS	—	—	—	CLCIN1PPS					277
3AD9h	CLCIN0PPS	—	—	—	CLCIN0PPS					277
3AD8h	MD1SRCPPS	—	—	—	MD1SRCPPS					277
3AD7h	MD1CARHPPS	—	—	—	MD1CARHPPS					277
3AD6h	MD1CARLPPS	—	—	—	MD1CARLPPS					277
3AD5h	CWG3INPPS	—	—	—	CWG3INPPS					277
3AD4h	CWG2INPPS	—	—	—	CWG2INPPS					277
3AD3h	CWG1INPPS	—	—	—	CWG1INPPS					277
3AD2h	SMT1SIGPPS	—	—	—	SMT1SIGPPS					277
3AD1h	SMT1WINPPS	—	—	—	SMT1WINPPS					277
3AD0h	CCP4PPS	—	—	—	CCP4PPS					277
3ACFh	CCP3PPS	—	—	—	CCP3PPS					277
3ACEh	CCP2PPS	—	—	—	CCP2PPS					277
3ACDh	CCP1PPS	—	—	—	CCP1PPS					277
3ACCh	T6INPPS	—	—	—	T6INPPS					277
3ACBh	T4INPPS	—	—	—	T4INPPS					277
3ACAh	T2INPPS	—	—	—	T2INPPS					277
3AC9h	T5GPPS	—	—	—	T5GPPS					277
3AC8h	T5CLKIPPS	—	—	—	T5CLKIPPS					277
3AC7h	T3GPPS	—	—	—	T3GPPS					277
3AC6h	T3CLKIPPS	—	—	—	T3CLKIPPS					277
3AC5h	T1GPPS	—	—	—	T1GPPS					277
3AC4h	T1CLKIPPS	—	—	—	T1CLKIPPS					277
3AC3h	T0CLKIPPS	—	—	—	T0CLKIPPS					277
3AC2h	INT2PPS	—	—	—	INT2PPS					277
3AC1h	INT1PPS	—	—	—	INT1PPS					277
3AC0h	INT0PPS	—	—	—	INT0PPS					277
3ABFh	PPSLOCK	—	—	—	—	—	—	—	PPSLOCKED	283
3ABEh	—	Reserved, maintain as '0'								
3ABDh - 3A9Ah	—	Unimplemented								
3A99h	—	Reserved, maintain as '0'								

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

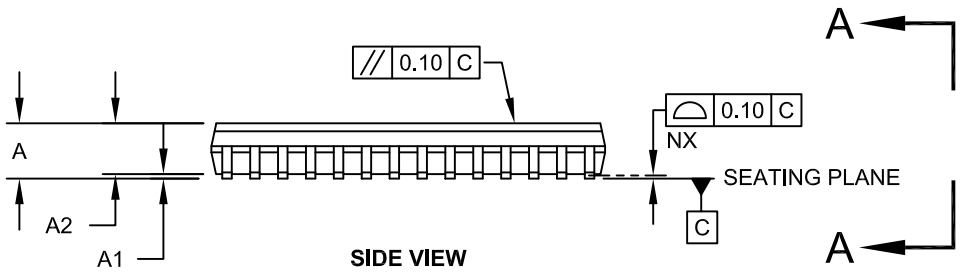
Note 1: Unimplemented in LF devices.
2: Unimplemented in PIC18(L)F26/27K42.
3: Unimplemented on PIC18(L)F26/27/45/46/47K42 devices.
4: Unimplemented in PIC18(L)F45/55K42.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

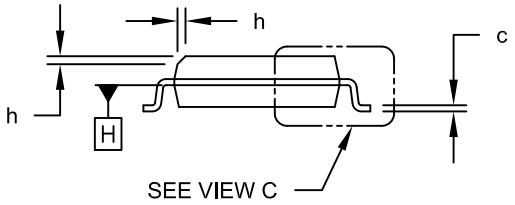
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

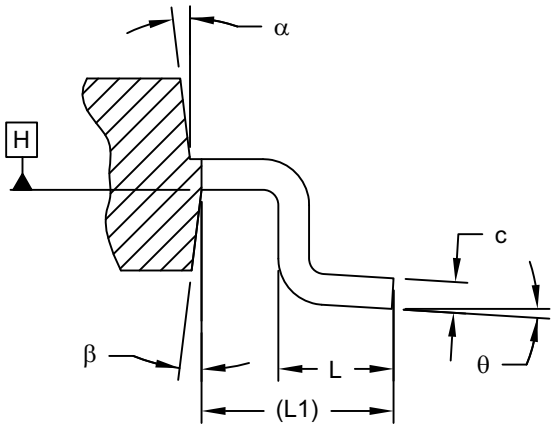


VIEW A-A

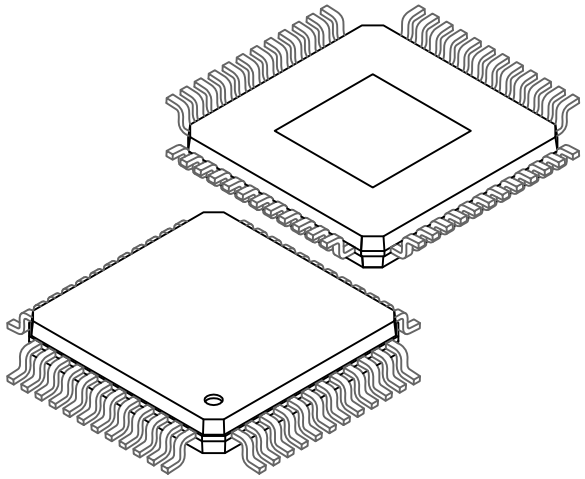
Microchip Technology Drawing C04-052C Sheet 1 of 2

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Exposed Pad Width	E2		3.50 BSC	
Exposed Pad Length	D2		3.50 BSC	
Lead Thickness	c	0.09	-	0.16
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-183A Sheet 2 of 2