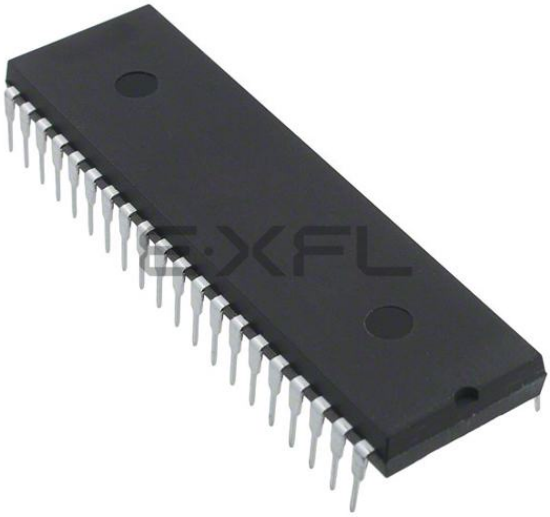

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf45k42-e-p

FIGURE 4-4: DATA MEMORY MAP FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

Bank	BSR<5:0>	Address addr<7:0>	PIC18(L)F45K42 PIC18(L)F55K42	PIC18(L)F26K42 PIC18(L)F46K42 PIC18(L)F56K42	PIC18(L)F27K42 PIC18(L)F47K42 PIC18(L)F57K42	Address addr<13:0>
Bank 0	00 0000	00h	Access RAM	Access RAM	Access RAM	0000h 005Fh
		FFh	GPR	GPR	GPR	0060h 00FFh
Bank 1	00 0001	00h FFh	GPR	GPR	GPR	0100h 03FFh
Bank 2	00 0010	00h FFh				
Bank 3	00 0011	00h FFh				
Banks 4 to 7	00 0100 – 00 0111	00h FFh	GPR	GPR	GPR	0400h 07FFh
Banks 8 to 15	00 1000 – 00 1111	00h FFh	Unimplemented	GPR	GPR	0800h 0FFFh
Banks 16 to 31	01 0000 – 01 1111	00h FFh		Unimplemented		1000h 1FFFh
Banks 32 to 55	10 0000 – 11 0111	00h FFh			Unimplemented	2000h 37FFh
Banks 56 to 62	11 1000 – 11 1110	00h FFh	SFR	SFR	SFR	3800h 3EFFh
Bank 63	11 1111	00h FFh	SFR	SFR	SFR	3800h 3EFFh 3F60h 3FFFh

TABLE 4-5: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES BANK 62

3EFFh	ADCLK	3EDFh	ADLTHH	3EBFh	CM1PCH	3E9Fh	—	3E7Fh	—	3E5Fh	—	3E3Fh	—	3E1Fh	—
3EFEh	ADACT	3EDEh	ADLTHL	3EBEh	CM1NCH	3E9Eh	DAC1CON0	3E7Eh	—	3E5Eh	—	3E3Eh	—	3E1Eh	—
3EFDh	ADREF	3EDDh	—	3EBDh	CM1CON1	3E9Dh	—	3E7Dh	—	3E5Dh	—	3E3Dh	—	3E1Dh	—
3EFCh	ADSTAT	3EDCh	—	3EBCh	CM1CON0	3E9Ch	DAC1CON1	3E7Ch	—	3E5Ch	—	3E3Ch	—	3E1Ch	—
3EFBh	ADCON3	3EDBh	—	3EBBh	CM2PCH	3E9Bh	—	3E7Bh	—	3E5Bh	—	3E3Bh	—	3E1Bh	—
3EFAh	ADCON2	3EDAh	—	3EBAh	CM2NCH	3E9Ah	—	3E7Ah	—	3E5Ah	—	3E3Ah	—	3E1Ah	—
3EF9h	ADCON1	3ED9h	—	3EB9h	CM2CON1	3E99h	—	3E79h	—	3E59h	—	3E39h	—	3E19h	—
3EF8h	ADCON0	3ED8h	—	3EB8h	CM2CON0	3E98h	—	3E78h	—	3E58h	—	3E38h	—	3E18h	—
3EF7h	ADPREH	3ED7h	ADCP	3EB7h	—	3E97h	—	3E77h	—	3E57h	—	3E37h	—	3E17h	—
3EF6h	ADPREL	3ED6h	—	3EB6h	—	3E96h	—	3E76h	—	3E56h	—	3E36h	—	3E16h	—
3EF5h	ADCAP	3ED5h	—	3EB5h	—	3E95h	—	3E75h	—	3E55h	—	3E35h	—	3E15h	—
3EF4h	ADACQH	3ED4h	—	3EB4h	—	3E94h	—	3E74h	—	3E54h	—	3E34h	—	3E14h	—
3EF3h	ADACQL	3ED3h	—	3EB3h	—	3E93h	—	3E73h	—	3E53h	—	3E33h	—	3E13h	—
2EF2h	—	3ED2h	—	3EB2h	—	3E92h	—	3E72h	—	3E52h	—	3E32h	—	3E12h	—
3EF1h	ADPCH	3ED1h	—	3EB1h	—	3E91h	—	3E71h	—	3E51h	—	3E31h	—	3E11h	—
3EF0h	ADRESH	3ED0h	—	3EB0h	—	3E90h	—	3E70h	—	3E50h	—	3E30h	—	3E10h	—
3EEFh	ADRESL	3ECFh	—	3EAFh	—	3E8Fh	—	3E6Fh	—	3E4Fh	—	3E2Fh	—	3E0Fh	—
3EEEh	ADPREVH	3ECEh	—	3EAEh	—	3E8Eh	—	3E6Eh	—	3E4Eh	—	3E2Eh	—	3E0Eh	—
3EEDh	ADPREVL	3ECDh	—	3EADh	—	3E8Dh	—	3E6Dh	—	3E4Dh	—	3E2Dh	—	3E0Dh	—
3EECh	ADRPT	3ECCh	—	3EACh	—	3E8Ch	—	3E6Ch	—	3E4Ch	—	3E2Ch	—	3E0Ch	—
3EEBh	ADCNT	3ECBh	—	3EABh	—	3E8Bh	—	3E6Bh	—	3E4Bh	—	3E2Bh	—	3E0Bh	—
3EEAh	ADACCU	3ECAh	HLVDCON1	3EAAh	—	3E8Ah	—	3E6Ah	—	3E4Ah	—	3E2Ah	—	3E0Ah	—
3EE9h	ADACCH	3EC9h	HLVDCON0	3EA9h	—	3E89h	—	3E69h	—	3E49h	—	3E29h	—	3E09h	—
3EE8h	ADACCL	3EC8h	—	3EA8h	—	3E88h	—	3E68h	—	3E48h	—	3E28h	—	3E08h	—
3EE7h	ADFLTRH	3EC7h	—	3EA7h	—	3E87h	—	3E67h	—	3E47h	—	3E27h	—	3E07h	—
3EE6h	ADFLTRL	3EC6h	—	3EA6h	—	3E86h	—	3E66h	—	3E46h	—	3E26h	—	3E06h	—
3EE5h	ADSTPTH	3EC5h	—	3EA5h	—	3E85h	—	3E65h	—	3E45h	—	3E25h	—	3E05h	—
3EE4h	ADSTPTL	3EC4h	—	3EA4h	—	3E84h	—	3E64h	—	3E44h	—	3E24h	—	3E04h	—
3EE3h	ADERRH	3EC3h	ZCDCON	3EA3h	—	3E83h	—	3E63h	—	3E43h	—	3E23h	—	3E03h	—
3EE2h	ADERRL	3EC2h	—	3EA2h	—	3E82h	—	3E62h	—	3E42h	—	3E22h	—	3E02h	—
3EE1h	ADUTHH	3EC1h	FVRCON	3EA1h	—	3E81h	—	3E61h	—	3E41h	—	3E21h	—	3E01h	—
3EE0h	ADUTHL	3EC0h	CMOUT	3EA0h	—	3E80h	—	3E60h	—	3E40h	—	3E20h	—	3E00h	—

Legend: Unimplemented data memory locations and registers, read as '0'.

Note 1: Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

3: Unimplemented in PIC18(L)F26/27/45/46/47K42.

TABLE 4-8: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES BANK 59

3BFFh	DMA1SIRQ	3BDFh	DMA2SIRQ	3BBFh	—	3B9Fh	—	3B7Fh	—	3B5Fh	—	3B3Fh	—	3B1Fh	—
3BFEh	DMA1AIRQ	3BDEh	DMA2AIRQ	3BBEh	—	3B9Eh	—	3B7Eh	—	3B5Eh	—	3B3Eh	—	3B1Eh	—
3BFDh	DMA1CON1	3BDDh	DMA2CON1	3BBDh	—	3B9Dh	—	3B7Dh	—	3B5Dh	—	3B3Dh	—	3B1Dh	—
3BFCh	DMA1CON0	3BDCh	DMA2CON0	3BBCh	—	3B9Ch	—	3B7Ch	—	3B5Ch	—	3B3Ch	—	3B1Ch	—
3BFBh	DMA1SSAU	3BDBh	DMA2SSAU	3BBBh	—	3B9Bh	—	3B7Bh	—	3B5Bh	—	3B3Bh	—	3B1Bh	—
3BFAh	DMA1SSAH	3BDAh	DMA2SSAH	3BBAh	—	3B9Ah	—	3B7Ah	—	3B5Ah	—	3B3Ah	—	3B1Ah	—
3BF9h	DMA1SSAL	3BD9h	DMA2SSAL	3BB9h	—	3B99h	—	3B79h	—	3B59h	—	3B39h	—	3B19h	—
3BF8h	DMA1SSZH	3BD8h	DMA2SSZH	3BB8h	—	3B98h	—	3B78h	—	3B58h	—	3B38h	—	3B18h	—
3BF7h	DMA1SSZL	3BD7h	DMA2SSZL	3BB7h	—	3B97h	—	3B77h	—	3B57h	—	3B37h	—	3B17h	—
3BF6h	DMA1SPTRU	3BD6h	DMA2SPTRU	3BB6h	—	3B96h	—	3B76h	—	3B56h	—	3B36h	—	3B16h	—
3BF5h	DMA1SPTRH	3BD5h	DMA2SPTRH	3BB5h	—	3B95h	—	3B75h	—	3B55h	—	3B35h	—	3B15h	—
3BF4h	DMA1SPTRL	3BD4h	DMA2SPTRL	3BB4h	—	3B94h	—	3B74h	—	3B54h	—	3B34h	—	3B14h	—
3BF3h	DMA1SCNTH	3BD3h	DMA2SCNTH	3BB3h	—	3B93h	—	3B73h	—	3B53h	—	3B33h	—	3B13h	—
3BF2h	DMA1SCNTL	3BD2h	DMA2SCNTL	3BB2h	—	3B92h	—	3B72h	—	3B52h	—	3B32h	—	3B12h	—
3BF1h	DMA1DSAH	3BD1h	DMA2DSAH	3BB1h	—	3B91h	—	3B71h	—	3B51h	—	3B31h	—	3B11h	—
3BF0h	DMA1DSAL	3BD0h	DMA2DSAL	3BB0h	—	3B90h	—	3B70h	—	3B50h	—	3B30h	—	3B10h	—
3BEFh	DMA1DSZH	3BCFh	DMA2DSZH	3BAFh	—	3B8Fh	—	3B6Fh	—	3B4Fh	—	3B2Fh	—	3B0Fh	—
3BEEh	DMA1DSZL	3BCEh	DMA2DSZL	3BAEh	—	3B8Eh	—	3B6Eh	—	3B4Eh	—	3B2Eh	—	3B0Eh	—
3BEDh	DMA1DPTRH	3BCDh	DMA2DPTRH	3BADh	—	3B8Dh	—	3B6Dh	—	3B4Dh	—	3B2Dh	—	3B0Dh	—
3BECh	DMA1DPTRL	3BCCh	DMA2DPTRL	3BACh	—	3B8Ch	—	3B6Ch	—	3B4Ch	—	3B2Ch	—	3B0Ch	—
3BEBh	DMA1DCNTH	3BCBh	DMA2DCNTH	3BABh	—	3B8Bh	—	3B6Bh	—	3B4Bh	—	3B2Bh	—	3B0Bh	—
3BEAh	DMA1DCNTL	3BCAh	DMA2DCNTL	3BAAh	—	3B8Ah	—	3B6Ah	—	3B4Ah	—	3B2Ah	—	3B0Ah	—
3BE9h	DMA1BUF	3BC9h	DMA2BUF	3BA9h	—	3B89h	—	3B69h	—	3B49h	—	3B29h	—	3B09h	—
3BE8h	—	3BC8h	—	3BA8h	—	3B88h	—	3B68h	—	3B48h	—	3B28h	—	3B08h	—
3BE7h	—	3BC7h	—	3BA7h	—	3B87h	—	3B67h	—	3B47h	—	3B27h	—	3B07h	—
3BE6h	—	3BC6h	—	3BA6h	—	3B86h	—	3B66h	—	3B46h	—	3B26h	—	3B06h	—
3BE5h	—	3BC5h	—	3BA5h	—	3B85h	—	3B65h	—	3B45h	—	3B25h	—	3B05h	—
3BE4h	—	3BC4h	—	3BA4h	—	3B84h	—	3B64h	—	3B44h	—	3B24h	—	3B04h	—
3BE3h	—	3BC3h	—	3BA3h	—	3B83h	—	3B63h	—	3B43h	—	3B23h	—	3B03h	—
3BE2h	—	3BC2h	—	3BA2h	—	3B82h	—	3B62h	—	3B42h	—	3B22h	—	3B02h	—
3BE1h	—	3BC1h	—	3BA1h	—	3B81h	—	3B61h	—	3B41h	—	3B21h	—	3B01h	—
3BE0h	—	3BC0h	—	3BA0h	—	3B80h	—	3B60h	—	3B40h	—	3B20h	—	3B00h	—

Legend: Unimplemented data memory locations and registers, read as '0'.

Note 1: Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

3: Unimplemented in PIC18(L)F26/27/45/46/47K42.

REGISTER 5-9: CONFIGURATION WORD 5L (30 0008h)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/W-1
—	—	—	—	—	—	—	$\overline{CP}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '1'

bit 0 **$\overline{CP}$:** User Program Flash Memory and Data EEPROM Code Protection bit
1 = User Program Flash Memory and Data EEPROM code protection is disabled
0 = User Program Flash Memory and Data EEPROM code protection is enabled

REGISTER 5-10: CONFIGURATION WORD 5H (30 0009h)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **Unimplemented:** Read as '1'

TABLE 5-2: SUMMARY OF CONFIGURATION WORDS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
30 0000h	CONFIG1L	—	RSTOSC<2:0>			—	FEXTOSC<2:0>			1111 1111
30 0001h	CONFIG1H	—	—	FCMEN	—	CSWEN	—	PR1WAY	$\overline{CLKOUTEN}$	1111 1111
30 0002h	CONFIG2L	BOREN<1:0>		$\overline{LPBOREN}$	IVT1WAY	MVECEN	PWRTS<1:0>		MCLRE	1111 1111
30 0003h	CONFIG2H	$\overline{XINST}$	—	$\overline{DEBUG}$	STVREN	PPS1WAY	$\overline{ZCD}$	BORV<1:0>		1111 1111
30 0004h	CONFIG3L	—	WDTE<1:0>		WDTCPS<4:0>					1111 1111
30 0005h	CONFIG3H	—	—	WDTCCS<2:0>			WDTCWS<2:0>			1111 1111
30 0006h	CONFIG4L	$\overline{WRTAPP}$	—	—	$\overline{SAFEN}$	$\overline{BBEN}$	BBSIZE<2:0>			1111 1111
30 0007h	CONFIG4H	—	—	LVP	—	$\overline{WRTSAF}$	$\overline{WRTD}$	$\overline{WRTC}$	$\overline{WRTB}$	1111 1111
30 0008h	CONFIG5L	—	—	—	—	—	—	—	$\overline{CP}$	1111 1111
30 0009h	CONFIG5H	—	—	—	—	—	—	—	—	1111 1111

REGISTER 5-12: REVISION ID: REVISION ID REGISTER

R	R	R	R	R	R	R	R
1	0	1	0	MJRREV<5:2>			
bit 15							bit 8

R	R	R	R	R	R	R	R
MJRREV<1:0>		MNRREV<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Read as '1010'**
These bits are fixed with value '1010' for all devices in this family.

bit 11-6 **MJRREV<5:0>:** Major Revision ID bits
These bits are used to identify a major revision. A major revision is indicated by revision (A0, B0, C0, etc.)
Revision A = 0b00 0000

bit 5-0 **MNRREV<5:0>:** Minor Revision ID bits
These bits are used to identify a minor revision.
Revision A0 = 0b00 0000

6.3 Register Definitions: BOR Control

REGISTER 6-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	—	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-out Reset Enable bit

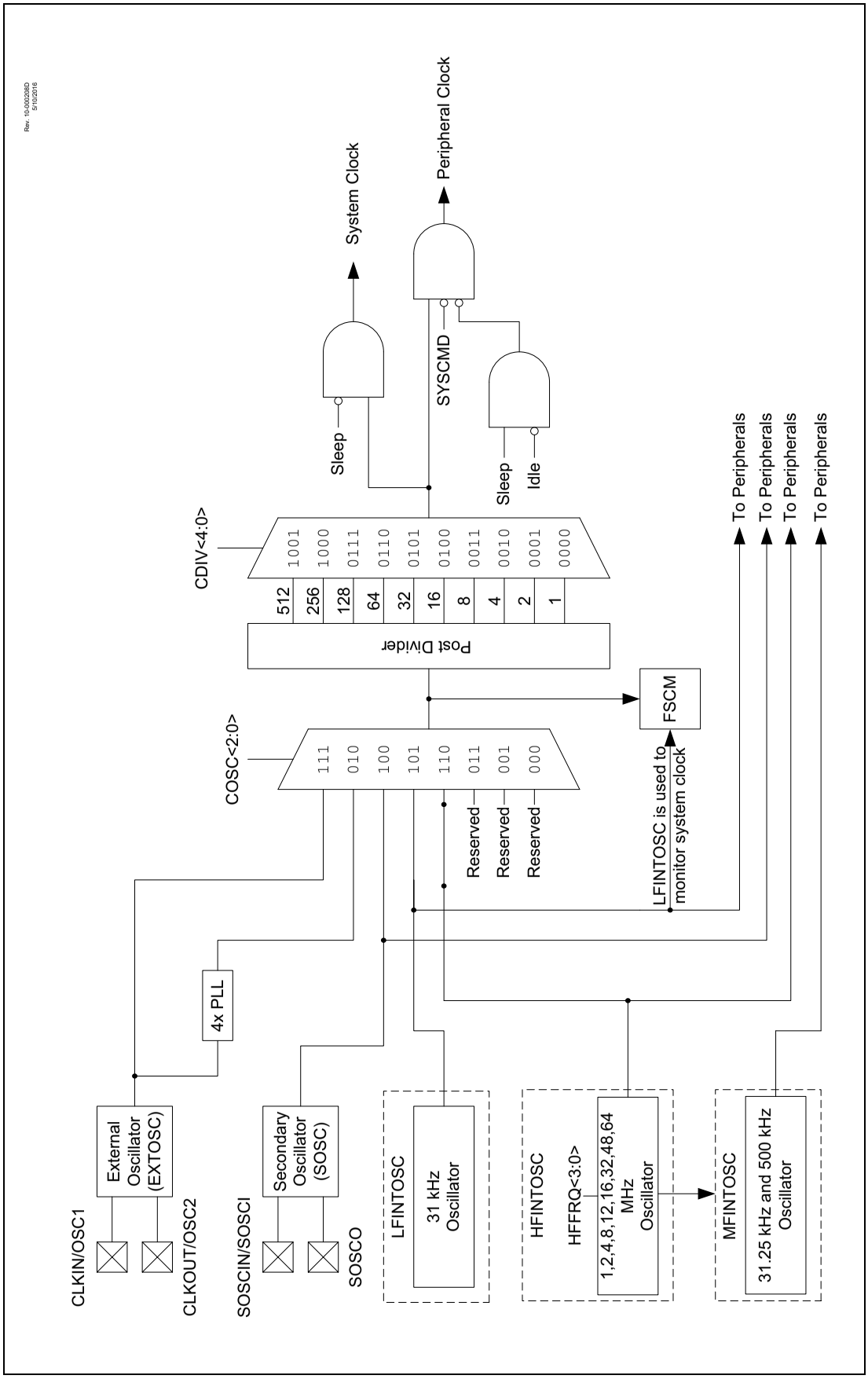
If BOREN ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-out Reset Circuit Ready Status bit

1 = The Brown-out Reset Circuit is active and armed
0 = The Brown-out Reset Circuit is disabled or is warming up

FIGURE 7-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



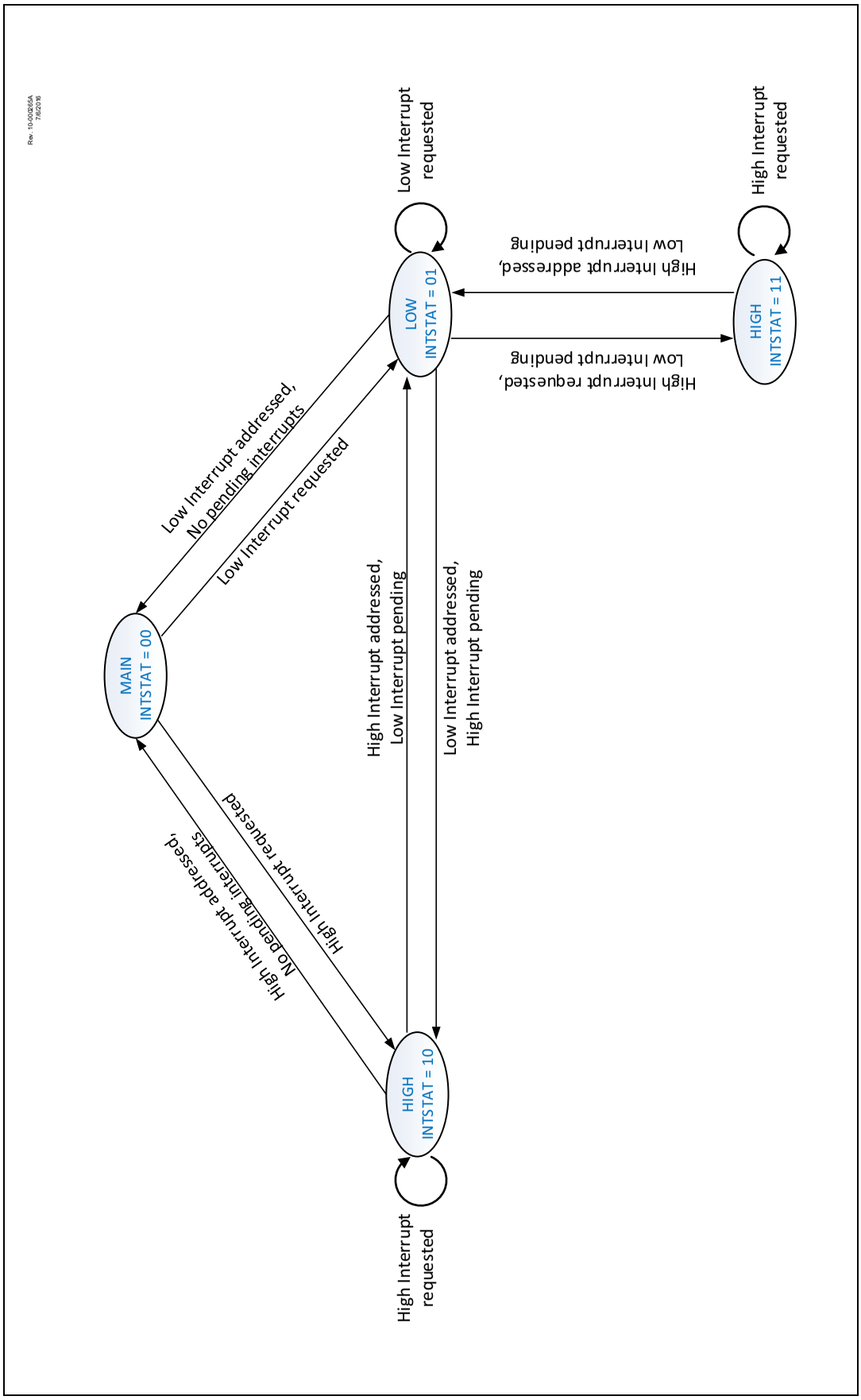


FIGURE 9-1: VECTORED INTERRUPTS STATE TRANSITION DIAGRAM

17.8 Register Definitions: PPS Input Selection

REGISTER 17-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION

U-0	U-0	R/W-m/u(1,3)	R/W-m/u(1)	R/W-m/u(1)	R/W-m/u(1)	R/W-m/u(1)	R/W-m/u(1)
—	—	xxxPPS<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	-n/n = Value at POR and BOR/Value at all other Resets
u = Bit is unchanged	x = Bit is unknown	q = value depends on peripheral
'1' = Bit is set	U = Unimplemented bit, read as '0'	m = value depends on default location for that input
'0' = Bit is cleared		

bit 7-6 **Unimplemented:** Read as '0'

bit 5-3 **xxxPPS<5:3>:** Peripheral xxx Input PORTx Pin Selection bits

See Table 17-1 for the list of available ports and default pin locations.

101 = PORTF(2)
100 = PORTE(3)
011 = PORTD(3)
010 = PORTC
001 = PORTB
000 = PORTA

bit 2-0 **xxxPPS<2:0>:** Peripheral xxx Input PORTx Pin Selection bits

111 = Peripheral input is from PORTx Pin 7 (Rx7)
110 = Peripheral input is from PORTx Pin 6 (Rx6)
101 = Peripheral input is from PORTx Pin 5 (Rx5)
100 = Peripheral input is from PORTx Pin 4 (Rx4)
011 = Peripheral input is from PORTx Pin 3 (Rx3)
010 = Peripheral input is from PORTx Pin 2 (Rx2)
001 = Peripheral input is from PORTx Pin 1 (Rx1)
000 = Peripheral input is from PORTx Pin 0 (Rx0)

Note 1: The Reset value 'm' of this register is determined by device default locations for that input.
2: Reserved on PIC18LF26/27/45/46/57K42 parts.
3: Reserved on PIC18LF26/27K42 parts.

21.3 Timer1/3/5 Prescaler

Timer1/3/5 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the TxCON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMRxH or TMRxL.

21.4 Timer1/3/5 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{SYNC}}$ of the TxCON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake up the processor. However, special precautions in software are needed to read/write the timer (see **Section 21.4.1 "Reading and Writing Timer1/3/5 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

21.4.1 READING AND WRITING TIMER1/3/5 IN ASYNCHRONOUS COUNTER MODE

Reading TMRxH or TMRxL while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads. For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMRxH:TMRxL register pair.

21.5 Timer1/3/5 16-Bit Read/Write Mode

Timer1/3/5 can be configured to read and write all 16 bits of data, to and from, the 8-bit TMRxL and TMRxH registers, simultaneously. The 16-bit read and write operations are enabled by setting the RD16 bit of the TxCON register.

To accomplish this function, the TMRxH register value is mapped to a buffer register called the TMRxH buffer register. While in 16-Bit mode, the TMRxH register is not directly readable or writable and all read and write operations take place through the use of this TMRxH buffer register.

When a read from the TMRxL register is requested, the value of the TMRxH register is simultaneously loaded into the TMRxH buffer register. When a read from the TMRxH register is requested, the value is provided from the TMRxH buffer register instead. This provides the user with the ability to accurately read all 16 bits of the Timer1/3/5 value from a single instance in time. Reference the block diagram in Figure 21-2 for more details.

In contrast, when not in 16-Bit mode, the user must read each register separately and determine if the values have become invalid due to a rollover that may have occurred between the read operations.

When a write request of the TMRxL register is requested, the TMRxH buffer register is simultaneously updated with the contents of the TMRxH register. The value of TMRxH must be preloaded into the TMRxH buffer register prior to the write request for the TMRxL register. This provides the user with the ability to write all 16 bits to the TMRxL:TMRxH register pair at the same time.

Any requests to write to the TMRxH directly does not clear the Timer1/3/5 prescaler value. The prescaler value is only cleared through write requests to the TMRxL register.

21.6.2 TIMER1/3/5 GATE SOURCE SELECTION

The gate source for Timer1/3/5 can be selected using the GSS<4:0> bits of the TMRxGATE register (Register 21-4). The polarity selection for the gate source is controlled by the TxGPOL bit of the TxGCON register (Register 21-2).

Any of the above mentioned signals can be used to trigger the gate. The output of the CMPx can be synchronized to the Timer1/3/5 clock or left asynchronous. For more information see **Section 38.3.1 "Comparator Output Synchronization"**.

21.6.3 TIMER1/3/5 GATE TOGGLE MODE

When Timer1/3/5 Gate Toggle mode is enabled, it is possible to measure the duration between every rising and falling edge of the gate signal.

The Timer1/3/5 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 21-5 for timing details.

Timer1/3/5 Gate Toggle mode is enabled by setting the GTM bit of the TxGCON register. When the GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note:	Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

21.6.4 TIMER1/3/5 GATE SINGLE-PULSE MODE

When Timer1/3/5 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1/3/5 Gate Single-Pulse mode is first enabled by setting the GSPM bit in the TxGCON register. Next, the GGO/DONE bit in the TxGCON register must be set. The Timer1/3/5 will be fully enabled on the next incrementing edge of the gate signal. On the next trailing edge of the pulse, the GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1/3/5 until the GGO/DONE bit is once again set in software.

Clearing the TxGSPM bit of the TxGCON register will also clear the GGO/DONE bit. See Figure 21-6 for timing details.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the period on the Timer1/3/5 gate source to be measured. See Figure 21-7 for timing details.

21.6.5 TIMER1/3/5 GATE VALUE STATUS

When Timer1/3/5 Gate Value Status is utilized, it is possible to read the most current level of the gate signal. The value is stored in the GVAL bit in the TxGCON register. The GVAL bit is valid even when the Timer1/3/5 gate is not enabled (GE bit is cleared).

21.6.6 TIMER1/3/5 GATE EVENT INTERRUPT

When Timer1/3/5 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of GVAL occurs, the TMRxGIF flag bit in the respective PIR register will be set. If the TMRxGIE bit in the respective PIE register is set, then an interrupt will be recognized.

The TMRxGIF flag bit operates even when the Timer1/3/5 gate is not enabled (GE bit is cleared).

For more information on selecting high or low priority status for the Timer1/3/5 Gate Event Interrupt see **Section 9.0 "Interrupt Controller"**.

21.12 Register Definitions: Timer1/3/5

Long bit name prefixes for the Timer1/3/5 are shown below. Refer to **Section 1.3.2.2 "Long Bit Names"** for more information.

Peripheral	Bit Name Prefix
Timer1	T1
Timer3	T3
Timer5	T5

REGISTER 21-1: TXCON: TIMERx CONTROL REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	U-0	R/W-0/u	R/W-0/0	R/W-0/u
—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	u = unchanged

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **$\overline{\text{SYNC}}$:** Timerx External Clock Input Synchronization Control bit
TMRxCLK = FOSC/4 or FOSC:
This bit is ignored. Timer1 uses the incoming clock as is.
Else:
1 = Do not synchronize external clock input
0 = Synchronize external clock input with system clock

bit 1 **RD16:** 16-Bit Read/Write Mode Enable bit
1 = Enables register read/write of Timerx in one 16-bit operation
0 = Enables register read/write of Timerx in two 8-bit operation

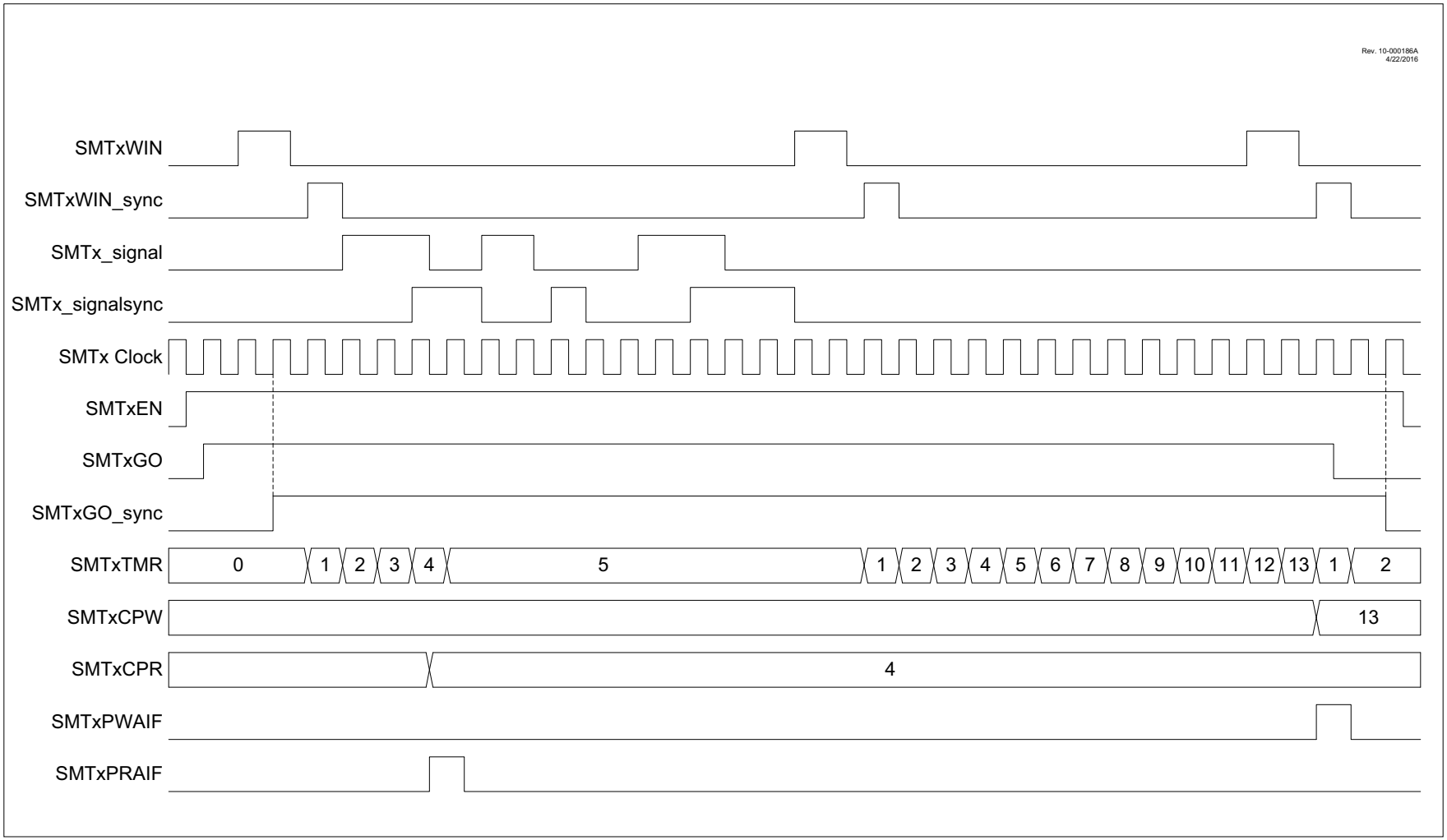
bit 0 **ON:** Timerx On bit
1 = Enables Timerx
0 = Disables Timerx

22.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the T2CON register are cleared).
- The diagrams illustrate any clock except FOSC/4 and show clock-sync delays of at least two full cycles for both ON and T2TMR_ers. When using FOSC/4, the clock-sync delay is at least one instruction period for T2TMR_ers; ON applies in the next instruction period.
- ON and T2TMR_ers are somewhat generalized, and clock-sync delays may produce results that are slightly different than illustrated.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 23.0 "Capture/ Compare/PWM Module"** and **Section 24.0 "Pulse-Width Modulation (PWM)"**. The signals are not a part of the T2TMR module.

FIGURE 25-14: TIME OF FLIGHT MODE REPEAT ACQUISITION TIMING DIAGRAM



REGISTER 25-2: SMT1CON1: SMT CONTROL REGISTER 1

R/W/HC-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
GO	REPEAT	—	—	MODE<3:0>			
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **GO:** GO Data Acquisition bit
1 = Incrementing, acquiring data is enabled
0 = Incrementing, acquiring data is disabled

bit 6 **REPEAT:** SMT Repeat Acquisition Enable bit
1 = Repeat Data Acquisition mode is enabled
0 = Single Acquisition mode is enabled

bit 5-4 **Unimplemented**: Read as '0'

bit 3-0 **MODE<3:0>** SMT Operation Mode Select bits
1111 = Reserved
•
•
•
1011 = Reserved
1010 = Windowed counter
1001 = Gated counter
1000 = Counter
0111 = Capture
0110 = Time of flight
0101 = Gated windowed measure
0100 = Windowed measure
0011 = High and low time measurement
0010 = Period and Duty-Cycle Acquisition
0001 = Gated Timer
0000 = Timer

FIGURE 30-2: On Off Keying (OOK) Synchronization

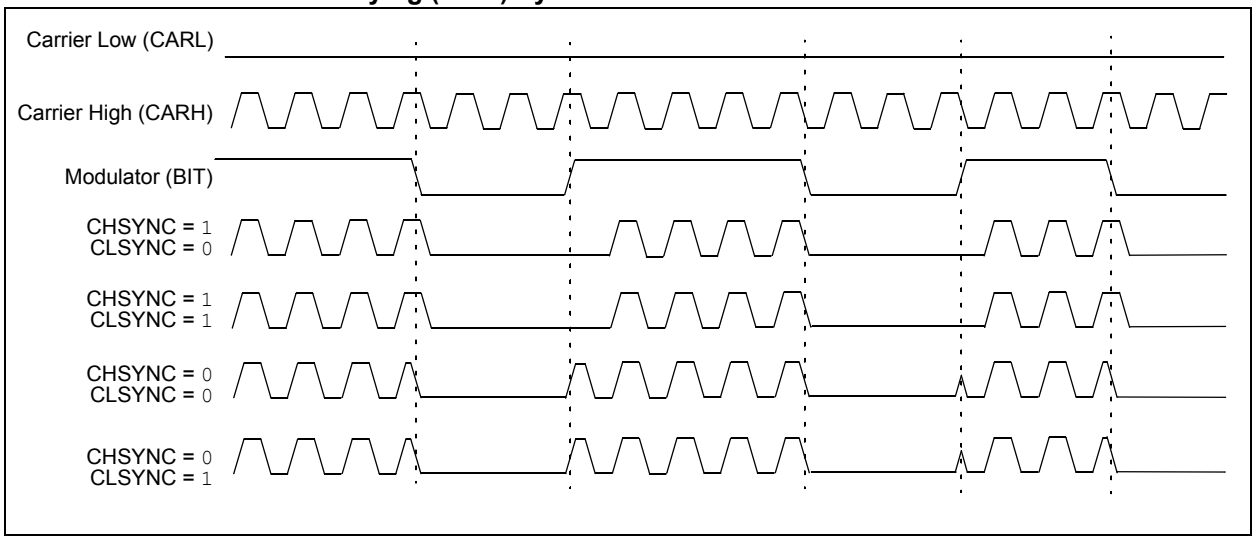


FIGURE 30-3: No Synchronization (CHSYNC = 0, CLSYNC = 0)

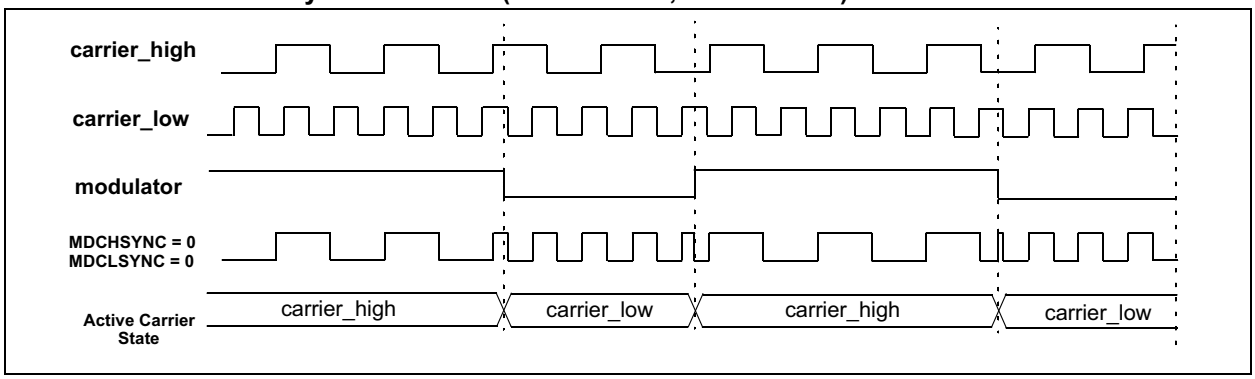
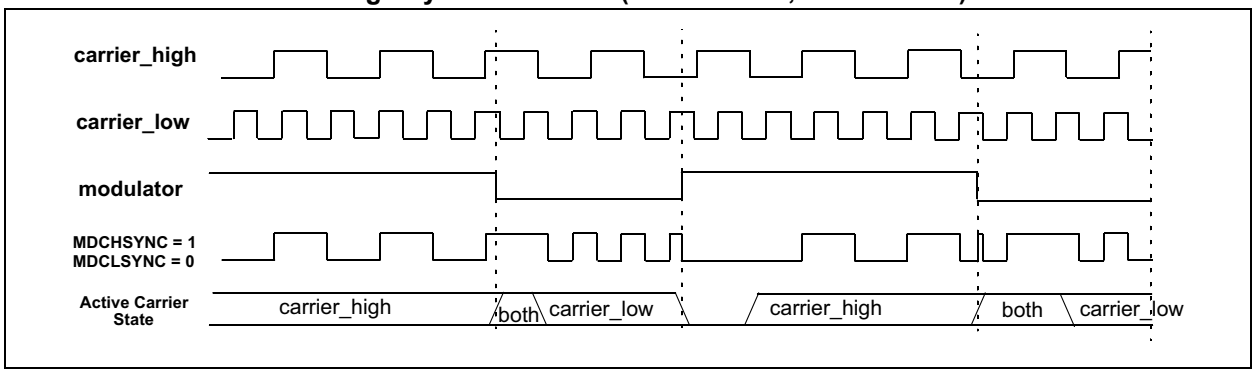


FIGURE 30-4: Carrier High Synchronization (CHSYNC = 1, CLSYNC = 0)



30.11 Register Definitions: Modulation Control

Long bit name prefixes for the Modulation peripheral is shown below. Refer to **Section 1.3.2.2 "Long Bit Names"** for more information.

Peripheral	Bit Name Prefix
MD1	MD1

REGISTER 30-1: MD1CON0: MODULATION CONTROL REGISTER 0

R/W-0/0	U-0	R-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
EN	—	OUT	OPOL	—	—	—	BIT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** Modulator Module Enable bit
1 = Modulator module is enabled and mixing input signals
0 = Modulator module is disabled and has no output

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Modulator Output bit
Displays the current output value of the Modulator module.(1)

bit 4 **OPOL:** Modulator Output Polarity Select bit
1 = Modulator output signal is inverted; idle high output
0 = Modulator output signal is not inverted; idle low output

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BIT:** Allows software to manually set modulation source input to module(2)
1 = Modulator selects Carrier High
0 = Modulator selects Carrier Low

Note 1: The modulated output frequency can be greater and asynchronous from the clock that updates this register bit, the bit value may not be valid for higher speed modulator or carrier signals.
2: BIT bit must be selected as the modulation source in the MD1SRC register for this operation.

FIGURE 32-7: CLOCKING DETAIL-MASTER MODE, CKE/SMP = 0/0

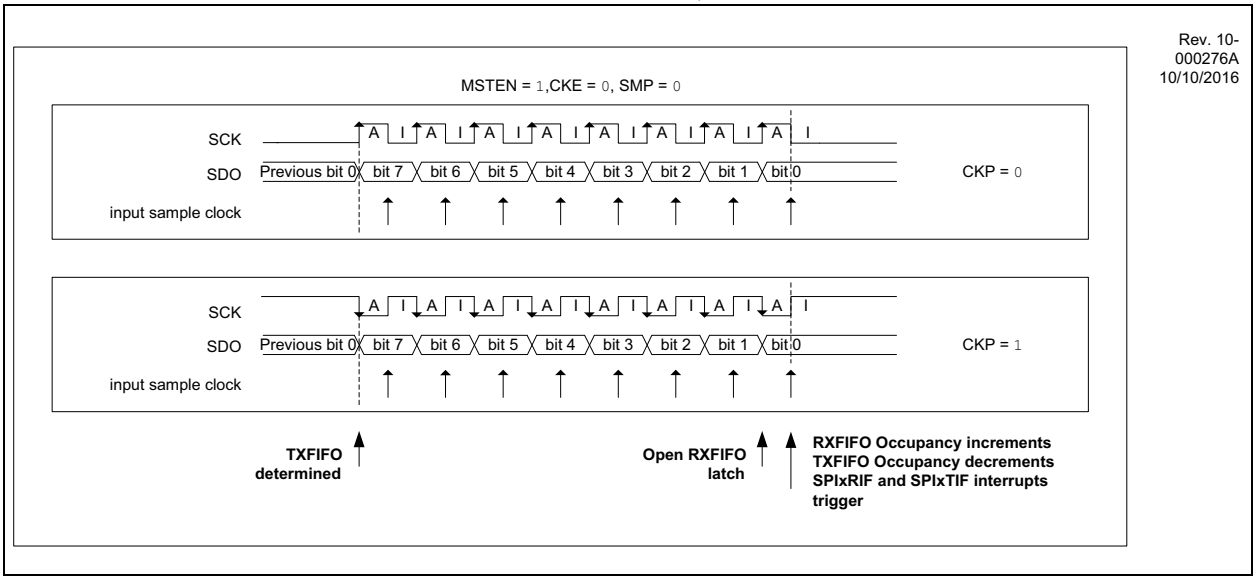
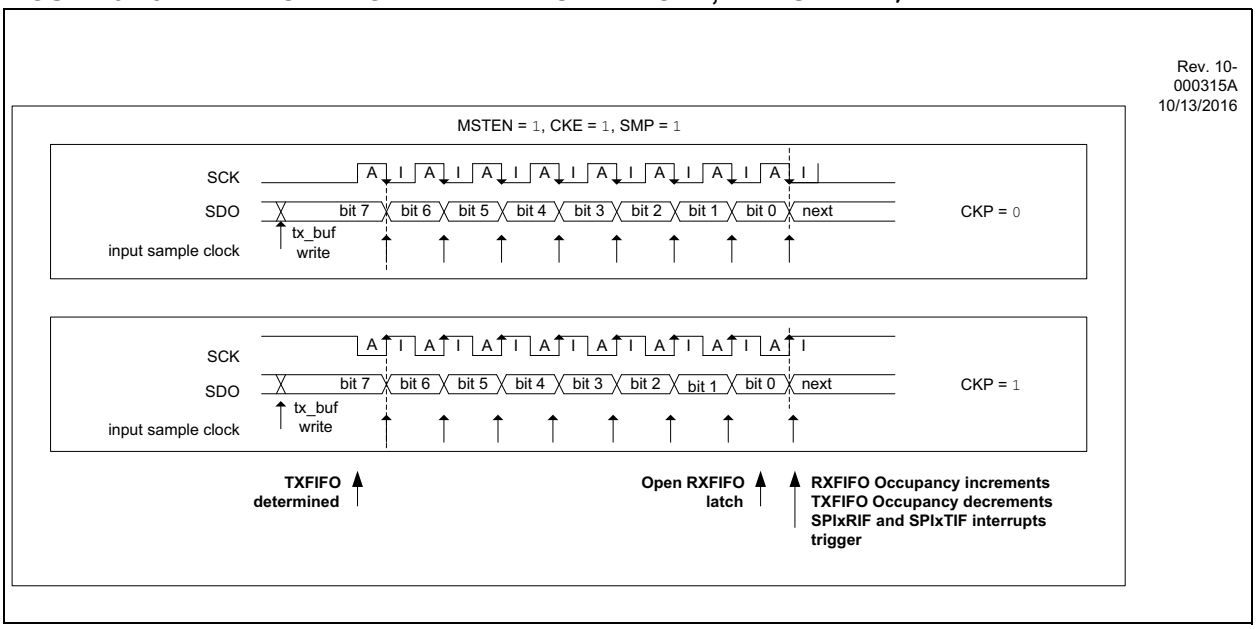


FIGURE 32-8: CLOCKING DETAIL - MASTER MODE, CKE/SMP = 1/1



32.6.3 SLAVE MODE SLAVE SELECT

In Slave mode, an external Slave Select Signal can be used to synchronize communication with the Master device. The Slave Select line is held in its inactive state (high by default) until the master device is ready to communicate. When the Slave Select transitions to its active state, the slave knows that a new transmission is starting.

When the Slave Select goes false at the end of the transmission the receive function of the selected SPI Slave device returns to the inactive state. The slave is then ready to receive a new transmission when the Slave Select goes True again.

The Slave Select signal is received on the $\overline{SS}$ input pin. This pin is remappable with the SPIxSSPPS register (see **Section 17.1 "PPS Inputs"**). When the input on this pin is true, transmission and reception are enabled, and the SDO pin is driven. When the input on this pin is false, the SDO pin is either tri-stated (if the TRIS bit associated with the SDO pin is set) or driven to the value of the LAT bit associated with the SDO pin (if the TRIS bit associated with the SDO pin is cleared). In addition, the SCK input is ignored.

If the SS input goes False, while a data transfer is still in progress, it is considered a slave select fault. The SSFLT bit of SPIxCON2 indicates whether such an event has occurred. The transfer counter value determines the number of bits in a valid data transfer (see **Section 32.4 "Transfer Counter"** for more details).

The Slave Select polarity is controlled by the SSP bit of SPIxCON1. When SSP is set (its default state), the Slave Select input is active-low, and when it is cleared, the Slave Select input is active-high.

The Slave Select for the SPI module is controlled by the SSET bit of SPIxCON2. When the bit is cleared (its default state), the slave select will act as described above. When the bit is set, the SPI module will behave as if the SS input was always in its active state.

Note:	When SSET is set, the effective SS(in) signal is always active. Hence, the SSFLT bit may be disregarded.

32.6.4 SLAVE MODE CLOCK CONFIGURATION

In Slave Mode, SCK is an input, and must be configured to the same polarity and clock edge as the master device. As in Master mode, the polarity of the clock input is controlled by the CKP bit of SPIxCON1 and the clock edge used for transmitting data is controlled by the CKE bit of SPIxCON1.

32.6.5 DAISY-CHAIN CONFIGURATION

The SPI bus can be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device connected to all slave devices (alternately, the slave devices can be configured to ignore the slave select line by setting the SSET bit). In a typical Daisy-Chain configuration, the SCK signal from the master is connected to each of the slave device SCK inputs. However, the SCK input and output are separate signals selected by the PPS control. When the PPS selection is made to configure the SCK input and SCK output on separate pins then, the SCK output will follow the SCK input, allowing for SCK signals to be daisy-chained like the SDO/SDI signals.

Figure 32-12 shows the block diagram of a typical daisy-chain connection, and Figure 32-13 shows the block diagram of a daisy-chain connection possible using this SPI module.

REGISTER 36-22: ADPREVH: ADC PREVIOUS RESULT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
PREV<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PREV<15:8>**: Previous ADC Results bits
If ADPSIS = 1:
Upper byte of FLTR at the start of current ADC conversion
If ADPSIS = 0:
Upper bits of ADRES at the start of current ADC conversion**(1)**

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the FM bit.

REGISTER 36-23: ADPREVL: ADC PREVIOUS RESULT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
PREV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PREV<7:0>**: Previous ADC Results bits
If ADPSIS = 1:
Lower byte of FLTR at the start of current ADC conversion
If ADPSIS = 0:
Lower bits of ADRES at the start of current ADC conversion**(1)**

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the FM bit.