



#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf46k42-i-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 1.3 Register and Bit naming conventions

#### 1.3.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

#### 1.3.2 BIT NAMES

There are two variants for bit names:

- · Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

#### 1.3.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the T0CON0 register can be set in C programs with the instruction T0CON0bits.EN = 1.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

#### 1.3.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the Timer0 enable bit is the Timer0 prefix, T0, appended with the enable bit short name, EN, resulting in the unique bit name T0EN.

Long bit names are useful in both C and assembly programs. For example, in C the TOCON0 enable bit can be set with the TOEN = 1 instruction. In assembly, this bit can be set with the BSF TOCON0, TOEN instruction.

#### 1.3.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. For example, the four Least Significant bits of the T0CON0 register contain the output prescaler select bits. The short name for this field is OUTPS and the long name is T0OUTPS. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the Timer0 output prescaler to the 1:6 Postscaler:

#### TOCONObits.OUTPS = 0x5;

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name OUTPS3. The following two examples demonstrate assembly program sequences for setting the Timer0 output prescaler to 1:6 Postscaler:

#### Example 1:

MOVLW ~(1<<0UTPS3 | 1<<0UTPS1) ANDWF T0CON0,F MOVLW 1<0UTPS2 | 1<<0UTPS0 IORWF T0CON0,F

#### Example 2:

BCF	TOCONO,OUTPS3
BSF	TOCONO,OUTPS2
BCF	TOCONO,OUTPS1
BSF	TOCONO,OUTPSO

#### 1.3.3 REGISTER AND BIT NAMING EXCEPTIONS

#### 1.3.3.1 Status, Interrupt, and Mirror Bits

Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

#### TABLE 4-5: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES BANK 62

_								_		_					
3EFFh	ADCLK	3EDFh	ADLTHH	3EBFh	CM1PCH	3E9Fh	_	3E7Fh	—	3E5Fh		3E3Fh	_	3E1Fh	—
3EFEh	ADACT	3EDEh	ADLTHL	3EBEh	CM1NCH	3E9Eh	DAC1CON0	3E7Eh		3E5Eh		3E3Eh		3E1Eh	—
3EFDh	ADREF	3EDDh	_	3EBDh	CM1CON1	3E9Dh	—	3E7Dh	_	3E5Dh	_	3E3Dh	_	3E1Dh	—
3EFCh	ADSTAT	3EDCh	—	3EBCh	CM1CON0	3E9Ch	DAC1CON1	3E7Ch	—	3E5Ch	—	3E3Ch	—	3E1Ch	—
3EFBh	ADCON3	3EDBh	—	3EBBh	CM2PCH	3E9Bh	—	3E7Bh	—	3E5Bh	—	3E3Bh	—	3E1Bh	—
3EFAh	ADCON2	3EDAh	—	3EBAh	CM2NCH	3E9Ah	—	3E7Ah	—	3E5Ah	—	3E3Ah	—	3E1Ah	—
3EF9h	ADCON1	3ED9h	_	3EB9h	CM2CON1	3E99h	_	3E79h	_	3E59h		3E39h	_	3E19h	—
3EF8h	ADCON0	3ED8h	_	3EB8h	CM2CON0	3E98h	_	3E78h	_	3E58h		3E38h	_	3E18h	—
3EF7h	ADPREH	3ED7h	ADCP	3EB7h	_	3E97h	_	3E77h	_	3E57h		3E37h	_	3E17h	—
3EF6h	ADPREL	3ED6h	_	3EB6h	_	3E96h	_	3E76h	_	3E56h	_	3E36h	_	3E16h	—
3EF5h	ADCAP	3ED5h	_	3EB5h	_	3E95h	_	3E75h	_	3E55h		3E35h	_	3E15h	—
3EF4h	ADACQH	3ED4h	_	3EB4h		3E94h	_	3E74h	_	3E54h	_	3E34h		3E14h	—
3EF3h	ADACQL	3ED3h	_	3EB3h	_	3E93h	_	3E73h	_	3E53h		3E33h	_	3E13h	—
2EF2h	—	3ED2h	_	3EB2h	_	3E92h	_	3E72h	_	3E52h		3E32h	_	3E12h	—
3EF1h	ADPCH	3ED1h	_	3EB1h	_	3E91h	_	3E71h	_	3E51h		3E31h	_	3E11h	—
3EF0h	ADRESH	3ED0h	_	3EB0h	_	3E90h	_	3E70h	_	3E50h		3E30h	_	3E10h	—
3EEFh	ADRESL	3ECFh	_	3EAFh	_	3E8Fh	_	3E6Fh	_	3E4Fh	_	3E2Fh	_	3E0Fh	—
3EEEh	ADPREVH	3ECEh	—	3EAEh	—	3E8Eh	—	3E6Eh	—	3E4Eh	—	3E2Eh	—	3E0Eh	—
3EEDh	ADPREVL	3ECDh	_	3EADh	_	3E8Dh	_	3E6Dh	_	3E4Dh		3E2Dh	_	3E0Dh	—
3EECh	ADRPT	3ECCh	_	3EACh	_	3E8Ch	_	3E6Ch	_	3E4Ch		3E2Ch	_	3E0Ch	
3EEBh	ADCNT	3ECBh	_	3EABh	_	3E8Bh	_	3E6Bh	_	3E4Bh		3E2Bh	_	3E0Bh	—
3EEAh	ADACCU	3ECAh	HLVDCON1	3EAAh	_	3E8Ah	_	3E6Ah	_	3E4Ah		3E2Ah	_	3E0Ah	—
3EE9h	ADACCH	3EC9h	HLVDCON0	3EA9h	_	3E89h	_	3E69h	_	3E49h		3E29h	_	3E09h	—
3EE8h	ADACCL	3EC8h	—	3EA8h	—	3E88h	—	3E68h	—	3E48h	—	3E28h	—	3E08h	—
3EE7h	ADFLTRH	3EC7h	—	3EA7h	—	3E87h	—	3E67h	—	3E47h	—	3E27h	—	3E07h	—
3EE6h	ADFLTRL	3EC6h	—	3EA6h	—	3E86h		3E66h	—	3E46h	—	3E26h	—	3E06h	—
3EE5h	ADSTPTH	3EC5h	—	3EA5h	—	3E85h		3E65h	—	3E45h	—	3E25h	—	3E05h	—
3EE4h	ADSTPTL	3EC4h	—	3EA4h	—	3E84h		3E64h	—	3E44h	—	3E24h	—	3E04h	—
3EE3h	ADERRH	3EC3h	ZCDCON	3EA3h		3E83h		3E63h	—	3E43h	—	3E23h	—	3E03h	—
3EE2h	ADERRL	3EC2h	—	3EA2h		3E82h		3E62h	—	3E42h	—	3E22h	—	3E02h	—
3EE1h	ADUTHH	3EC1h	FVRCON	3EA1h	—	3E81h	—	3E61h	—	3E41h	—	3E21h	—	3E01h	—
3EE0h	ADUTHL	3EC0h	CMOUT	3EA0h	_	3E80h	_	3E60h	—	3E40h	—	3E20h	_	3E00h	—

Legend: Unimplemented data memory locations and registers, read as '0'.

**Note 1:** Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

**3:** Unimplemented in PIC18(L)F26/27/45/46/47K42.

INTCOM         GIE/GIEH         GIEL         IPPEN         T         INT         INT_EOG         INTGEOR         INTREE         UIRX         UIRX         UIRX         IDAAL         DMAADORE         UMAADORE         UMAADORE         UMAADORE         UMAADORE         UMAADORE         UMAADORE         UIRX         IDAAL         IDAAL <thidaal< th=""> <thida< th=""><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Register on Page</th></thida<></thidaal<>	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCOMSTAT+™¬¬ <t< td=""><td>INTCON0</td><td>GIE/GIEH</td><td>GIEL</td><td>IPEN</td><td>-</td><td>-</td><td>INT2EDG</td><td>INT1EDG</td><td>INT0EDG</td><td>135</td></t<>	INTCON0	GIE/GIEH	GIEL	IPEN	-	-	INT2EDG	INT1EDG	INT0EDG	135
Piefor Piefor Piefor CirtikeCKCIE 	INTCON1	STAT	<1:0>	-	-	-	-	-	-	136
PietSMT1PPAMESMT1RECTIEADTEDAIDEZOENINTOREINTOR1448PiezTRRNOEUIESPIITXIESPIITXIEDMAIAREDMAIAREDMAIORIEDMAISORTEIACSITXIE150PiezTRRNOEUIEUIEUITXIEUTRNEUZCIEIZCIENEIZCIENEIZCIENEIZCIENEIZCITXIE150PiesTRRNOEUIZCIEDMAZORDMAZORNEDMAZORNEDMAZORNEDMAZORNEIZCIENEIZCIENEIZCIENEIZCIENE155PiesTMRSOETMRSIEUZIEUZIEUZIEUZIECOP3ECOP3ETMRNE155PiesTTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ECOP3ETMRNE155PiesTOCIFCRCIFSCANFSMTIFCSWFOSFFHUDFSWF133PiesTOCIFCRCIFSCANFSMTIFOTTADDFZCIFNTTOF138PiesTMRSIFSMTIFSMTIFOTTDMAZORFDMAZORFMMADCHMADCHMATCH141PiesTMRSIFSMTIFSMTIFCOF1FDMAZORFDMAZORFMAGCHMATCH142141Pies <t< td=""><td>PIE0</td><td>IOCIE</td><td>CRCIE</td><td>SCANIE</td><td>NVMIE</td><td>CSWIE</td><td>OSFIE</td><td>HLVDIE</td><td>SWIE</td><td>147</td></t<>	PIE0	IOCIE	CRCIE	SCANIE	NVMIE	CSWIE	OSFIE	HLVDIE	SWIE	147
PE2I2C1RXIESPI17IESPI17IESPI17XIEDMA1ACDMA1ORIEDMA1ORIEDMA1ORIEDMA1ORIEDMA1ORIEMATSONTEM41SONTE149PIE3TURRIEUTIEUTIEUTIRUEUTRUEUTRUEIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIST1PIE4CLC1IECORVIEMA2CREDMA2ORTEDMA2CNTEDMA2CREDMA2CREIMA2EIZC1EIZC1EIZC1EIZC1EIST2PIE5TMR3GETMR3EUZIEUZIECUC2IECWG2IETCCITRAE155PIE6TMR3GETMR3EINT2IECIC2IECWG2IETCCC2IEITMR8E155PIE10TTTTTTCCC2IEKM33EKTRAE155PIE10TCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIFE137PIR1SMTIPMAFSWT1FFSMT1FFSMT1FFDMA1AFDMA1ORIFDMA1ORIFMASCNTF138PIR2IZC1RXIFSMT1FFSW1TIFSWIFTFUZXIFUZXIFIZC1FFIZC1FF141PIR4CLC1FFFMR0FUTIFFSWIFTFUXXIFFUXXIFFUXXIFF12C1FF141PIR4IZC1FFITM81FNT1FFSWIFTFUXXIFFUXXIFFUXXIFF12C1FF12C1FF141PIR4CLC1FFOWG1FNCAC	PIE1	SMT1PWAIE	SMT1PRAIE	SMT1IE	C1IE	ADTIE	ADIE	ZCDIE	INT0IE	148
PE3TMR0IEU11EU1EIEU1TXIEU17XIEU12CIEE12C1EIE12C1EIE12C1EIE12C1TXIE150PIE4ICC2TXIEICC2TIF	PIE2	I2C1RXIE	SPI1IE	SPI1TXIE	SPI1RXIE	DMA1AIE	DMA10RIE	DMA1DCNTIE	DMA1SCNTIE	149
PE4CLC1IECWG1IENC01IETCCP1IETMR2IETMR2IETMR1GIETMR1IE151PIE6IZCZTXIEIZCZTXIEIZCZRXIEDMAZANEDMAZORIEDMAZORIEDMAZORIEDMAZORIEDMAZORIEIZCZIEINT1IE152PIE6TMR3GIETMR3IEUZIEUZIEUZIEUZIEUZIEIZCZIETMR4IE155PIE7TTIITIZIECLC2IECWG2IECP3IETMR4IE155PIE8TTTITTCLC3IECWG3IECP3IETMR6IE156PIE70TTTTCLC3IECWG3IECD3IETMR6IE156PIR0IOCIFCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIF133PIR11SMT1PRAIFSMT1FAIFSPITIAIFSPITIAIFSPITIAIFDMA1AIFDMA1ORIFDMATOCTIFDMATOCTIF141PIR3IICIFCLC1IFCWG1IFNC01IFITTCCP1IFTMR2IFTMR1GIF141PIR4CLC1IFCWG3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFUZIFIF142PIR4TMR3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFTMR1GIF141PIR5IZC2TXFIZC2RXFDMA2AFDMA2ORIFDMA2ORIFDMA2ORIFDMA2ORIFDMA2ORIFCI2IFITMR3IF141PIR6TMR3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFUZIFIFI	PIE3	TMR0IE	U1IE	U1EIE	U1TXIE	U1RXIE	I2C1EIE	I2C1IE	I2C1TXIE	150
PIESI2C2TXIEI2C2RXIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDVA20EC2IEINTIE152PIEGTMTMITMR3IEUZIEUZIEUZIKIEUZRIEIZC2ELEIZC2ELEIZC2ELEIS3PIE7TTITMR3IEINTIECLC2IECWG2IETCC2PIETMR4IE155PIE3TTTTCLC3IECWG3IECC2IETMR4IE155PIE10TTTTTCLC3IECWG3IECC2IETMR4IE155PIR10NOCIFCRCIFSCANIFNVMIFCSUFOSFFHLVDIFSWITIF137PIR1SMT1PMAIFSMT1FSPITAIFSPITAFADIFADIFZCDIFINTOIF138PIR2I2C1RXIFSPITAFSPITAFSPITAFDMA10FFDMA10CNFDMA10CNTFDMA10CNTF140PIR3TMR0FU1FU1FFUTTIFUTR1FUTR1FTMR1GFIMT1F141PIR5I2C2TXF10/2CXFDMA2AFDMA2AFDMA2CNTFDMA2SCNTFC2EFFINT1F142PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2TKFI2C1TXF144PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2FFIMT4F144PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2FFIMT6F145PIR7<	PIE4	CLC1IE	CWG1IE	NCO1IE	—	CCP1IE	TMR2IE	TMR1GIE	TMR1IE	151
PIEGTMR3GIETMR3IEU2IEU2IEIU2IEIEU2IXIEU2RXIEI2C2IEII12C2IE1533PIE7CC22IETMR4IE1544PIE8TMR5IETMR5IECC22IETMR6IE1555PIE9CLC3IECWG3IECCP3IETMR6IE1556PIE10CLC3IECWG3IECCP3IETMR6IE1556PIR0IOCIFCRCIFSCANIFN/MIFCSWIFOSFIFHIVDIFSWIF1377PIR1SMT1PWAIFSMT1PRAIFSMT1IFC11FAD1FAD1FZCDIFINTOF138PIR2I2C17XIFSP11FXSP11FXIFSP11FXIFDMA1AIFDMA1CRIFDMA1CRIFDMA1CRIFIMACRIFIMACRIF1411PIR3TMR0IFU11FU11EIFU11XIFU1RXIFIZC1FIFIZC1FIFIZC1TXIF1420PIR4CLC1IFCWG1IFNC01IFCCP1IFTMR2IFTMR1GFTMR1IF1442PIR3ITM2FIDM2FDMA2CRIFDMA2CNTIFDMA2SCNTIFIZC2IFIZC1TXIF1420PIR4CLC1IFCWG1IFU2IFU2IFU2IFU2IFU2IFIZC1TXIF1441PIR5ITM2FIDM2FCLC2IFCWG2IFCCP2IFTMR1IF1442PIR6ITM2FITM2FU2IFU2IFU2IFU2IFIZC1FIFIZC1FFIZC	PIE5	I2C2TXIE	I2C2RXIE	DMA2AIE	DMA2ORIE	DMA2DCNTIE	DMA2SCNTIE	C2IE	INT1IE	152
PIE7INT2IECLC2IECWG2IECCP2IETMR4IE154PIE8TMR5IETMR5IE155PIE9155PIE9CLC3IECWG3IECCP3IETMR6IE155PIR0IOCIFCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIF137PIR1SMT1PWAFSMT1PAFAFSMT1FCHFADTFADFZCDIFINTOIF138PIR2ICC1FCRCIFSCANIFOTHADM1AIFDMA1ORIFDMAIONIFDMAISCNTF139PIR3TMR0IFU11FU11FU11FU11FU11FU11F141141PIR4CLC1FCWG1FNC01F-CCP1IFTMR2IFTMR6IFTMR1F141PIR512C2TXF12C3TXFDMA2AFDMA2ORIFDMA2CNTFDMA2SCNTFC2FINT1F142PIR6TMR3GFTMR3FU2FU2FU2TKFU2RXF12C2EF12C2IF143PIR7T145PIR8TMR3GFTMR3FV2FU2FU2TKFU2RXF12C2FF12C2IF144PIR9TMR3GFTMR3FSMT1PO145PIR10<	PIE6	TMR3GIE	TMR3IE	U2IE	U2EIE	U2TXIE	U2RXIE	I2C2EIE	I2C2IE	153
PIE8TIMRSGIETIMRSIE111 <td>PIE7</td> <td>_</td> <td>-</td> <td>INT2IE</td> <td>CLC2IE</td> <td>CWG2IE</td> <td>-</td> <td>CCP2IE</td> <td>TMR4IE</td> <td>154</td>	PIE7	_	-	INT2IE	CLC2IE	CWG2IE	-	CCP2IE	TMR4IE	154
PIE9             CLC3IE         CWG3IE         CCP3IE         TMR6IE         155           PIE10             CLC3IE         CCP3IE         TMR6IE         155           PIR0         IOCIF         CRCIF         SCANIF         IC           CLC4IE         CCP4IE         156           PIR0         SMT1PAUR         SMT1PAUR         SCANIF         CIF         ADTIF         ADDIF         ADDIF         ADDIF         MA10CNIF         DMA1SCNTF         138           PIR2         12C1RXIF         SP1IIF         SP1ITXIF         SP1IXIF         DMA1AIF         DMA1ORIF         DMA1SCNTF         139           PIR3         TMR0IF         U11F         U1EIF         U1XIF         U1XIF         U2RUF         12C21F         12C21F         12C21F         12C21F         141           PIR3         TMR3GIF         TMR3IF          CLC3IF         CW31F         CMA2CNTF         DMA2CNTF         DMA2CNTF         CL2IF         141           PIR4         CLC1F         TMR3IF         TMR3IF         TMR3IF         TMR3IF         TMR3IF         145           PIR7	PIE8	TMR5GIE	TMR5IE	-	—	-	—	—	_	155
PHE10         —         —         —         —         —         CLC4HE         CCP4HE         156           PIR0         IOCIF         CRCH         SCAMIF         NVMIF         CSWIF         OSFIF         HLVDIF         SWITF         137           PIR1         SMT1PWAHF         SMT1PRAF         SMT1H         C1IF         ADTIF         ADIF         ZCDIF         INTOIF         138           PIR2         IZC1RXIF         SP114F         SMT1VF         DMA1ALF         DMA1ALF         DMA1ALF         DMA1ALF         DMA1ALF         DMA1ALF         IMATISCHTF         139           PIR3         TMR0IF         U1IF         U1EF         U1TKIF         U1RXIF         IZC1EF         IZC1FF         IZC1TXF         IZC2TXF         IZC2XF         DMA2ACHF         DMA2SCNTF         C2LF         INT1F         141           PIR4         CLC1IF         CWG1IF         TMR3GF         TMR3F         U2LF         UZCIF         UZCIF         UZCIF         IXTR3F         U2C2IF         IXTR3F         IZC2F         TMR4F         144           PIR6         TMR3GF         TMR3F         TMR3F         CC23F         CWG3F         CCP3IF         TMR4F         145           PIR7	PIE9	_	-	-	—	CLC3IE	CWG3IE	CCP3IE	TMR6IE	155
PIRO         IOCIF         CRCIF         SCANIF         NVMIF         CSWIF         OSFIF         HLVDIF         SWIF         137           PIR1         SMT1PWAIF         SMT1PRAIF         SMT1IF         C1IF         ADTF         ADIF         ZCIR         INTOIF         138           PIR2         IZCIRXIF         SPI1IF         SPI1IF         SPI1IF         SPI1IF         SPI1IF         DMAISCITF         DMAISCITF         DMAISCITF         139           PIR3         TMR0IF         UUIF         UITXIF         DMAISCITF         DMAISCITF         DMAISCITF         140           PIR4         CLCIFF         CWGIFF         NCOIFF         CCP1IF         TMR3IGF         TMR1IF         141           PIR5         12C2TXF         12C2RXF         DMA2AIF         DMA2ORIF         DMA2COTFF         DMA2SCITF         C2IF         INT1IF         142           PIR6         TMR3GIF         TMR3F         U2IF         U2EIF         U2TXIF         U2RXIF         12C2IFF         TMR1IF         144           PIR6         TMR3GIF         TMR3F         C12IF         CCP3IF         TMR6IF         145           PIR6         TMR3GIF         TMR3F         C12IF         CCC3IF         CC	PIE10	_	_	-	—	-	-	CLC4IE	CCP4IE	156
PIR1         SMT1PWAIF         SMT1IPRAIF         SMT1IF         C1IF         ADIF         ADIF         ZCDIF         INTOIF         138           PIR2         I2C1RXIF         SP11IF         SP11TXIF         SP11XIF         DMA1AIF         DMA1ORIF         DMA1DCNTIF         DMA1SCNTF         139           PIR3         TMR0IF         U1F         U1EF         U1TXIF         URXIF         I2C1EF         I2C1F         I2C1F         I2C1F         I2C1F         IANT1F         141           PIR4         CLC1IF         CWG1IF         NC0IF         —         CCP1IF         TMR1F         IATT1F         142           PIR5         I2C2TXF         I2C2RXF         DMA2AIF         DMA2ORIF         DMA2SCNTF         U2Z1F         IXT1F         142           PIR6         TMR3GIF         TMR3IF         U2IF         U2Z1F         U2RXIF         U2C2EIF         TMR4IF         144           PIR6         TMR5GIF         TMR3IF         TMR1F         U2IF         CLC3IF         CWG3IF         CCP3IF         TMR4IF         144           PIR7         —         —         —         —         —         —         145           PIR8         TMR5GIF         TMR5IF         <	PIR0	IOCIF	CRCIF	SCANIF	NVMIF	CSWIF	OSFIF	HLVDIF	SWIF	137
PIR2         IZC1RXIF         SPI1T         SPI1TXIF         SPI1TXIF         DMA1AIF         DMA1ORIF         DMA1DCNTIF         DMA1SCNTIF         139           PIR3         TMR0IF         U1IF         U1EIF         U1TXIF         U1RXIF         I2C1EIF         I2C1IF         I2C1TXIF         140           PIR4         CLC1IF         CWG1IF         NC01F         —         CCP1F         TMR2IF         TMR3IF         TMR1F         141           PIR6         TMR3GIF         TMR3IF         U2EF         DMA2CIFF         DMA2SCNTF         C2IF         INT1F         142           PIR6         TMR3GIF         TMR3IF         U2E         U2EIF         U2RXIF         U2RXIF         IZC2IF         TMR4F         144           PIR7         —         —         INT2F         CLC2IF         CWG3IF         CCP3IF         TMR4F         144           PIR8         TMR5GIF         TMR5IF         —         —         —         CCP3IF         TMR6F         145           PIR9         —         —         —         —         CLC3IF         CWG3IF         CCP3IF         TMR6F         145           PIR10         —         CCIP         SCANP         NVMIP	PIR1	SMT1PWAIF	SMT1PRAIF	SMT1IF	C1IF	ADTIF	ADIF	ZCDIF	INT0IF	138
PIR3       TMR0IF       U1IF       U1EIF       U1TXIF       U1RXIF       I2C1EIF       I2C1IF       I2C1TXIF       140         PIR4       CLC1IF       CWG1IF       NCO1IF       —       CCP1IF       TMR2IF       TMR1GIF       TMR1IF       141         PIR5       I2C2TXF       I2C2RXF       DMA2AF       DMA2ORIF       DMA2SCNTIF       C2F       INT1GF       142         PIR6       TMR3GIF       TMR3IF       U2IF       U2EIF       U2TXIF       U2RXIF       I2C2EF       I2C2IF       143         PIR7       —       —       ITMR3GIF       TMR3IF       —       —       —       —       —       145         PIR8       TMRSGIF       TMRSIF       —       —       —       —       —       145         PIR9       —       —       —       —       —       —       —       145         PIR10       —       —       —       —       CLC3IF       CWG3IF       CCP3IF       TMR6IF       145         PIR10       IOCIP       CRCIP       SCANIP       NVMIP       CSWIP       OSFIP       HLVDIP       SWIP       157         IPR1       SMT1PRAIP       SMT1PRAIP       S	PIR2	I2C1RXIF	SPI1IF	SPI1TXIF	SPI1RXIF	DMA1AIF	DMA10RIF	DMA1DCNTIF	DMA1SCNTIF	139
PIR4         CLC1IF         CWG1IF         NC01IF         T         CCP1IF         TMR2IF         TMR1GIF         TMR1IF         141           PIR5         I2C2TXF         I2C2RXF         DMA2AIF         DMA2ORIF         DMA2CNTIF         DMA2SCNTIF         C2IF         INT1IF         142           PIR6         TMR3GIF         TMR3IF         U2IF         U2TXIF         U2RXIF         I2C2EIF         I2C2IF         143           PIR7         -         -         -         CCP2IF         TMR4IF         144           PIR8         TMR5GIF         TMR5IF         -         -         -         -         -         -         145           PIR9         -         -         -         -         -         -         -         145           PIR9         -         -         -         -         -         -         -         145           PIR10         -         -         -         -         -         CLC3IF         CWG3IF         CC4IF         146           IPR0         IOCIP         CRCIP         SCANIP         NVMIP         CSWIP         OSFIP         HLVDIP         SWIP         157           IPR1 <td< td=""><td>PIR3</td><td>TMR0IF</td><td>U1IF</td><td>U1EIF</td><td>U1TXIF</td><td>U1RXIF</td><td>I2C1EIF</td><td>I2C1IF</td><td>I2C1TXIF</td><td>140</td></td<>	PIR3	TMR0IF	U1IF	U1EIF	U1TXIF	U1RXIF	I2C1EIF	I2C1IF	I2C1TXIF	140
PIRSI2C2TXFI2C2RXFDMA2AIFDMA2ORIFDMA2DCNTIFDMA2DCNTIFDMA2SCNTIFC2IFINT1IF142PIR6TMR3GIFTMR3IFU2IFU2EIFU2TXIFU2RXIFI2C2EIFI2C2IF143PIR7———INT2IFCLC2IFCWG2IF—CCP2IFTMR4IF144PIR8TMR5GIFTMR5IF——————145PIR9————————145PIR10————————145PIR10IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PMAPSMT1PANIPSMT1IPC1IPADIPADIPZCDIPINA1SCNTIP158IPR2I2C1RPSPI1IPSPI1IPSPI1RIPDMA1AIPDMA1ORIPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG3IPNCO1IP—CCP1IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2XPDMA2AIPDMA2ORIPDMA2SCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR6TMR3GIPTMR3IPO——————— <td< td=""><td>PIR4</td><td>CLC1IF</td><td>CWG1IF</td><td>NCO1IF</td><td>—</td><td>CCP1IF</td><td>TMR2IF</td><td>TMR1GIF</td><td>TMR1IF</td><td>141</td></td<>	PIR4	CLC1IF	CWG1IF	NCO1IF	—	CCP1IF	TMR2IF	TMR1GIF	TMR1IF	141
PIR6         TMR3GIF         TMR3IF         U2IF         U2EIF         U2TXIF         U2CXIF         I2C2EIF         I2C2IF         143           PIR7         —         —         INT2IF         CLC2IF         CWG2IF         —         CCP2IF         TMR4IF         144           PIR8         TMR5GIF         TMR5IF         —         —         —         —         CCP2IF         TMR4IF         144           PIR8         TMR5GIF         TMR5IF         —         —         —         —         —         —         145           PIR9         —         —         —         —         —         —         —         —         145           PIR0         —         —         —         —         —         —         —         145           PIR0         —         —         —         —         —         —         CLC3IF         CM31F         CCP3IF         TMR6IF         145           PIR10         —         CRCIP         SCANIP         NVMIP         CSWIP         OSFIP         HLVDIP         SWIP         157           IPR1         SMT1PWAIP         SMT1P         SMT1P         MIP         IMA10P         IMA10CN	PIR5	I2C2TXF	I2C2RXF	DMA2AIF	DMA2ORIF	DMA2DCNTIF	DMA2SCNTIF	C2IF	INT1IF	142
PIR7         —         INT2IF         CLC2IF         CWG2IF         —         CCP2IF         TMR4IF         144           PIR8         TMR5GIF         TMR5IF         —         —         —         —         —         —         145           PIR9         —         —         —         —         —         —         —         145           PIR9         —         —         —         —         —         —         —         145           PIR0         —         —         —         —         —         —         —         —         145           PIR0         —         —         —         —         —         —         —         —         145           PIR10         —         —         —         —         —         CLC3IF         CWG3IF         CCP3IF         TMR6IF         145           IPR0         IOCIP         CRCIP         SCANIP         NVMIP         CSWIP         OSFIP         HLVDIP         SWIP         157           IPR1         SMTPWAIP         SMT1PAIP         SMT1PAIP         SMT1PAIP         DMA1AIP         DMA1DCNIP         DMA1SCNTP         DMA1SCNTP         IDA1SCNTP	PIR6	TMR3GIF	TMR3IF	U2IF	U2EIF	U2TXIF	U2RXIF	I2C2EIF	I2C2IF	143
PIR8TMR5GIFTMR5IF——————145PIR9————CLC3IFCWG3IFCCP3IFTMR6IF145PIR10—————CLC3IFCWG3IFCCP3IFTMR6IF145PIR10———————CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PRAIPSMT1IPC1IPADTPADIPZCDIPINT0IP158IPR2I2C1RIPSP11IPSP11TIPSP11RIPDMA1AIPDMA1ORIPDMA10CNTIPDMA1SCNTIP159IPR3TMR0IPU11PU1EIPU1TXIPU1RXIPI2C1EIP12C1IP12C1TXIP160IPR4CLC1IPCWG1IPNCO1IP—CCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2ORTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7——————————164IPR8TMR5GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIP12C1P164IPR8TMR5GIPTMS1P———————16	PIR7	-	-	INT2IF	CLC2IF	CWG2IF	—	CCP2IF	TMR4IF	144
PIR9CLC3IFCWG3IFCCP3IFTMR6IF145PIR10CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PAIPSM11PC1IPADTIPADIPZCDIPINT0IP158IPR212C1RIPSP11IPSP11TIPSP11RIPDMA1AIPDMA1ORIPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIP12C1EIP12C1IP12C1TXIP160IPR4CLC1PCWG1IPNC01IP-CCP1IPTMR2IPTMR1GIPTMR1IP161IPR512C2TXP12C2RXPDMA2AIPDMA2ORIPDMA2DCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIP12C2EIP12C2IP163IPR7164IPR8TMR5GIPTMR5IP164IPR9165IPR10166NTBASEU166NTBASEU166NTBASEL167NTBASEL-<	PIR8	TMR5GIF	TMR5IF	-	—	-	—	—	—	145
PIR10CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PAIPSMT1PC1IPADTIPADIPZCDIPINTOIP158IPR2I2C1RIPSP11IPSP11IPSP1RIPDMA1AIPDMA1ORIPDMA1DCNTPDMA1SCNTP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG1IPNCO1IPCCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2DCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7164IPR8TMR5GIPTMR3IP164IPR8TMR5GIPTMR5IP165IPR10166IVTBASEU166IVTBASEL167IVTADU167IVTADL167IVTADL167IVTADL<	PIR9	-	-	-	—	CLC3IF	CWG3IF	CCP3IF	TMR6IF	145
IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PRAIPSMT1PC1IPADTIPADIPZCDIPINTOIP158IPR2I2C1RIPSPI1IPSPI1TIPSPI1RIPDMA1AIPDMA1ORPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG1IPNCO1P—CCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2ORIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7IMTSIPCLC2IPCWG2IP-CCP3IPTMR4IP164IPR8TMRSGIPTMRSIP164IPR8TMRSGIPTMRSIP166IPR10166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IFR8TMRSGIP	PIR10	_	-	-	—	-	—	CLC4IF	CCP4IF	146
IPR1         SMT1PWAIP         SMT1PRAIP         SMT1IP         C1IP         ADTIP         ADIP         ZCDIP         INTOIP         158           IPR2         I2C1RIP         SPI1IP         SPI1TIP         SPI1RIP         DMA1AIP         DMA1ORIP         DMA1DCNTIP         DMA1SCNTIP         159           IPR3         TMR0IP         U1IP         U1EIP         U1TXIP         U1RXIP         I2C1EIP         I2C1IP         I2C1TXIP         160           IPR4         CLC1IP         CWG1IP         NC01IP         —         CCCP1IP         TMR2IP         TMR1GIP         TMR1IP         161           IPR4         CLC1IP         CWG1IP         NC01IP         —         CCCP1IP         TMR2IP         TMR1GIP         TMR1IP         161           IPR5         I2C2TXP         I2C2RXP         DMA2AIP         DMA2ORIP         DMA2CNTIP         DMA2SCNTIP         C2IP         INT1IP         162           IPR6         TMR3GIP         TMR3IP         U2IP         U2EIP         U2TXIP         U2RXIP         I2C2EIP         I2C2IP         163           IPR6         TMR5GIP         TMR3IP         —         —         —         CC2G3IP         TMR4IP         164           IPR9	IPR0	IOCIP	CRCIP	SCANIP	NVMIP	CSWIP	OSFIP	HLVDIP	SWIP	157
IPR2         I2C1RIP         SPI1IP         SPI1RIP         DMA1AIP         DMA1ORIP         DMA1DCNTP         DMA1SCNTIP         159           IPR3         TMR0IP         U1IP         U1EIP         U1TXIP         U1RXIP         I2C1EIP         I2C1IP         I2C1TXIP         160           IPR4         CLC1IP         CWG1IP         NCO1IP         —         CCP1IP         TMR2IP         TMR1GIP         TMR1IP         161           IPR4         I2C2TXP         I2C2RXP         DMA2AIP         DMA2ORIP         DMA2DCNTIP         DM2SCNTIP         C2IP         INT1IP         162           IPR6         TMR3GIP         TMR3IP         U2IP         U2EIP         U2TXIP         U2RXIP         I2C2EIP         I2C2IP         163           IPR7         —         —         INT2IP         CLC2IP         CWG2IP         —         CCP2IP         TMR4IP         164           IPR8         TMR5GIP         TMR5IP         —         —         —         —         —         164           IPR9         —         —         —         —         CC3IP         CWG3IP         CCP3IP         TMR6IP         165           IPR10         —         —         —         —<	IPR1	SMT1PWAIP	SMT1PRAIP	SMT1IP	C1IP	ADTIP	ADIP	ZCDIP	INT0IP	158
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR2	I2C1RIP	SPI1IP	SPI1TIP	SPI1RIP	DMA1AIP	DMA10RIP	DMA1DCNTIP	DMA1SCNTIP	159
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	IPR3	TMR0IP	U1IP	U1EIP	U1TXIP	U1RXIP	I2C1EIP	I2C1IP	I2C1TXIP	160
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR4	CLC1IP	CWG1IP	NCO1IP	—	CCP1IP	TMR2IP	TMR1GIP	TMR1IP	161
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR5	I2C2TXP	I2C2RXP	DMA2AIP	DMA2ORIP	DMA2DCNTIP	DMA2SCNTIP	C2IP	INT1IP	162
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR6	TMR3GIP	TMR3IP	U2IP	U2EIP	U2TXIP	U2RXIP	I2C2EIP	I2C2IP	163
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR7	-	-	INT2IP	CLC2IP	CWG2IP	—	CCP2IP	TMR4IP	164
IPR9         -         -         -         CLC3IP         CWG3IP         CCP3IP         TMR6IP         165           IPR10         -         -         -         -         -         CLC3IP         CCP3IP         TMR6IP         165           IPR10         -         -         -         -         -         CLC4IP         CCP4IP         165           IVTBASEU         -         -         -         -         BASE<20:16>         166           IVTBASEL         -         -         BASE<15:8>         166         165           IVTBASEL         -         -         BASE<7:0>         166         167           IVTADU         Image: Comparison of the c	IPR8	TMR5GIP	TMR5IP	-	—	-	—	—	—	164
IPR10     -     -     -     -     CCP4IP     165       IVTBASEU     -     -     -     -     -     166       IVTBASEH     -     -     -     BASE<15:8>     166       IVTBASEL     BASE<15:8>     166       IVTBASEL     BASE<7:0>     166       IVTADU     Image: Comparison of the temperature of temper	IPR9	-	-	-	—	CLC3IP	CWG3IP	CCP3IP	TMR6IP	165
IVTBASEU         —         —         —         BASE         BASE         166           IVTBASEH         BASE<15:8>         166         166           IVTBASEL         BASE<7:0>         166           IVTADU         Image: Comparison of the system of the sys	IPR10	_	_	_	-	_	-	CLC4IP	CCP4IP	165
IVTBASEH         BASE<15:8>         166           IVTBASEL         BASE<7:0>         166           IVTADU         AD         167           IVTADH         AD<15:8>         167           IVTADL         AD<7:0>         167	IVTBASEU	_	_	-			BASE<20:16>			166
IVTBASEL         BASE<7:0>         166           IVTADU         AD         AD         167           IVTADH         AD         AD         167           IVTADL         AD         AD<7:0>         167	IVTBASEH	BASE<15:8>							166	
IVTADU         AD         AD         167           IVTADH         AD<15:8>         167           IVTADL         AD<7:0>         167	IVTBASEL	BASE<7:0>						166		
IVTADH         AD<15:8>         167           IVTADL         AD<7:0>         167	IVTADU	AD<20:16>							167	
IVTADL AD<7:0> 167	IVTADH				AD	<15:8>				167
	IVTADL				AE	)<7:0>				167
IVTLOCK — — — — — — — IVTLOCKED 168	IVTLOCK	—	—	—	—	_	—	—	IVTLOCKED	168

TABLE 9-3:	SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

**Legend:** — = unimplemented locations, read as '0'. Shaded bits are not used for interrupts.

#### FIGURE 15-3: DMA COUNTERS BLOCK DIAGRAM



Table 15-2 has a few examples of configuring DMAMessage sizes.

TABLE 15-2:	EXAMPLE	E MESSAGE SIZE	TABLE	
Operat	ion	Framplo	SCNT	DONT

Operation	Example	SCNT	DCNT	Comments
Read from single SFR location to RAM	U1RXB	1	Ν	N equals the number of bytes desired in the destination buffer. N >= 1.
Write to single SFR location from RAM	U1TXB	Ν	1	N equals the number of bytes desired in the source buffer. N >= 1.
	ADRES[H:L]	2	2*N	N equals the number of ADC results to be stored in memory. N>= 1
Read from multiple SFR location	TMR1[H:L]	2	2*N	N equals the number of TMR1 Acquisition results to be stored in memory. N>= 1
	SMT1CPR[U:H:L]	3	3*N	N equals the number of Capture Pulse Width measurements to be stored in memory. N>= 1
Write to Multiple SFR regis- ters	PWMDC[H:L]	2*N	2	N equals the number of PWM duty cycle val- ues to be loaded from a memory table. N>= 1
	All ADC registers	N*31	31	Using the DMA to transfer a complete ADC context from RAM to the ADC registers.N>= 1

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	U-0		
CWG3MD	CWG2MD	CWG1MD	_	_	_	_	—		
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable I	bit	U = Unimplem	nented bit, read	l as '0'			
u = Bit is uncl	nanged	x = Bit is unkn	iown	-n/n = Value at POR and BOR/Value at all other Re					
'1' = Bit is set		'0' = Bit is clea	ared	q = Value depends on condition					
bit 7	CWG3MD: Di	isable CWG3 N	lodule bit						
	1 = CWG3 m	odule disabled							
	0 = CWG3 m	iodule enabled							
bit 6 <b>CWG2MD</b> : Disable CWG2 Module bit			lodule bit						
	0 = CWG2 m	odule enabled							
bit 5	CWG1MD: Di	isable CWG1 M	lodule bit						
	1 = CWG1 m	odule disabled							
	0 = CWG1 m	odule enabled							
bit 4-0	Unimplemen	ted: Read as 'o	)'						

#### REGISTER 19-5: PMD4: PMD CONTROL REGISTER 4



FIGURE 2

PIC18(L)F26/27/45/46/47/55/56/57K42

### 25.8 Register Definitions: SMT Control

Long bit name prefixes for the Signal Measurement Timer peripherals are shown in **Section 1.3 "Register and Bit naming conventions"**.

## TABLE 25-2:LONG BIT NAMES PREFIXESFOR SMT PERIPHERALS

Peripheral	Bit Name Prefix		
SMT1	SMT1		

#### REGISTER 25-1: SMT1CON0: SMT CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
EN <sup>(1)</sup>	—	STP	WPOL	SPOL	CPOL	PS<1:0>		
bit 7							bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	<ul> <li>EN: SMT Enable bit<sup>(1)</sup></li> <li>1 = SMT is enabled</li> <li>0 = SMT is disabled; internal states are reset, clock requests are disabled</li> </ul>
bit 6	Unimplemented: Read as '0'
bit 5	<pre>STP: SMT Counter Halt Enable bit When SMT1TMR = SMT1PR: 1 = Counter remains SMT1PR; period match interrupt occurs when clocked 0 = Counter resets to 24'h000000; period match interrupt occurs when clocked</pre>
bit 4	<pre>WPOL: SMT1WIN Input Polarity Control bit 1 = SMT1WIN signal is active-low/falling edge enabled 0 = SMT1WIN signal is active-high/rising edge enabled</pre>
bit 3	SPOL: SMT1SIG Input Polarity Control bit 1 = SMT1_signal is active-low/falling edge enabled 0 = SMT1_signal is active-high/rising edge enabled
bit 2	<b>CPOL:</b> SMT Clock Input Polarity Control bit 1 = SMT1TMR increments on the falling edge of the selected clock signal 0 = SMT1TMR increments on the rising edge of the selected clock signal
bit 1-0	PS<1:0>: SMT Prescale Select bits 11 = Prescaler = 1:8 10 = Prescaler = 1:4 01 = Prescaler = 1:2 00 = Prescaler = 1:1

#### **Note 1:** Setting EN to '0' does not affect the register contents.

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BO	R/Value at all c	ther Resets
'1' = Bit is set		'0' = Bit is cle	ared				
bit 7	G3D4T: Gate	2 Data 4 True	(noninverted)	bit			
	1 = CLCIN3	(true) is gated i	nto CLCx Gal	te 2			
<b>h</b> # 0		(true) is not ga	ted into CLCX				
DIT 6		e 2 Data 4 Nega	ated (inverted				
	1 = CLCIN3 0 = CLCIN3	(inverted) is ga	t gated into CLCX	I Cx Gate 2			
bit 5	G3D3T: Gate	2 Data 3 True	(noninverted)	bit			
	1 = CLCIN2	(true) is gated i	nto CLCx Gat	te 2			
	0 = CLCIN2	(true) is not ga	ted into CLCx	Gate 2			
bit 4	G3D3N: Gate	e 2 Data 3 Neg	ated (inverted	) bit			
	1 = CLCIN2	(inverted) is ga	ted into CLCx	Gate 2			
	0 = CLCIN2	(inverted) is no	t gated into C	LCx Gate 2			
bit 3	G3D2T: Gate	2 Data 2 True	(noninverted)	bit			
	1 = CLCIN1	(true) is gated i	Into CLCX Gat	te 2 Gate 2			
hit 2	G3D2N: Gate	(ilue) is not ga	ated (inverted	) bit			
	1 = CLCIN1	(inverted) is a	ted into CI Cx	Gate 2			
	0 = CLCIN1	(inverted) is no	t gated into C	LCx Gate 2			
bit 1	G3D1T: Gate	2 Data 1 True	(noninverted)	bit			
	1 = CLCIN0	(true) is gated i	into CLCx Gat	te 2			
	0 = CLCIN0	(true) is not ga	ted into CLCx	Gate 2			
bit 0	G3D1N: Gate	e 2 Data 1 Nega	ated (inverted	) bit			
	1 = CLCINO	(inverted) is ga	ted into CLCx	Gate 2			
	0 = CLCINO	(invertea) is no	t gated into C	LUX Gate 2			

#### REGISTER 27-9: CLCxGLS2: GATE 2 LOGIC SELECT REGISTER

### 28.1 NCO Operation

The NCO operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCO output (NCO\_overflow). This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See Equation 28-1.

The NCO output can be further modified by stretching the pulse or toggling a flip-flop. The modified NCO output is then distributed internally to other peripherals and can be optionally output to a pin. The accumulator overflow also generates an interrupt (NCO\_overflow).

The NCO period changes in discrete steps to create an average frequency. This output depends on the ability of the receiving circuit (i.e., CWG or external resonant converter circuitry) to average the NCO output to reduce uncertainty.

#### EQUATION 28-1: NCO OVERFLOW FREQUENCY

 $FOVERFLOW = \frac{NCO \ Clock \ Frequency \times Increment \ Value}{2^{20}}$ 

## 28.1.1 NCO CLOCK SOURCES

Clock sources available to the NCO include:

- Fosc
- HFINTOSC
- LFINTOSC
- MFINTOSC/4 (32 kHz)
- MFINTOSC (500 kHz)
- CLC1/2/3/4\_out
- CLKREF
- SOSC

The NCO clock source is selected by configuring the N1CKS<2:0> bits in the NCO1CLK register.

#### 28.1.2 ACCUMULATOR

The accumulator is a 20-bit register. Read and write access to the accumulator is available through three registers:

- NCO1ACCL
- NCO1ACCH
- NCO1ACCU

#### 28.1.3 ADDER

The NCO Adder is a full adder, which operates independently from the source clock. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

#### 28.1.4 INCREMENT REGISTERS

The increment value is stored in three registers making up a 20-bit incrementer. In order of LSB to MSB they are:

- NCO1INCL
- NCO1INCH
- NCO1INCU

When the NCO module is enabled, the NCO1INCU and NCO1INCH registers should be written first, then the NCO1INCL register. Writing to the NCO1INCL register initiates the increment buffer registers to be loaded simultaneously on the second rising edge of the NCO\_clk signal.

The registers are readable and writable. The increment registers are double-buffered to allow value changes to be made without first disabling the NCO module.

When the NCO module is disabled, the increment buffers are loaded immediately after a write to the increment registers.

**Note:** The increment buffer registers are not user-accessible.

#### 32.8.3.4 Receiver Overflow and Transmitter Underflow Interrupts

The receiver overflow interrupt triggers if data is received when the RXFIFO is already full and RXR = 1. In this case, the data will be discarded and the RXOIF bit will be set. The receiver overflow interrupt flag is the RXOIF bit of SPIxINTF. The receiver overflow interrupt enable bit is the RXOIE bit of SPIxINTE.

The Transmitter Underflow interrupt flag triggers if a data transfer begins when the TXFIFO is empty and TXR = 1. In this case, the most recently received data will be transmitted and the TXUIF bit will be set. The transmitter underflow interrupt flag is the TXUIF bit of SPIxINTF. The transmitter underflow interrupt enable bit is the TXUIE bit of SPIxINTE.

Both of these interrupts will only occur in Slave mode, as Master mode will not allow the RXFIFO to overflow or the TXFIFO to underflow.

#### **REGISTER 32-4:** SPIXTCNTH: SPI TRANSFER COUNTER MSB REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	_	TCNT10	TCNT9	TCNT8
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'

#### bit 7-3 Unimplemented: Read as '0'

bit 2-0	TCNT<10:8>:
	BMODE = 0
	Bits 13-11 of the Transfer Counter, counting the total number of bits to transfer
	BMODE = 1
	Bits 10-8 of the Transfer Counter, counting the total number of bytes to transfer
Notor	This register should not be written to while a transfer is in progress (PLISY hit of SPIVCON2 is

Note: This register should not be written to while a transfer is in progress (BUSY bit of SPIxCON2 is set).

#### REGISTER 32-5: SPIxTWIDTH: SPI TRANSFER WIDTH REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	TWIDTH2	TWIDTH1	TWIDTH0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'

- bit 7-3 Unimplemented: Read as '0'
- bit 2-0 TWIDTH<2:0>:

BMODE = 0

Bits 2-0 of the Transfer Counter, counting the total number of bits to transfer

BMODE = 1

Size (in bits) of each transfer counted by the transfer counter

- 111 **= 7 bits**
- 110 **= 6 bits**
- 101 **= 5 bits**
- 100 **= 4 bits**
- 011 = 3 bits
- 010 = 2 bits
- 001 **= 1 bit**
- 000 **= 8 bits**

Note: This register should not be written to while a transfer is in progress (BUSY bit of SPIxCON2 is set).

#### FIGURE 33-18: STOP CONDITION DURING RECEIVE OR TRANSMIT



#### 33.5.9 MASTER TRANSMISSION IN 7-BIT ADDRESSING MODE

This section describes the sequence of events for the  $I^2C$  module configured as an  $I^2C$  master in 7-bit Addressing mode and is transmitting data. Figure 33-19 is used as a visual reference for this description.

#### 1. If ABD = 0; i.e., Address buffers are enabled

Master software loads number of bytes to be transmitted in one sequence in I2CxCNT, slave address in I2CxADB1 with R/W = 0 and the first byte of data in I2CxTXB. Master software has to set the Start (S) bit to initiate communication.

If ABD = 1; i.e., Address buffers are disabled

Master software loads the number of bytes to be transmitted in one sequence in I2CxCNT and the slave address with R/W = 0 into the I2CxTXB register. Writing to the I2CxTXB will assert the start condition on the bus and sets the S bit. Software writes to the S bit are ignored in this case.

- 2. Master hardware waits for BFRE bit to be set; then shifts out start and address.
- If the transmit buffer is empty (i.e., TXBE = 1) and I2CxCNT!= 0, the I2CxTXIF and MDR bits are set and the clock is stretched on the 8th falling SCL edge. Clock can be started by loading the next data byte in I2CxTXB register.
- 4. Master sends out the 9th SCL pulse for ACK.
- If the Master hardware receives ACK from Slave device, it loads the next byte from the transmit buffer (I2CxTXB) into the shift register and the

value of I2CxCNT register is decremented.

- 6. If a NACK was received, Master hardware asserts Stop or Restart
- 7. If ABD = 0; i.e., Address buffers are enabled

If I2CxCNT = 0, Master hardware sends Stop or sets MDR if RSEN = 1 and waits for the software to set the Start bit again to issue a restart condition.

If ABD = 1; i.e., Address buffers are disabled

If I2CxCNT = 0, Master hardware sends Stop or sets MDR if RSEN = 1 and waits for the software to write the new address to the I2CxTXB register. Software writes to the S bit are ignored in this case.

- 8. Master hardware outputs data on SDA.
- 9. If TXBE = 1 and I2CxCNT! = 0, I2CxTXIF and MDR bits are set and the clock is stretched on 8th falling SCL edge. The user can release the clock by writing the next data byte to I2CxTXB register.
- 10. Master hardware clocks in ACK from Slave, and loads the next data byte from I2CTXB to the shift register. The value of I2CxCNT is decremented.
- 11. Go to step 7.



### FIGURE 33-22: I<sup>2</sup>C MASTER, 10-BIT ADDRESS, RECEPTION (USING RSTEN BIT)

© 2016-2017 Microchip Technology Inc

RETURN Return from Subroutine										
Synta	ax:	RETURN	{s}							
Oper	ands:	s ∈ [0,1]								
Oper	ation:	$(TOS) \rightarrow P0$ if s = 1 $(WS) \rightarrow W$ , (STATUSS) $(BSRS) \rightarrow 1$ PCLATU, P	$(TOS) \rightarrow PC,$ if s = 1 $(WS) \rightarrow W,$ $(STATUSS) \rightarrow Status,$ $(BSRS) \rightarrow BSR,$ PCLATU, PCLATH are unchanged							
Statu	is Affected:	None								
Enco	oding:	0000	0000	0001	001s					
		is loaded into the program counter. If 's'= 1, the contents of the shadow registers, WS, STATUSS and BSRS, are loaded into their corresponding registers, W, Status and BSR. If 's' = 0, no update of these registers								
Word	ls:	1								
Cycle	es:	2								
QC	ycle Activity:									
	Q1	Q2	Q3		Q4					
	Decode	No operation	Proce Data	ess a f	POP PC rom stack					
	No	No	No		No					
	operation	operation	operat	tion	operation					
_										
Exan	nple:	RETURN								
	After Instruction	on:								

PC = TOS

RLC	F Rotate Left f through Carry								
Synta	ax:	RLCF	f {,d {,a}}						
Oper	ands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]	5						
Oper	ation:	dest <n +="" 1=""> C, st&lt;0&gt;</n>	,						
Statu	is Affected:	C, N, Z							
Enco	oding:	0011	01da	ffff	ffff				
Desc	ription:	The conte one bit to flag. If 'd' is in register If 'a' is '0', selected. I select the If 'a' is '0' set is enal operates i Addressin $f \le 95$ (5FI 41.2.3 "By ented Ins: Offset Mo	The contents of register 'f' are rotated one bit to the left through the CARRY flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 41.2.3 "Byte-Oriented and Bit-Ori- ented Instructions in Indexed Literal Offset Mode" for details.						
Word	ls:	1							
Cycle	es:	1							
QC	ycle Activity:								
	Q1	Q2	Q3		Q4				
	Decode	Read register 'f'	Process Data	s de	Write to estination				
<u>Exar</u>	nple:	RLCF	RLCF REG, 0, 0						
	Before Instruct REG C After Instructio REG W C	tion = 1110 = 0 on = 1110 = 1100 = 1	0110 0110 1100						

MOV	/SS	Move Ind	Move Indexed to Indexed								
Synta	ax:	MOVSS [	MOVSS [z <sub>s</sub> ], [z <sub>d</sub> ]								
Oper	ands:	$0 \le z_s \le 12$ $0 \le z_d \le 12$	7 7								
Oper	ation:	((FSR2) + 2	$z_s) \rightarrow ((F)$	SR2) + z	: <sub>d</sub> )						
Statu	s Affected:	None									
Enco 1st w 2nd v	ding: ord (source) vord (dest.)	1110 1111	1011 xxxx	1zzz xzzz	zzzz <sub>s</sub> zzzz <sub>d</sub>						
Desc	ription	The conter moved to ti addresses registers a 7-bit literal respectivel registers ca the 4096-b (000h to FI The MOVSS PCL, TOSU destination If the result an indirect value retur resultant di an indirect instruction	$\begin{array}{ c c c c c } \hline 1111 & xxxx & xzzz & zzz_d \\ \hline \hline 1111 & xxxx & xzzz & zzz_d \\ \hline \hline 1111 & xxxx & xzzz & zzz_d \\ \hline \hline 1111 & xxxx & xzzz & zzz_d \\ \hline \hline 1111 & xxxx & xzzz & zzz_d \\ \hline 1111 & xxxx & xzzz & zzzz_d \\ \hline 1111 & xxxx & xzzz & zzzz_d \\ \hline 1111 & xxxx & xzzz & zzzz_d \\ \hline 1111 & xxxx & xzzz & zzz_d \\ \hline 1111 & xxxx & xzzz & zzz_d \\ \hline 1111 & xxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & xzzz & zzzz_d \\ \hline 1111 & xxxxx & zzz & zzzz_d \\ \hline 1111 & xxxxx & zzz & zzzz_d \\ \hline 1111 & xxxxxx & zzzz & zzzzz & zzzz & zzzz$								
Word	S:	2									
Cycle	es:	2									
QC	ycle Activity:										
	Q1	Q2	Q3		Q4						
	Decode	Determine	Detern	nine	Read						
		source addr	source	addr s	ource reg						
	Decode	Determine dest addr	Detern dest a	nine ddr te	Write o dest reg						

Example:	MOVSS	[05h],	[06h]
Before Instructio FSR2 Contents	on =	80h	
of 85h	=	33h	
of 86h	=	11h	
After Instruction FSR2 Contents	=	80h	
of 85h	=	33h	
of 86h	=	33h	

PUS	HL	S	tore Liter	al a	t FSR	2, Decr	em	nent FSR2
Synta	ax:	Ы	JSHL k					
Opera	ands:	0	≤ k ≤ 255					
Oper	ation:	k FS	→ (FSR2) SR2 – 1 –	, → FS	R2			
Statu	s Affected:	N	one					
Enco	ding:		1111	10	010	kkkk		kkkk
Description.			emory add decremer his instruc hto a softw	dres nted tion /are	s spec by 1 a allows stack.	cified by after the o susers to	FS ope o pi	R2. FSR2 eration. Jsh values
Word	s:	1						
Cycle	es:	1						
QC	ycle Activity	/:						
	Q1		Q2			Q3		Q4
	Decode		Read 'l	¢'	Pro c	ocess lata	d	Write to estination
<u>Exam</u>	<u>nple</u> :		PUSHL	081	ı			
Before Instr FSR2H Memo		ruct H:F ory (	ruction H:FSR2L vry (01ECh)		=	01ECh 00h		
	After Instru FSR2 Memo	ctio H:F ory (	n SR2L (01ECh)		= =	01EBh 08h		

### 42.0 REGISTER SUMMARY

#### **TABLE 42-1**: REGISTER FILE SUMMARY FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
3FFFh	TOSU	_	_	_		Top	o of Stack Uppe	r byte	•	37
3FFEh	TOSH		Top of Stack High byte							
3FFDh	TOSL		Top of Stack Low byte							
3FFCh	STKPTR	_		_			Stack Pointe	r		39
3FFBh	PCLATU	_	_	_		Holding	Register for PC	Upper byte		36
3FFAh	PCLATH			Но	lding Register	for PC High b	yte			36
3FF9h	PCL				PC Lo	w byte				36
3FF8h	TBLPTRU	_	_		Progr	am Memory T	able Pointer Up	per byte		192
3FF7h	TBLPTRH			Progra	m Memory Ta	ble Pointer Hig	gh byte			192
3FF6h	TBLPTRL			Progra	am Memory Ta	ble Pointer Lo	w byte			192
3FF5h	TABLAT				Table	Latch				192
3FF4h	PRODH				Product Regis	ster High byte				187
3FF3h	PRODL				Product Regi	ster Low byte				187
3FF2h	_				Unimple	emented				
3FF1h	PCON1	—	_	_	—	—	—	MEMV	_	91
3FF0h	PCON0	STKOVF	STKUNF	WDTWV	RWDT	RMCLR	RI	POR	BOR	90
3FEFh	INDF0	Uses contents	of FSR0 to addr	ress data mem	ory – value of	FSR0 not cha	nged			60
3FEEh	POSTINC0	Uses contents	of FSR0 to addr	ress data mem	ory – value of	FSR0 post-ind	cremented			61
3FEDh	POSTDEC0	Uses contents	of FSR0 to addr	ress data mem	ory – value of	FSR0 post-de	cremented			61
3FECh	PREINC0	Uses contents	of FSR0 to addr	ress data mem	ory – value of	FSR0 pre-inci	remented			61
3FEBh	PLUSW0	Uses contents	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented – value of FSR0 offset by W							
3FEAh	FSR0H	—	—		Indirec	t Data Memor	y Address Poin	ter 0 High		61
3FE9h	FSR0L			Indirect	Data Memory	Address Point	er 0 Low			61
3FE8h	WREG				Working	Register				
3FE7h	INDF1	Uses contents	of FSR1 to addr	ress data mem	ory – value of	FSR1 not cha	nged			61
3FE6h	POSTINC1	Uses contents	of FSR1 to addr	ress data mem	ory – value of	FSR1 post-ind	cremented			61
3FE5h	POSTDEC1	Uses contents	of FSR1 to addr	ress data mem	ory – value of	FSR1 post-de	cremented			61
3FE4h	PREINC1	Uses contents	of FSR1 to addr	ress data mem	ory – value of	FSR1 pre-inci	remented			61
3FE3h	PLUSW1	Uses contents	of FSR1 to addr	ress data mem	ory – value of	FSR1 pre-inci	remented – valu	ie of FSR1 off	set by W	61
3FE2h	FSR1H	—	—		Indirec	t Data Memor	y Address Poin	ter 1 High		61
3FE1h	FSR1L			Indirect	Data Memory	Address Point	er 1 Low			61
3FE0h	BSR	—	—			Bank Se	lect Register			44
3FDFh	INDF2	Uses contents	of FSR2 to addr	ress data mem	ory – value of	FSR2 not cha	nged			61
3FDEh	POSTINC2	Uses contents	of FSR2 to addr	ress data mem	ory – value of	FSR2 post-ind	cremented			61
3FDDh	POSTDEC2	Uses contents	of FSR2 to addr	ress data mem	ory – value of	FSR2 post-de	cremented			61
3FDCh	PREINC2	Uses contents	of FSR2 to addr	ress data mem	ory – value of	FSR2 pre-inci	remented			61
3FDBh	PLUSW2	Uses contents	of FSR2 to addr	ress data mem	ory – value of	FSR2 pre-inci	remented – valu	ie of FSR2 off	set by W	61
3FDAh	FSR2H	—	—		Indirec	t Data Memor	y Address Poin	ter 2 High		61
3FD9h	FSR2L			Indirect	Data Memory	Address Point	er 2 Low			61
3FD8h	STATUS	—	TO	PD	N	OV	Z	DC	С	58
3FD7h	IVTBASEU	—	—	—	BASE20	BASE19	BASE18	BASE17	BASE16	166
3FD6h	IVTBASEH	BASE15	BASE14	BASE13	BASE12	BASE11	BASE10	BASE9	BASE8	166
3FD5h	IVTBASEL	BASE7	BASE6	BASE5	BASE4	BASE3	BASE2	BASE1	BASE0	166
3FD4h	IVTLOCK	_	_	_		_	_	_	IVTLOCKED	168
3FD3h	INTCON1	ST	TAT		_		_	_	_	136
3FD2h	INTCON0	GIE	GIEL	IPEN	_	_	INT2EDG	INT1EDG	INT0EDG	135

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition Note

Unimplemented in LF devices. 1:

Unimplemented in PIC18(L)F26/27K42. 2:

3: Unimplemented on PIC18(L)F26/27/45/46/47K42 devices.

Unimplemented in PIC18(L)F45/55K42. 4:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
3A16h	RC6PPS	_	—	—	RC6PPS4	RC6PPS3	RC6PPS2	RC6PPS1	RC6PPS0	280
3A15h	RC5PPS		_	—	RC5PPS4	RC5PPS3	RC5PPS2	RC5PPS1	RC5PPS0	280
3A14h	RC4PPS	—	_	—	RC4PPS4	RC4PPS3	RC4PPS2	RC4PPS1	RC4PPS0	280
3A13h	RC3PPS	_	_	—	RC3PPS4	RC3PPS3	RC3PPS2	RC3PPS1	RC3PPS0	280
3A12h	RC2PPS	_	_	—	RC2PPS4	RC2PPS3	RC2PPS2	RC2PPS1	RC2PPS0	280
3A11h	RC1PPS	_	_	—	RC1PPS4	RC1PPS3	RC1PPS2	RC1PPS1	RC1PPS0	280
3A10h	RC0PPS	_	_	—	RC0PPS4	RC0PPS3	RC0PPS2	RC0PPS1	RC0PPS0	280
3A0Fh	RB7PPS	—	—	_	RB7PPS4	RB7PPS3	RB7PPS2	RB7PPS1	RB7PPS0	280
3A0Eh	RB6PPS	—	—	_	RB6PPS4	RB6PPS3	RB6PPS2	RB6PPS1	RB6PPS0	280
3A0Dh	RB5PPS	—	—	—	RB5PPS4	RB5PPS3	RB5PPS2	RB5PPS1	RB5PPS0	280
3A0Ch	RB4PPS	—	—	_	RB4PPS4	RB4PPS3	RB4PPS2	RB4PPS1	RB4PPS0	280
3A0Bh	RB3PPS	—	—	—	RB3PPS4	RB3PPS3	RB3PPS2	RB3PPS1	RB3PPS0	280
3A0Ah	RB2PPS	—	—	—	RB2PPS4	RB2PPS3	RB2PPS2	RB2PPS1	RB2PPS0	280
3A09h	RB1PPS	—	—	—	RB1PPS4	RB1PPS3	RB1PPS2	RB1PPS1	RB1PPS0	280
3A08h	RB0PPS		_	—	RB0PPS4	RB0PPS3	RB0PPS2	RB0PPS1	RB0PPS0	280
3A07h	RA7PPS		_	—	RA7PPS4	RA7PPS3	RA7PPS2	RA7PPS1	RA7PPS0	280
3A06h	RA6PPS		—	—	RA6PPS4	RA6PPS3	RA6PPS2	RA6PPS1	RA6PPS0	280
3A05h	RA5PPS		—	—	RA5PPS4	RA5PPS3	RA5PPS2	RA5PPS1	RA5PPS0	280
3A04h	RA4PPS	_	_	_	RA4PPS4	RA4PPS3	RA4PPS2	RA4PPS1	RA4PPS0	280
3A03h	RA3PPS			_	RA3PPS4	RA3PPS3	RA3PPS2	RA3PPS1	RA3PPS0	280
3A02h	RA2PPS	—	—	—	RA2PPS4	RA2PPS3	RA2PPS2	RA2PPS1	RA2PPS0	280
3A01h	RA1PPS	—	—	—	RA1PPS4	RA1PPS3	RA1PPS2	RA1PPS1	RA1PPS0	280
3A00h	RA0PPS	—	—	—	RA0PPS4	RA0PPS3	RA0PPS2	RA0PPS1	RA0PPS0	280
39FFh - 39F8h	—	Unimplemented								
39F7h	SCANPR		—	—	—	—		PR		31
39F6h - 39F5h	—	Unimplemented								
39F4h	DMA2PR	_	_	—	—	—		PR		31
39F3h	DMA1PR	_	_	—	—	—		30		
39F2h	MAINPR	—	—	—	—	_		30		
39F1h	ISRPR	—	—	—	—	—		PR		30
39F0h	—		Unimplemented							
39EFh	PRLOCK		—	—	—	—	—	—	PRLOCKED	31
39EEh - 39E7h	—	Unimplemented								
39E6h	NVMCON2				NVMCON2					211
39E5h	NVMCON1	RE	EG	—	FREE	WRERR	WREN	WR	RD	210
39E4h	<u> </u>	Unimplemented								0.10
39E3h	NVMDAT	DAT								
39E2h		— Unimplemented								011
39E1h	NVMADRH <sup>(4)</sup>	—	ADR							211
39E0h	ADR ADR ADR ADR ADR ADR ADR FRQ								211	
39DFh								KQ		107
39DEh	OSCIUNE			MEGEN		000051/				108
39DDh	OSCEN	EXIOEN	HFUEN	MFOEN	LFUEN	SUSCEN	ADOEN	—	-	109
39DCh	USUSTAI	EXTOR	HFUR	MFOR		SUR	ADOR	—	PLLR	100
39DBh	USCCON3	CSWHOLD	SOSCPWR	—	OKDY	NOSCR	—	—	—	105

#### TABLE 42-1:REGISTER FILE SUMMARY FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

3: Unimplemented on PIC18(L)F26/27/45/46/47K42 devices.

4: Unimplemented in PIC18(L)F45/55K42.

### 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

## APPENDIX A: REVISION HISTORY

### Revision A (6/2017)

Initial release of the document.

#### Revision B (12/2017)

Standard operating conditions updated in Section 44.0, Electrical Specifications. Other minor corrections.

### THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- Product Support Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- General Technical Support Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- Business of Microchip Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

### **CUSTOMER SUPPORT**

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: http://www.microchip.com/support