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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32t355-133dhgi

- **USB**
  - *Revision 1.1 compliant*
  - *USB slave device controller*
  - *Supports a 6th USB endpoint*
  - *Full speed operation at 12 Mb/s*
  - *Supports control, interrupt, bulk and isochronous endpoints*
  - *Supports USB remote wakeup*
  - *Integrated USB transceiver*
- **TDM**
  - *Serial Time Division Multiplexed (TDM) voice and data interface*
  - *Provides interface to telephone CODECs and DSPs*
  - *Interface to high quality audio A/Ds and D/As with external glue logic*
  - *Support 1 to 128 8-bit time slots*
  - *Compatible with Lucent CHI, GCI, Mitel ST-bus, K2 and SLD busses*
  - *Supports data rates of up to 8.192 Mb/s*
  - *Supports internal or external frame generation*
  - *Supports multiple non-contiguous active input and output time slots*
- **EJTAG**
  - *Run-time Mode provides a standard JTAG interface*
  - *Real-Time Mode provides additional pins for real-time trace information*
- **Ethernet**
  - *Full duplex support for 10 and 100 Mb/s Ethernet*
  - *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
  - *IEEE 802.3u auto-negotiation for automatic speed selection*
  - *Flexible address filtering modes*
  - *64-entry hash table based multicast address filtering*
- **ATM SAR**
  - *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
  - *Supports 25Mb/s and faster ATM*
  - *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
  - *Supports standard 53-byte ATM cells*
  - *Performs HEC generation and checking*
  - *Cell processing discards short cells and clips long cells*
  - *16 cells worth of buffering*
  - *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
  - *Hardware support for CRC-32 generation and checking for AAL5*
  - *Hardware support for CRC-10 generation and checking*
  - *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
  - *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*
- **System Features**
  - *JTAG Interface (IEEE Std. 1149.1 compatible)*
  - *208 pin PQFP package*
  - *2.5V core supply and 3.3V I/O supply*
  - *Up to 180 MHz pipeline frequency and up to 75 MHz bus frequency*

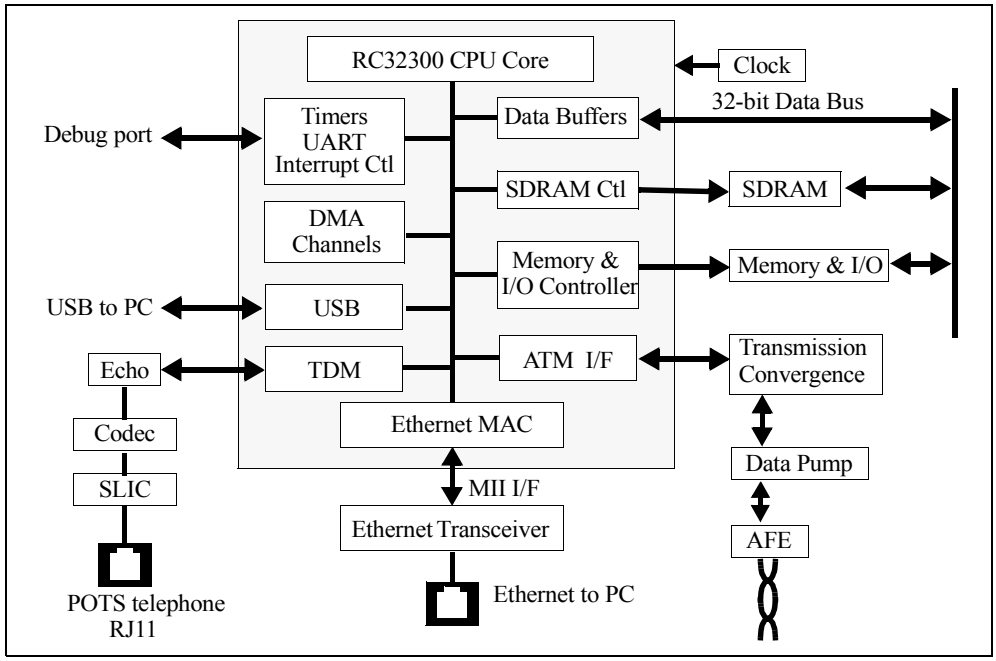


Figure 2 Example of xDSL Residential Gateway Using RC32355

Device Overview

The RC32355 is a “System on a Chip” which contains a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

The RC32355 meets the requirements of various embedded communications and digital consumer applications. It is a single chip solution that incorporates most of the generic system functionalities and application specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

CPU Execution Core

The RC32355 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The DSP instructions enable the RC32300 to implement 33.6 and 56kbps modem functionality in software, removing the need for external dedicated hardware. Cache locking guarantees real-time performance by holding critical DSP code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

Memory and I/O Controller

The RC32355 incorporates a flexible memory and peripheral device controller providing support for SDRAM, Flash ROM, SRAM, dual-port memory, and other I/O devices. It can interface directly to 8-bit boot ROM for a very low cost system implementation. It enables access to very high bandwidth external memory (380 MB/sec peak) at very low system costs. It also offers various trade-offs in cost / performance for the main memory architecture. The timers implemented on the RC32355 satisfy the requirements of most RTOS.

DMA Controller

The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The DMA controller supports scatter / gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

TDM Bus Interface

The RC32355 incorporates an industry standard TDM bus interface to directly access external devices such as telephone CODECs and quality audio A/Ds and D/As. This feature is critical for applications, such as cable modems and xDSL modems, that need to carry voice along with data to support Voice Over IP capability.

Ethernet Interface

The RC32355 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line interface with an MII interface. It supports up to 4 MAC addresses. In a SOHO router, the high performance RC32300 CPU core routes the data between the Ethernet and the ATM interface. In other applications, such as high speed modems, the Ethernet interface can be used to connect to the PC.

USB Device Interface

The RC32355 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC.

ATM SAR

The RC32355 includes a configurable ATM SAR that supports a UTOPIA level 1 or a UTOPIA level 2 interface. The ATM SAR is implemented as a hybrid between software and hardware. A hardware block provides the necessary low level blocks (like CRC generation and checking and cell buffering) while the software is used for higher level SARing functions. In xDSL modem applications, the UTOPIA port interfaces directly to an xDSL chip set. In SOHO routers or in a line card for a Layer 3 switch, it provides access to an ATM network.

Enhanced JTAG Interface for ICE

For low-cost In-Circuit Emulation (ICE), the RC32300 CPU core includes an Enhanced JTAG (EJTAG) interface. This interface consists of two operation modes: Run-Time Mode and Real-Time Mode.

The Run-Time Mode provides a standard JTAG interface for on-chip debugging, and the Real-Time Mode provides additional status pins—PCST[2:0]—which are used in conjunction with the JTAG pins for real-time trace information at the processor internal clock or any division of the pipeline clock.

Thermal Considerations

The RC32355 consumes less than 2.5 W peak power. It is guaranteed in a ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

March 29, 2001: Initial publication.

September 24, 2001: Removed references to DPI interface. Removed references to “edge-triggered interrupt input” for GPIO pins. Changed 208-pin package designation from DP to DH.

October 10, 2001: Revised AC timing characteristics in Tables 5, 6, 7, 8, 10, 12, and 15. Revised values in Table 18, “DC Electrical Characteristics”; Table 20, “RC32355 Power Consumption”; and Figure 23, “Typical Power Usage.” Changed data sheet from Preliminary to Final.

October 23, 2001: Revised Figure 23, “Typical Power Usage.”

November 1, 2001: Added Input Voltage Undershoot parameter and a footnote to Table 21.

January 30, 2002: In Table 6, changed values from 1.5 to 1.2 for the following signals: MDATA Tdo1, MADDR Tdo2, CASN Tdo3, CKENP Tdo4, BDIRN Tdo5, BOEN Tdo6.

May 20, 2002: Changed values in Table 20, Power Consumption.

September 19, 2002: Added COLDRSTN Trise1 parameter to Table 5, Reset and System AC Timing Characteristics.

December 6, 2002: In Features section, changed UART speed from 115 Kb/s to 1.5 Mb/s.

December 17, 2002: Added V_{OH} parameter to Table 18, DC Electrical Characteristics.

January 27, 2004: Added 180MHz speed grade.

May 25, 2004: In Table 7, signals MIIRXCLK and MIITXCLK, the Min and Max values for 10 Mbps Thigh1/Tlow1 were changed to 140 and 260 respectively and the Min and Max values for 100 Mbps Thigh1/Tlow1 were changed to 14.0 and 26.0 respectively.

Signal	Name/Description
MDATA[11]	**Hold SYSCLKP Constant**. For systems that do not require a SYSCLKP output and can instead use CLKP, setting this bit to a one causes the SYSCLKP output to be held at a constant level. This may be used to reduce EMI. 0x0 - Allow SYSCLKP to toggle 0x1 - Hold SYSCLKP constant
MDATA[12]	**JTAG Boundary Scan Reset Enable**. When this bit is set, Alternate 2 pin function, JTAG_TRST_N is selected. 0x0 - GPIOP[2] pin behaves as GPIOP 0x1 - GPIOP[2] pin behaves as JTAG_TRST_N
MDATA[13]	**CPU / DMA Transaction Indicator Enable**. When this bit is set, Alternate 2 pin function, CPUP is selected. 0x0 - GPIOP[4] pin behaves as GPIOP 0x1 - GPIOP[4] pin behaves as CPUP
MDATA[15:14]	**Reserved**. These pins must be driven low during boot configuration.

Table 2 Boot Configuration Vector Encoding (Part 2 of 2)

Clock Parameters

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%, V_{cc} Core and V_{cc}P = +2.5V±5%)

Parameter	Symbol	Reference Edge	133MHz		150MHz		180MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Internal CPU pipeline clock[1]	Frequency	none	100	133	100	150	100	180	MHz	Figure 4
CLKP[2,3,4]	Frequency	none	25	67	25	75	25	90	MHz	
	Tperiod1		15	40	13.3	40	11.1	40	ns	
	Thigh1		6	—	5.4	—	5.4	—	ns	
	Tlow1		6	—	5.4	—	5.4	—	ns	
	Trise1		—	3	—	2.5	—	2.5	ns	
	Tfall1		—	3	—	2.5	—	2.5	ns	
	Tjitter		—	±250	—	±200	—	±200	ps	

[1] The CPU pipeline clock speed is selected during cold reset by the boot configuration vector (see Table 2).
[2] Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.
[3] USB clock (USBCLKP) frequency must be less than CLKP frequency.
[4] ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

Table 3 Clock Parameters

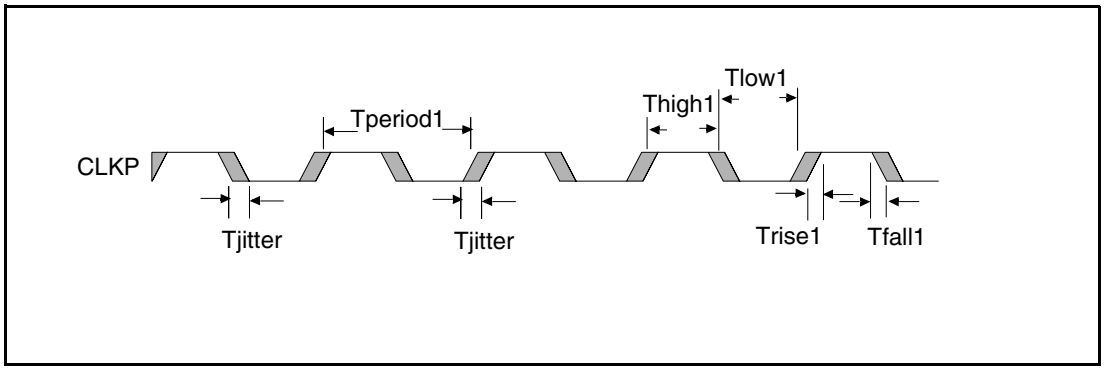


Figure 4 Clock Parameters Waveform

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

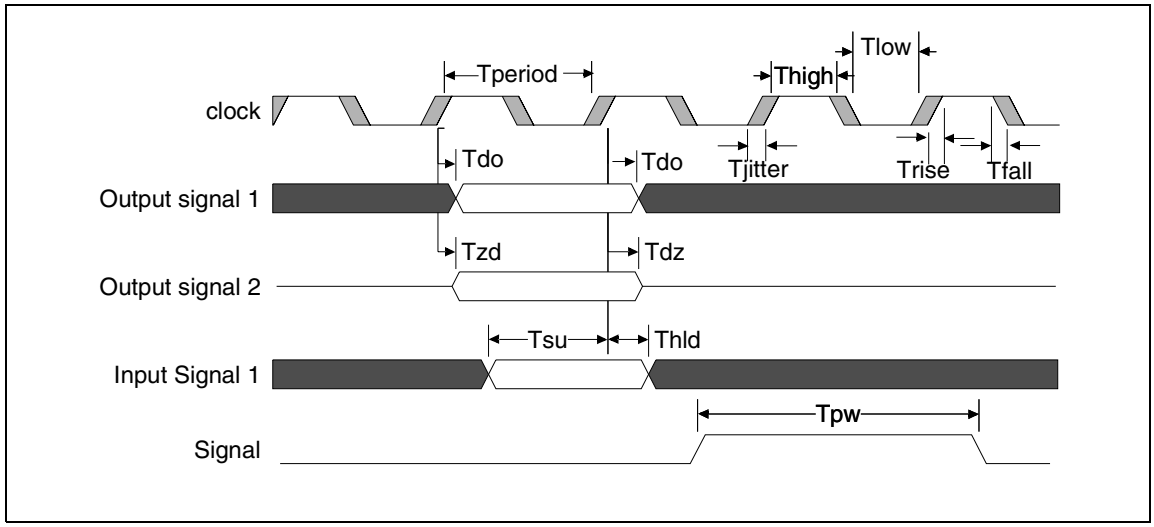


Figure 5 AC Timing Definitions Waveform

Symbol	Definition
Tperiod	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active.

Table 4 AC Timing Definitions

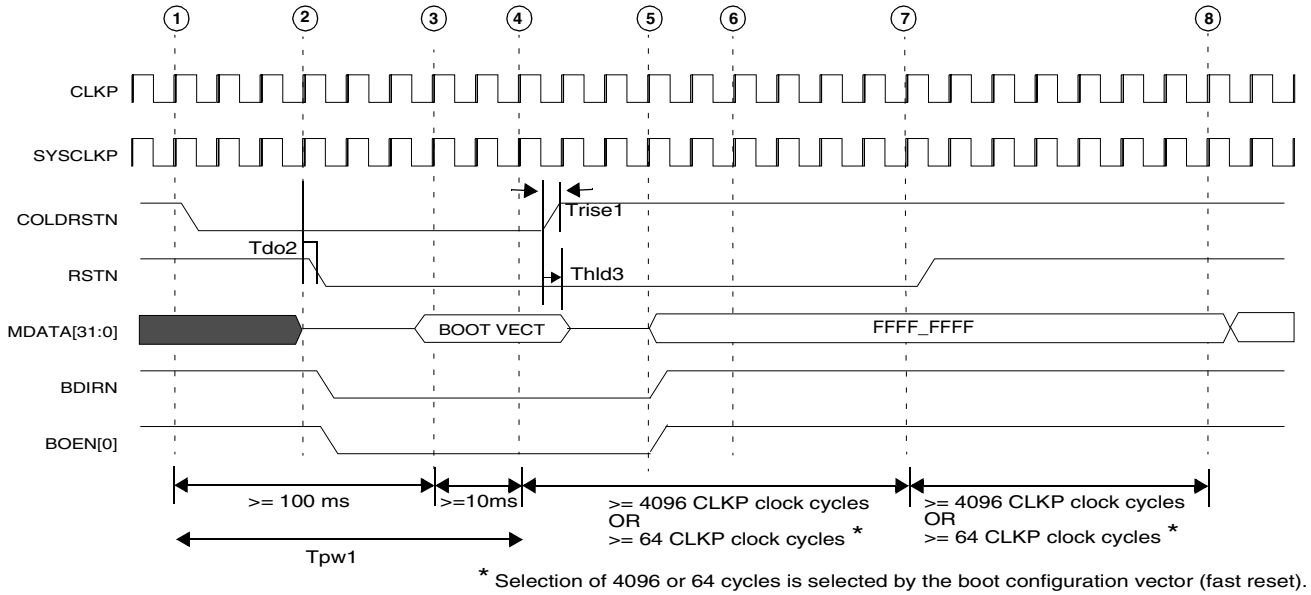
AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%,V_{cc} Core = +2.5V±5%, V_{cc}P = +2.5V±5%)

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Reset and System											
COLDRSTN	Tpw1	none	110	—	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	—	5.0	ns		
RSTN[1]	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5.0	8.0	5.0	8.0	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7.0	3.5	7.0	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	3.5	6.6	ns		
DMAREQN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	3.3	5.8	ns		

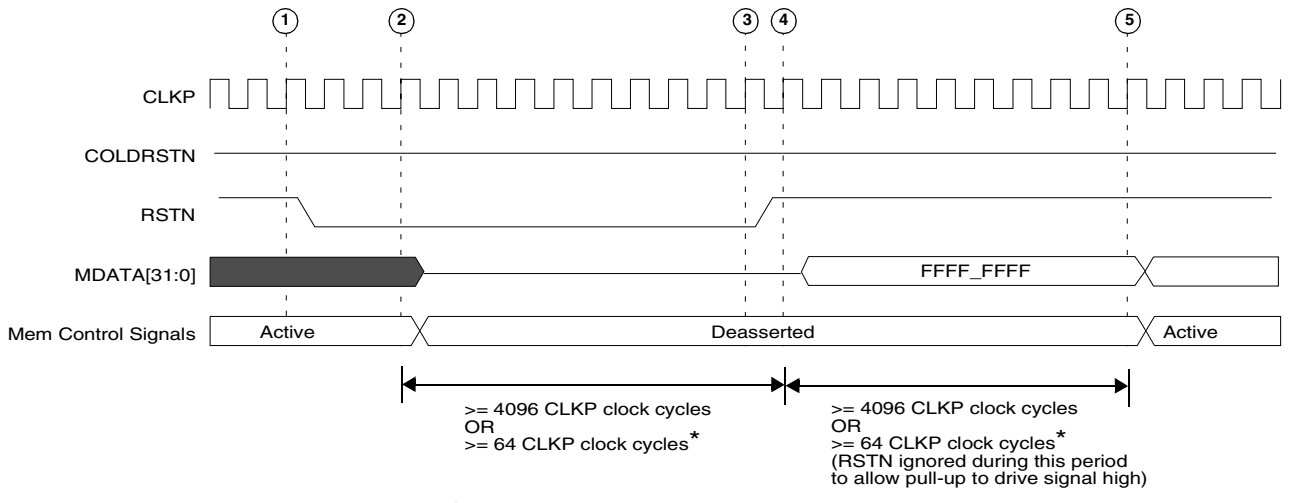
[1] RSTN is a bidirectional signal. It is treated as an asynchronous input.
[2] DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.

Table 5 Reset and System AC Timing Characteristics



1. COLDRSTN asserted by external logic.
2. The RC32355 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32355 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32355 stops sampling the boot configuration vector.
5. The RC32355 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLKP may be held constant after this point if Hold SYSCLKP Constant is selected in the boot configuration vector.
7. RSTN negated by RC32355.
8. CPU begins executing by taking MIPS reset exception, and the RC32355 starts sampling RSTN as a warm reset input.

Figure 6 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32355 asserts RSTN output low in response.
2. The RC32355 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32355 deasserts RSTN.
4. The RC32355 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - SDRAM Access											
MDATA[31:0]	Tsu1	SDCLKINP rising	2.5	—	2.5	—	2.5	—	ns		Figure 8 Figure 9 Figure 10
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1	SYSCLKP rising	1.2	5.8	1.2	5.8	1.2	5.8	ns		
	Tdz1		—	5.0	—	5.0	—	5.0	ns		
	Tzd1		1.0	—	1.0	—	1.0	—	ns		
MADDR[20:2], BWEN[3:0]	Tdo2	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CASN, RASN, SDCSN[1:0], SDWEN	Tdo3	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CKENP	Tdo4	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BDIRN	Tdo5	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BOEN[1:0]	Tdo6	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
SYSCLKP rising	Tdo7	CLKP rising	0.5	5.0	0.5	5.0	0.5	5.0	ns		
SDCLKINP	Tperiod8	none	15	50	13.3	50	13.3	50	ns		
	Thigh8,Tlow8		6.0	—	5.4	—	5.4	—	ns		
	Trise8,Tfall8		—	3.0	—	2.5	—	2.5	ns		
	Tdelay8	SYSCLKP rising	0	4.8	0	4.8	0	4.8	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - Device Access											
MDATA[31:0]	Tsu1	CLKP rising	2.5	—	2.5	—	2.5	—	ns		Figure 11 Figure 12
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1		2.0	6.5	2.0	6.5	2.0	6.5	ns		
	Tdz1		—	9.0	—	9.0	—	9.0	ns		
	Tzd1		2.0	—	2.0	—	2.0	—	ns		
WAITACKN, BRN	Tsu	CLKP rising	2.5	—	2.5	—	2.5	—	ns		
	Thld		1.5	—	1.5	—	1.5	—	ns		
MADDR[21:0]	Tdo2	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz2		—	9.0	—	9.0	—	9.0	ns		
	Tzd2		2.0	—	2.0	—	2.0	—	ns		
MADDR[25:22]	Tdo3	CLKP rising	2.5	6.5	2.5	6.5	2.5	6.5	ns		
	Tdz3		—	9.0	—	9.0	—	9.0	ns		
	Tzd3		2.0	—	2.0	—	2.0	—	ns		
BDIRN, BOEN[0]	Tdo4	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz4		—	9.0	—	9.0	—	9.0	ns		
	Tzd4		2.0	—	2.0	—	2.0	—	ns		
BGN, BWEN[3:0], OEN, RWN	Tdo5	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz5		—	9.0	—	9.0	—	9.0	ns		
	Tzd5		2.0	—	2.0	—	2.0	—	ns		
CSN[3:0]	Tdo6	CLKP rising	1.7	5.0	1.7	5.0	1.7	5.0	ns		
	Tdz6		—	9.0	—	9.0	—	9.0	ns		
	Tzd6		2.0	—	2.0	—	2.0	—	ns		
CSN[5:4]	Tdo7	CLKP rising	2.5	6.0	2.5	6.0	2.5	6.0	ns		
	Tdz7		—	9.0	—	9.0	—	9.0	ns		
	Tzd7		2.0	—	2.0	—	2.0	—	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

Note: The RC32355 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32355 are both driving. See the chapters “Device Controller,” “Synchronous DRAM Controller,” and “Bus Arbitration” in the RC32355 User Reference Manual.

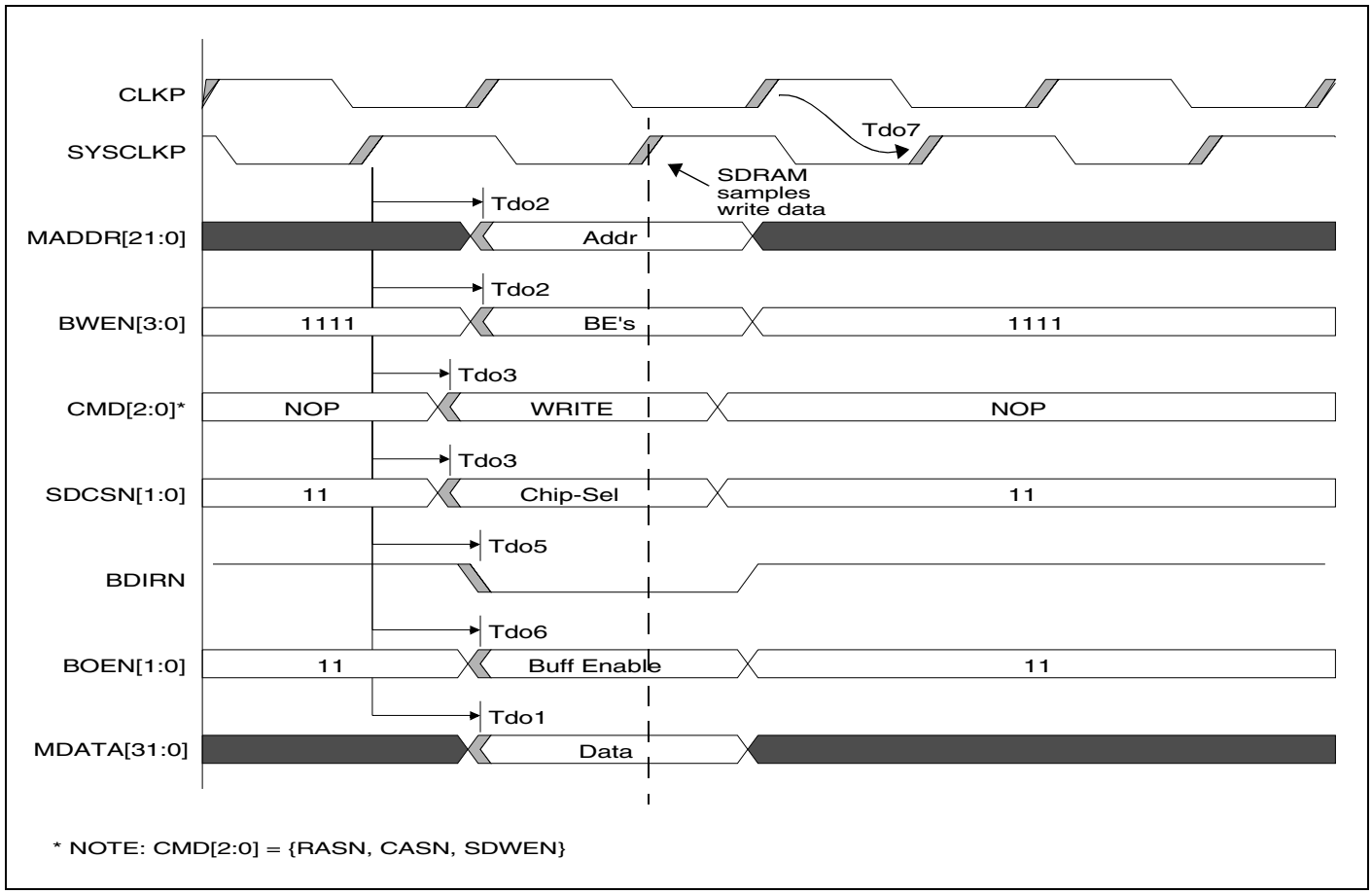


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

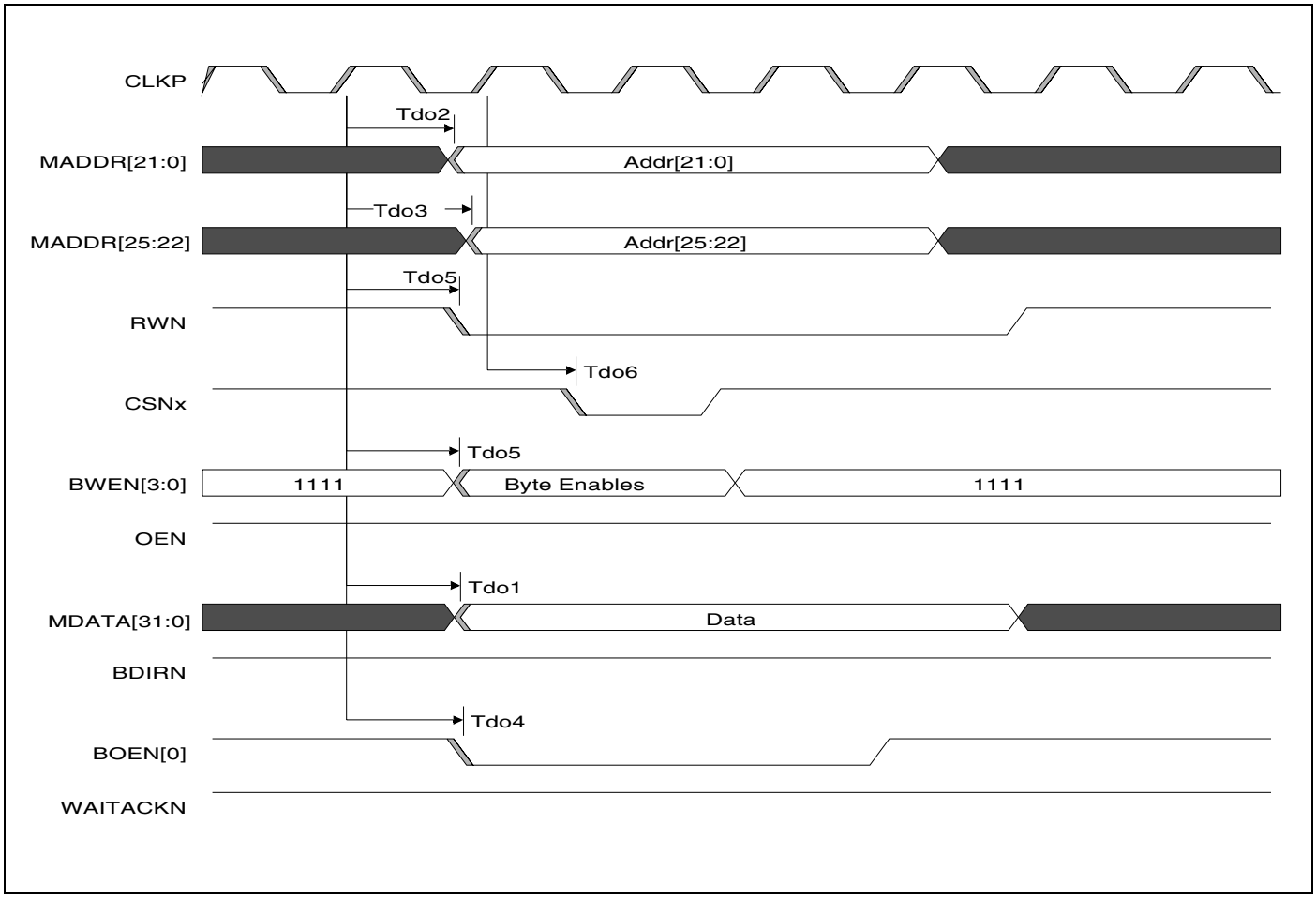


Figure 12 Memory AC and Peripheral Bus Timing Waveform - Device Write Access

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
ATM Interface, Utopia Mode[1, 2]											
RXCLKP, TXCLKP[1]	Tperiod1	none	—	40	—	40	—	40	ns	25 MHz Utopia	Figure 14
	Thigh1,Tlow1		16	—	16	—	16	—	ns		
	Trise1,Tfall1		—	4	—	4	—	4	ns		
RXCLKP, TXCLKP[1]	Tperiod1	none	—	30	—	30	—	30	ns	33 MHz Utopia	
	Thigh1,Tlow1		12	—	12	—	12	—	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
RXCLKP, TXCLKP	Tperiod1	none	—	20	—	20	—	20	ns	50 MHz Utopia	
	Thigh,Tlow1		8	—	8	—	8	—	ns		
	Trise1,Tfall1		—	2	—	2	—	2	ns		
TXFULLN	Tsu2	TXCLKP rising	2	—	2	—	2	—	ns		
	Thld2		2	—	2	—	2	—	ns		
TXDATA[7:0], TXSOC, TXENBN, TXADDR[1:0]	Tdo3	TXCLKP rising	4	8	4	8	4	8	ns		
RXDATA[7:0], RXEMP-TYN, RXSOC	Tsu4	RXCLKP rising	3	—	3	—	3	—	ns		
	Thld4		2	—	2	—	2	—	ns		
RXADDR[1:0], RXENBN	Tdo5	RXCLKP rising	3	8	3	8	3	8	ns		

Table 8 ATM AC Timing Characteristics

1. ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

2. All Utopia Mode pins are multiplexed on the ATM interface pins as described in Table 9.

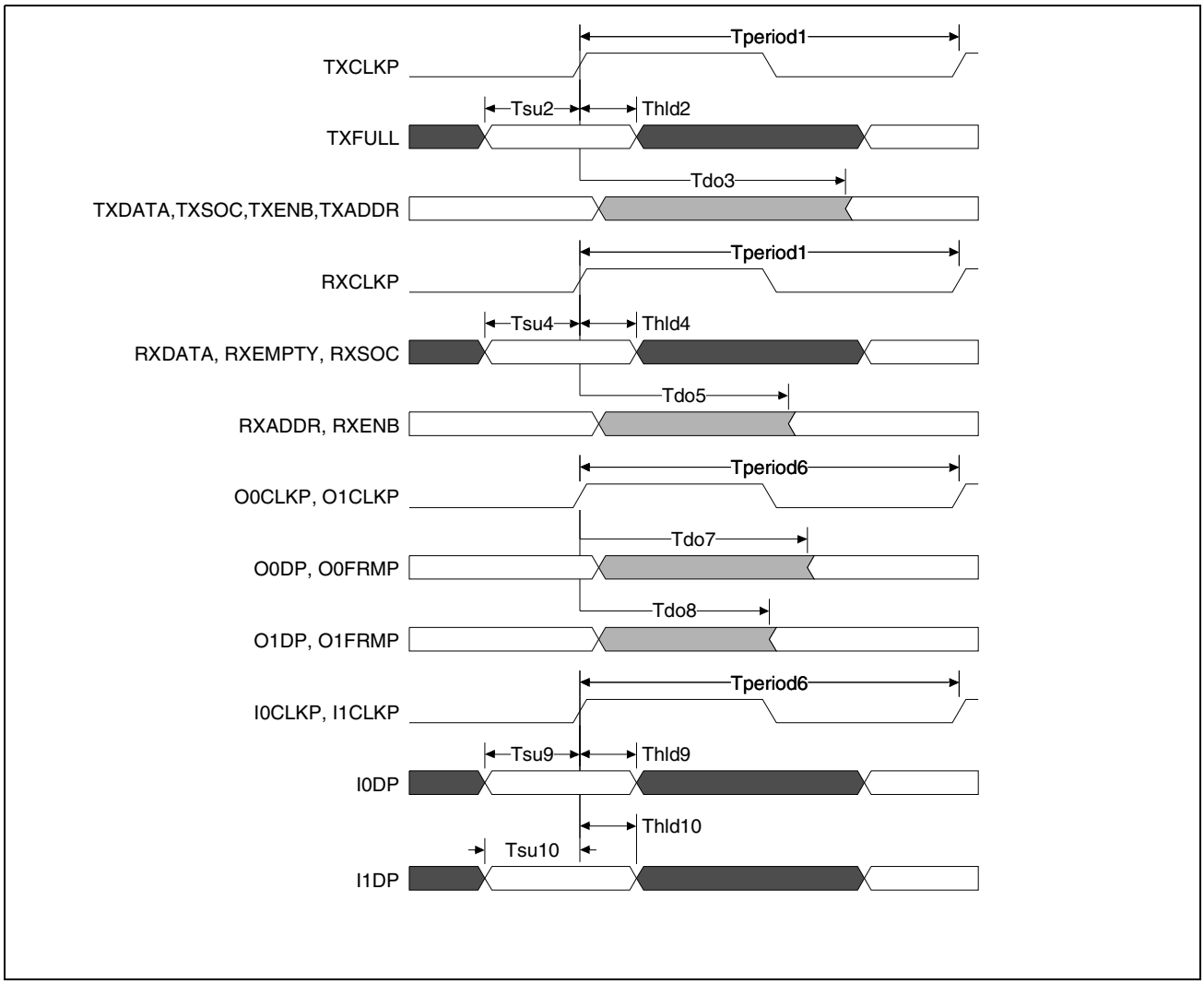


Figure 14 ATM AC Timing Waveform

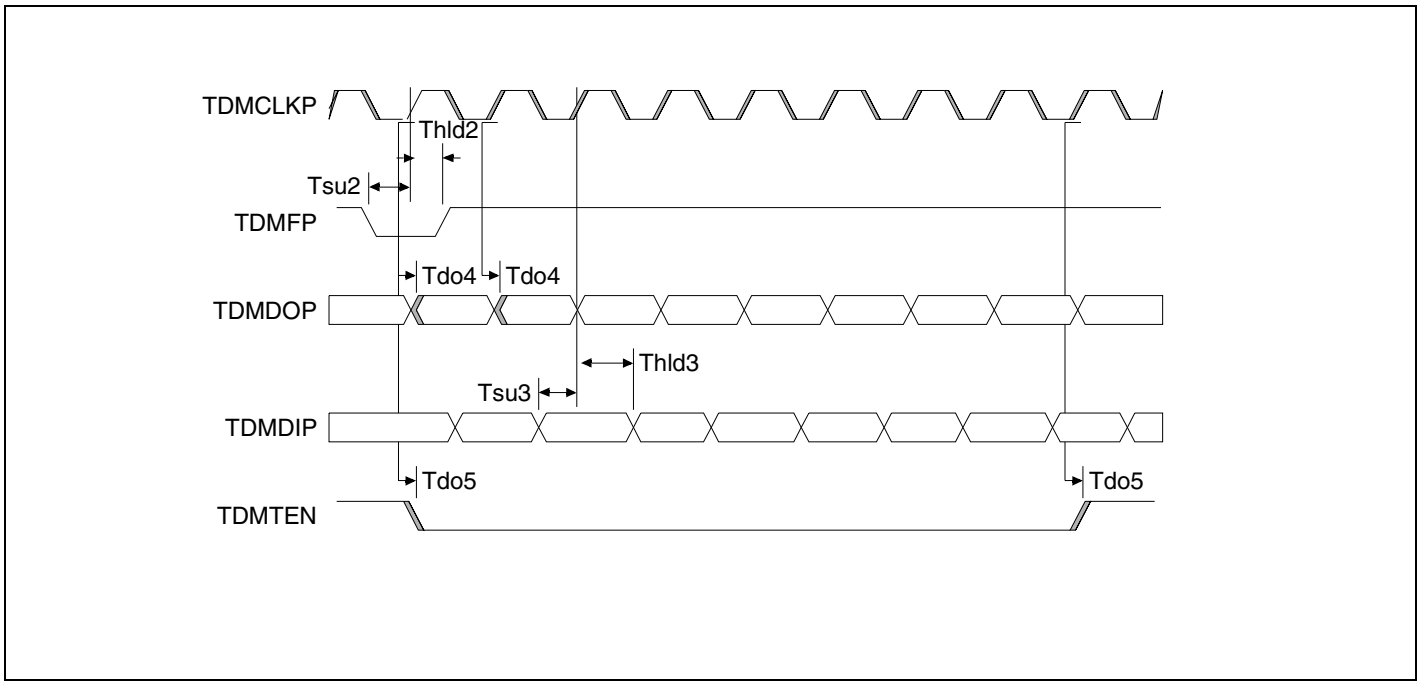


Figure 16 TDM AC Timing Waveform, Slave Mode

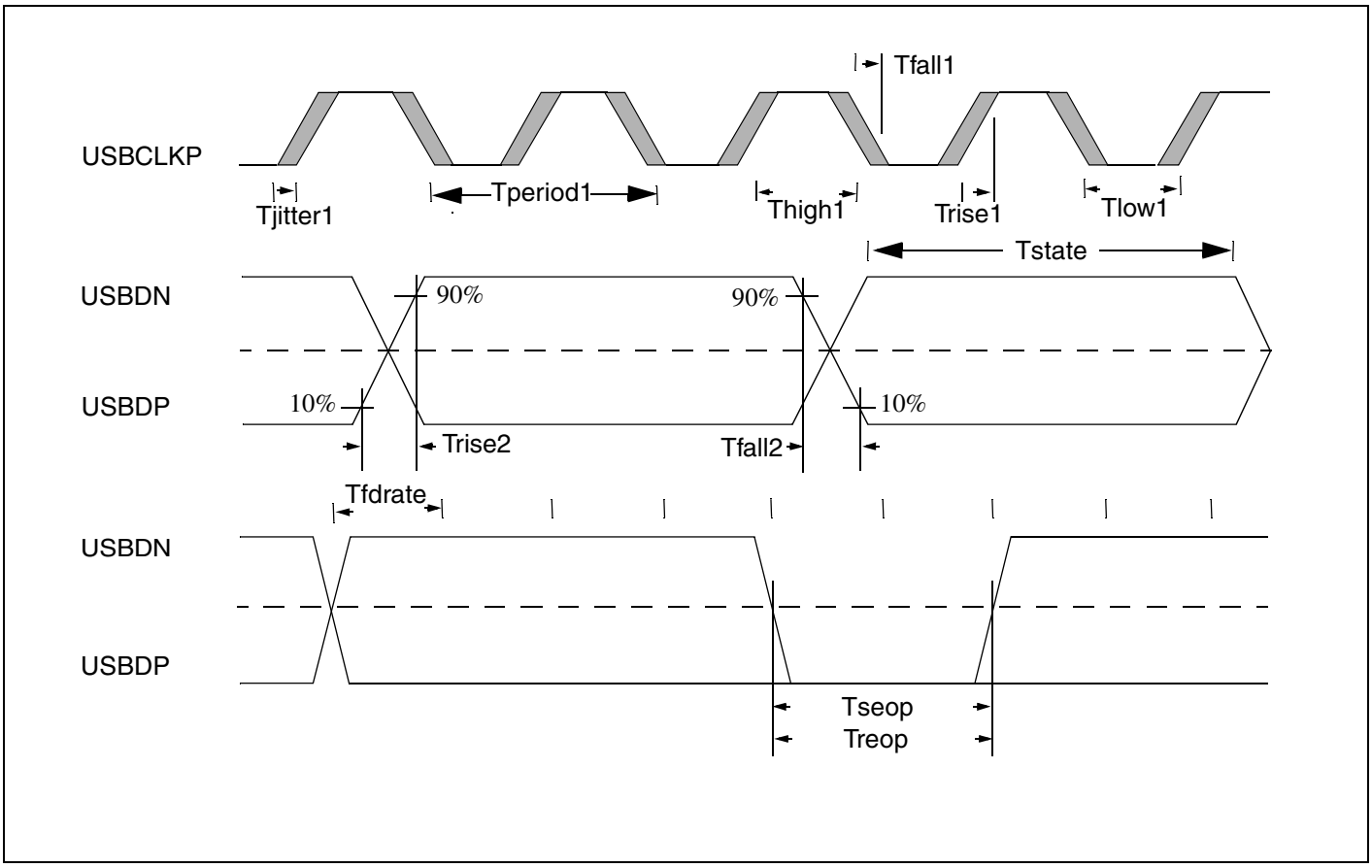


Figure 17 USB AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
UART											
U0SINP, U0RIN, U0DCDN, U0DSRN, U0CTSN, U1SINP, U1DSRN, U1CTSN	Tsu[1]	CLKP rising	5	—	5	—	5	—	ns		
	Thld[1]		3	—	3	—	3	—	ns		
U0SOUTP, U0DTRN, U0RTSN, U1SOUTP, U1DTRN, U1RTSN	Tdo[1]	CLKP rising	1	12	1	12	1	12	ns		
[1] These are asynchronous signals and the values are provided for ATE (test) only.											

Table 12 UART AC Timing Characteristics

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
I^2C[1]											
SCLP	Frequency	none	0	100	0	100	0	100	kHz	100 KHz	Figure 18
	Thigh1		4.0	—	4.0	—	4.0	—	µs		
	Tlow1		4.7	—	4.7	—	4.7	—	µs		
	Trise1		—	1000	—	1000	—	1000	ns		
	Tfall1		—	300	—	300	—	300	ns		
SDAP	Tsu2	SCLP rising	250	—	250	—	250	—	ns		
	Thld2		0	3.45	0	3.45	0	3.45	µs		
	Trise2		—	1000	—	1000	—	1000	ns		
	Tfall2		—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu3	SDAP falling	4.7	—	4.7	—	4.7	—	µs		
	Thld3		4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu4	SDAP rising	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay5		4.7	—	4.7	—	4.7	—	µs		
SCLP	Frequency	none	0	400	0	400	0	400	kHz	400 KHz	
	Thigh1		0.6	—	0.6	—	0.6	—	µs		
	Tlow1		1.3	—	1.3	—	1.3	—	µs		
	Trise1		—	300	—	300	—	300	ns		
	Tfall1		—	300	—	300	—	300	ns		
SDAP	Tsu2	SCLP rising	100	—	100	—	100	—	ns		
	Thld2		0	0.9	0	0.9	0	0.9	µs		
	Trise2		—	300	—	300	—	300	ns		
	Tfall2		—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu3	SDAP falling	0.6	—	0.6	—	0.6	—	µs		
	Thld3		0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu4	SDAP rising	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay5		1.3	—	1.3	—	1.3	—	µs		

Table 13 I^2C AC Timing Characteristics

1. For more information see the I^2C-Bus specification by Philips Semiconductor

USB Electrical Characteristics

	Parameter	Min	Max	Unit	Conditions
USB Interface					
V_{di}	Differential Input Sensitivity	-0.2		V	I(D+)-(D-)I
V_{cm}	Differential Input Common Mode Range	0.8	2.5	V	
V_{se}	Single ended Receiver Threshold	0.8	2.0	V	
C_{in}	Transceiver Capacitance		20	pF	
I_{li}	Hi-Z State Data Line Leakage	-10	10	µA	$0V < V_{in} < 3.3V$
USB Upstream/Downstream Port					
V_{oh}	Static Output High	2.8	3.6	V	15km ± 5% to Gnd
V_{ol}	Static Output Low		0.3	V	
Z_o	USB Driver Output Impedance	28	44	Ω	Including $R_{ext} = 20\ \Omega$

Table 19 USB Interface Characteristics

Power Consumption

Note: This table is based on a 2:1 CPU pipeline to system (PClock to CLKP) clock ratio.

Parameter		133MHz		150MHz		180MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC} I/O		80	130	100	150	120	170	mA	
$I_{CC\ core}$	Normal mode	400	450	450	500	500	550	mA	C_L = 25pF (affects I/O) $T_a = 25^oC$ VccP = 2.625V (for max. values) V_{cc} core = 2.625V (for max. values) V_{cc} I/O = 3.46V (for max. values) VccP = 2.5V (for typical values) V_{cc} core = 2.5V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	320	370	360	410	400	450	mA	
Power Dissipation	Normal mode	1.26	1.63	1.46	1.86	1.73	2.03	W	
	Standby mode[1]	1.06	1.42	1.22	1.59	1.47	1.77	W	

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions; however, other logic continues to function. Standby mode reduces power consumption by 0.6 mA per MHz of the CPU pipeline clock, PClock.

Table 20 RC32355 Power Consumption

Alternate Pin Functions

Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		51	GPIOP[32]	TDMDOP	
21	GPIOP[01]	U0SINP		54	GPIOP[16]	CSN[4]	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	55	GPIOP[17]	CSN[5]	
24	GPIOP[03]	U0DCRN		56	GPIOP[18]	DMAREQN	
27	GPIOP[04]	U0DTRN	CPUP	59	GPIOP[19]	DMADONEN	
28	GPIOP[05]	U0DSRN		60	GPIOP[20]	USBSOF	
33	GPIOP[06]	U0RTSN		62	GPIOP[21]	CKENP	
35	GPIOP[07]	U0CTSN		64	GPIOP[22]	TXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	65	GPIOP[23]	TXADDR[1]	DMAP[0]
39	GPIOP[09]	U1SINP	DMAP[2]	66	GPIOP[24]	RXADDR[0]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	69	GPIOP[26]	TDMTEN	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	71	GPIOP[27]	MADDR[22]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	73	GPIOP[28]	MADDR[23]	
46	GPIOP[14]	SDAP		74	GPIOP[29]	MADDR[24]	
47	GPIOP[15]	SCLP		75	GPIOP[30]	MADDR[25]	
48	GPIOP[35]	TDMCLKP		76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
49	GPIOP[34]	TDMFP					
50	GPIOP[33]	TDMDIP					

Table 23 Alternate Pin Functions

Package Drawing - 208-pin QFP