Renesas Electronics America Inc - IDT79RC32T355-133DH Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t355-133dh

- **USB**
  - *Revision 1.1 compliant*
  - *USB slave device controller*
  - *Supports a 6th USB endpoint*
  - *Full speed operation at 12 Mb/s*
  - *Supports control, interrupt, bulk and isochronous endpoints*
  - *Supports USB remote wakeup*
  - *Integrated USB transceiver*
- **TDM**
  - *Serial Time Division Multiplexed (TDM) voice and data interface*
  - *Provides interface to telephone CODECs and DSPs*
  - *Interface to high quality audio A/Ds and D/As with external glue logic*
  - *Support 1 to 128 8-bit time slots*
  - *Compatible with Lucent CHI, GCI, Mitel ST-bus, K2 and SLD busses*
  - *Supports data rates of up to 8.192 Mb/s*
  - *Supports internal or external frame generation*
  - *Supports multiple non-contiguous active input and output time slots*
- **EJTAG**
  - *Run-time Mode provides a standard JTAG interface*
  - *Real-Time Mode provides additional pins for real-time trace information*
- **Ethernet**
  - *Full duplex support for 10 and 100 Mb/s Ethernet*
  - *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
  - *IEEE 802.3u auto-negotiation for automatic speed selection*
  - *Flexible address filtering modes*
  - *64-entry hash table based multicast address filtering*
- **ATM SAR**
  - *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
  - *Supports 25Mb/s and faster ATM*
  - *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
  - *Supports standard 53-byte ATM cells*
  - *Performs HEC generation and checking*
  - *Cell processing discards short cells and clips long cells*
  - *16 cells worth of buffering*
  - *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
  - *Hardware support for CRC-32 generation and checking for AAL5*
  - *Hardware support for CRC-10 generation and checking*
  - *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
  - *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*
- **System Features**
  - *JTAG Interface (IEEE Std. 1149.1 compatible)*
  - *208 pin PQFP package*
  - *2.5V core supply and 3.3V I/O supply*
  - *Up to 180 MHz pipeline frequency and up to 75 MHz bus frequency*

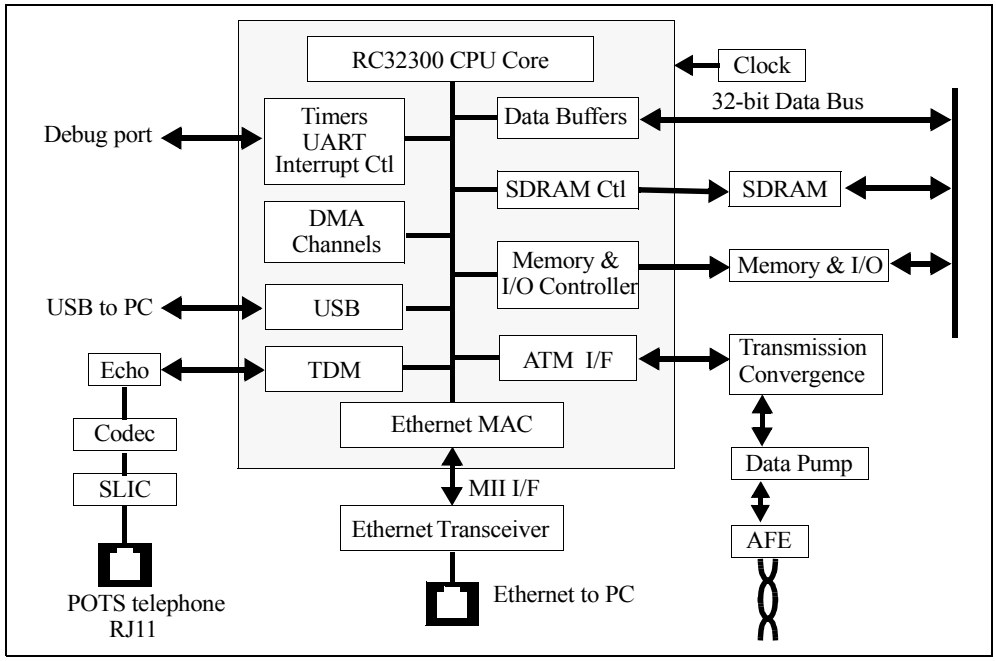


Figure 2 Example of xDSL Residential Gateway Using RC32355

Name	Type	I/O Type	Description
RWN	O	High Drive	**Read or Write.** This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device, a low level indicates a write to an external device.
OEN	O	High Drive	**Output Enable.** This signal is asserted low when data should be driven by an external device during device read transactions on the memory and peripheral bus.
BWEN[3:0]	O	High Drive	**SDRAM Byte Enable Mask or Memory and I/O Byte Write Enables.** These signals are used as data input/output masks during SDRAM transactions and as byte write enable signals during device controller transactions on the memory and peripheral bus. They are active low. BWEN[0] corresponds to byte lane MDATA[7:0]. BWEN[1] corresponds to byte lane MDATA[15:8]. BWEN[2] corresponds to byte lane MDATA[23:16]. BWEN[3] corresponds to byte lane MDATA[31:24].
SDCSN[1:0]	O	High Drive	**SDRAM Chip Select.** These signals are used to select the SDRAM device on the memory and peripheral bus. Each bit is asserted low during an access to the selected SDRAM.
RASN	O	High Drive	**SDRAM Row Address Strobe**. The row address strobe asserted low during memory and peripheral bus SDRAM transactions.
CASN	O	High Drive	**SDRAM Column Address Strobe.** The column address strobe asserted low during memory and peripheral bus SDRAM transactions.
SDWEN	O	High Drive	**SDRAM Write Enable.** Asserted low during memory and peripheral bus SDRAM write transactions.
CKENP	O	Low Drive	**SDRAM Clock Enable.** Asserted high during active SDRAM clock cycles. Primary function: General Purpose I/O, GPIOP[21].
SDCLKINP	I	STI	**SDRAM Clock Input.** This clock input is a delayed version of SYSCLKP. SDRAM read data is sampled into the RC32355 on the rising edge of this clock.
ATM Interface			
ATMINP[11:0]	I	STI	**ATM PHY Inputs.** These pins are the inputs for the ATM interface.
ATMIOP[1:0]	I/O	Low Drive with STI	**ATM PHY Bidirectional Signals.** These pins are the bidirectional pins for the ATM interface.
ATMOUTP[9:0]	O	Low Drive	**ATM PHY Outputs.** These pins are the outputs for the ATM interface.
TXADDR[1:0]	O	Low Drive	**ATM Transmit Address [1:0]**. 2-bit address bus used for transmission in Utopia-2 mode. TXADDR[0] Primary function: General purpose I/O, GPIOP[22]. TXADDR[1] Primary function: General purpose I/O, GPIOP[23].
RXADDR[1:0]	O	Low Drive	**ATM Receive Address [1:0]**. 2-bit address bus for receiving in Utopia-2 mode. RXADDR[0] Primary function: General purpose I/O, GPIOP[24]. RXADDR[1] Primary function: General purpose I/O, GPIOP[25].
TDM Bus			
TDMDOP	O	High Drive	**TDM Serial Data Output.** Serial data is driven by the RC32355 on this signal during an active output time slot. During inactive time slots this signal is tri-stated. Primary function: General purpose I/O, GPIOP[32].
TDMDIP	I	STI	**TDM Serial Data Input.** Serial data is received by the RC32355 on this signal during active input time slots. Primary function: General purpose I/O, GPIOP[33].
TDMFP	I/O	High Drive	**TDM Frame Signal.** A transition on this signal, the active polarity of which is programmable, delineates the start of a new TDM bus frame. TDMFP is driven if the RC32355 is a master, and is received if it is a slave. Primary function: General purpose I/O, GPIOP[34].
TDMCLKP	I	STI	**TDM Clock.** This input clock controls the rate at which data is sent and received on the TDM bus. Primary function: General purpose I/O, GPIOP[35].

Table 1 Pin Descriptions (Part 2 of 8)

Name	Type	I/O Type	Description
TDMTEN	O	Low Drive	**TDM External Buffer Enable.** This signal controls an external tri-state buffer output enable connected to the TDM output data, TDMDOP. It is asserted low when the RC32355 is driving data on TDMDOP. Primary function: General Purpose I/O, GPIOP[26]
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
GPIOP[5]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data set ready, U0DSRN.
GPIOP[6]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 request to send, U0RTSN.
GPIOP[7]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 clear to send, U0CTSN.
GPIOP[8]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial output, U1SOUTP. 2nd Alternate function: Active DMA channel code, DMAP[3].
GPIOP[9]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial input, U1SINP. 2nd Alternate function: Active DMA channel code, DMAP[2].
GPIOP[10]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[0].
GPIOP[11]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data set ready, U1DSRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[1].
GPIOP[12]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 request to send, U1RTSN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[2].
GPIOP[13]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 clear to send, U1CTSN. 2nd Alternate function: ICE PC trace clock, EJTAG_DCLK.
GPIOP[14]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface data, SDAP.
GPIOP[15]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface clock, SCLP.
GPIOP[16]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[4].

Table 1 Pin Descriptions (Part 3 of 8)

Name	Type	I/O Type	Description
JTAG_TMS	I	STI	**JTAG Mode Select**. This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 16.
EJTAG_PCST[0]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	**PC trace clock.** This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.
EJTAG_TRST_N	I	STI	**EJTAG Test Reset.** EJTAG_TRST_N is an active-low signal for asynchronous reset of only the EJTAG/ICE controller. EJTAG_TRST_N requires an external pull-up on the board. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary: General Purpose I/O, GPIOP[31] 1st Alternate function: DMA finished output, DMAFIN.
JTAG_TRST_N	I	STI	**JTAG Test Reset.** JTAG_TRST_N is an active-low signal for asynchronous reset of only the JTAG boundary scan controller. JTAG_TRST_N requires an external pull-down on the board that will hold the JTAG boundary scan controller in reset when not in use if selected. JTAG reset enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[2]. 1st Alternate function: UART channel 0 ring indicator, U0RIN.
Debug			
INSTP	O	Low Drive	**Instruction or Data Indicator**. This signal is driven high during CPU instruction fetches and low during CPU data transactions on the memory and peripheral bus.
CPUP	O	Low Drive	**CPU or DMA Transaction Indicator**. This signal is driven high during CPU transactions and low during DMA transactions on the memory and peripheral bus if CPU/DMA Transaction Indicator Enable is enabled. CPU/DMA Status mode enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[4]. 1st Alternate function: UART channel 0 data terminal ready U0DTRN.
DMAP[0]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[23]. 1st Alternate function: TXADDR[1].
DMAP[1]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[25]. 1st Alternate function: RXADDR[1].

Table 1 Pin Descriptions (Part 6 of 8)

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

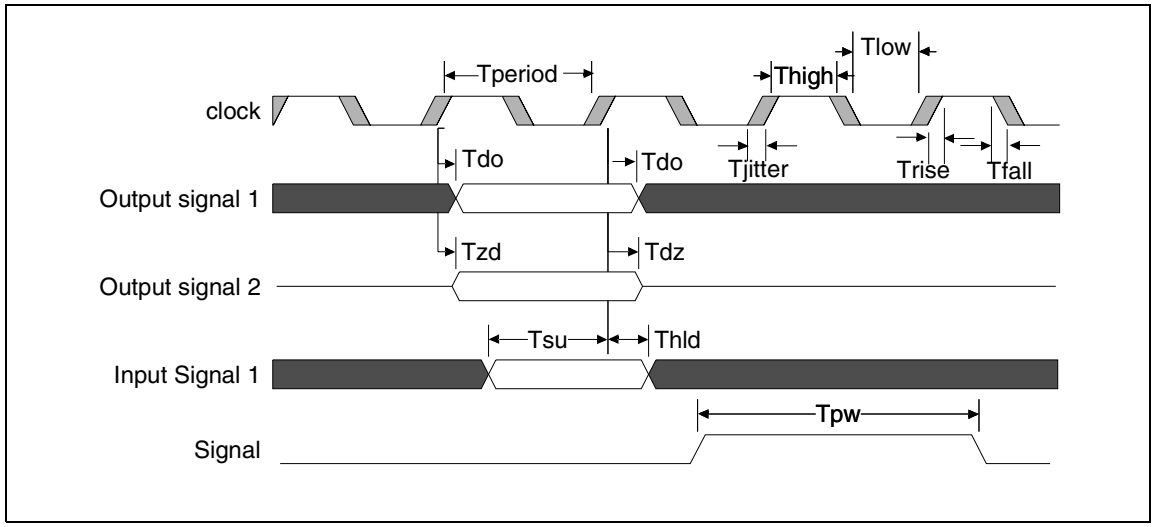


Figure 5 AC Timing Definitions Waveform

Symbol	Definition
Tperiod	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active.

Table 4 AC Timing Definitions

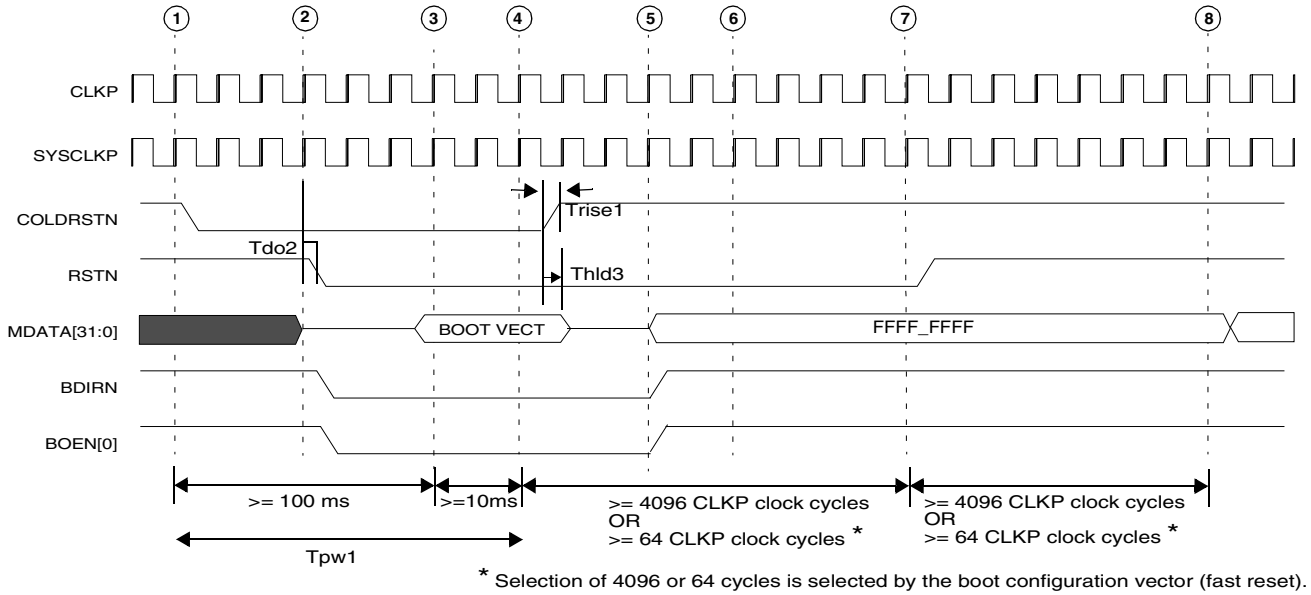
AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%,V_{cc} Core = +2.5V±5%, V_{cc}P = +2.5V±5%)

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Reset and System											
COLDRSTN	Tpw1	none	110	—	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	—	5.0	ns		
RSTN[1]	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5.0	8.0	5.0	8.0	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7.0	3.5	7.0	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	3.5	6.6	ns		
DMAREQN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	3.3	5.8	ns		

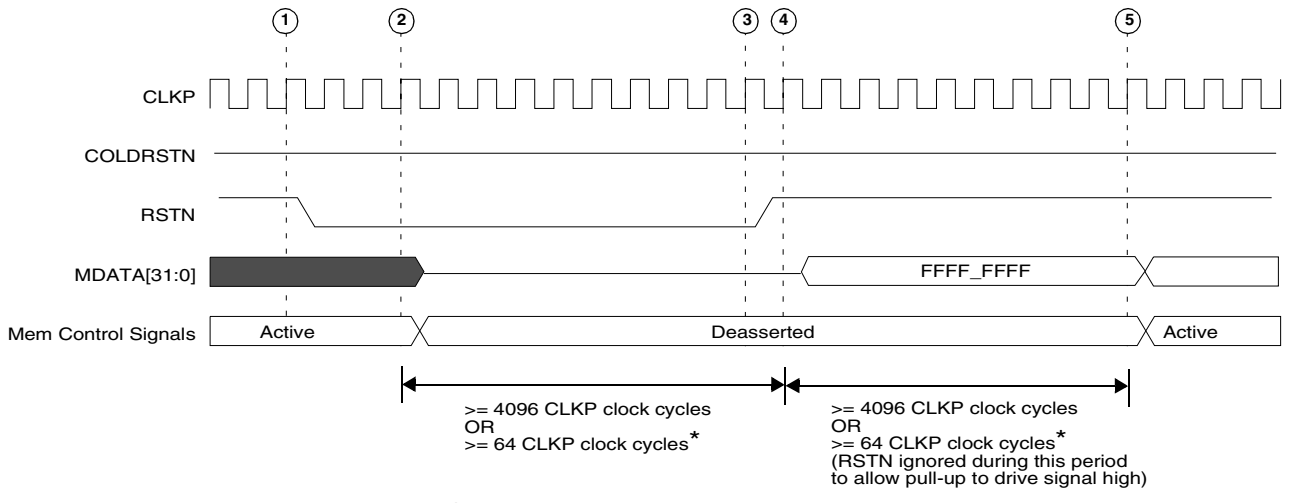
[1] RSTN is a bidirectional signal. It is treated as an asynchronous input.
[2] DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.

Table 5 Reset and System AC Timing Characteristics



1. COLDRSTN asserted by external logic.
2. The RC32355 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32355 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32355 stops sampling the boot configuration vector.
5. The RC32355 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLKP may be held constant after this point if Hold SYSCLKP Constant is selected in the boot configuration vector.
7. RSTN negated by RC32355.
8. CPU begins executing by taking MIPS reset exception, and the RC32355 starts sampling RSTN as a warm reset input.

Figure 6 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32355 asserts RSTN output low in response.
2. The RC32355 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32355 deasserts RSTN.
4. The RC32355 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

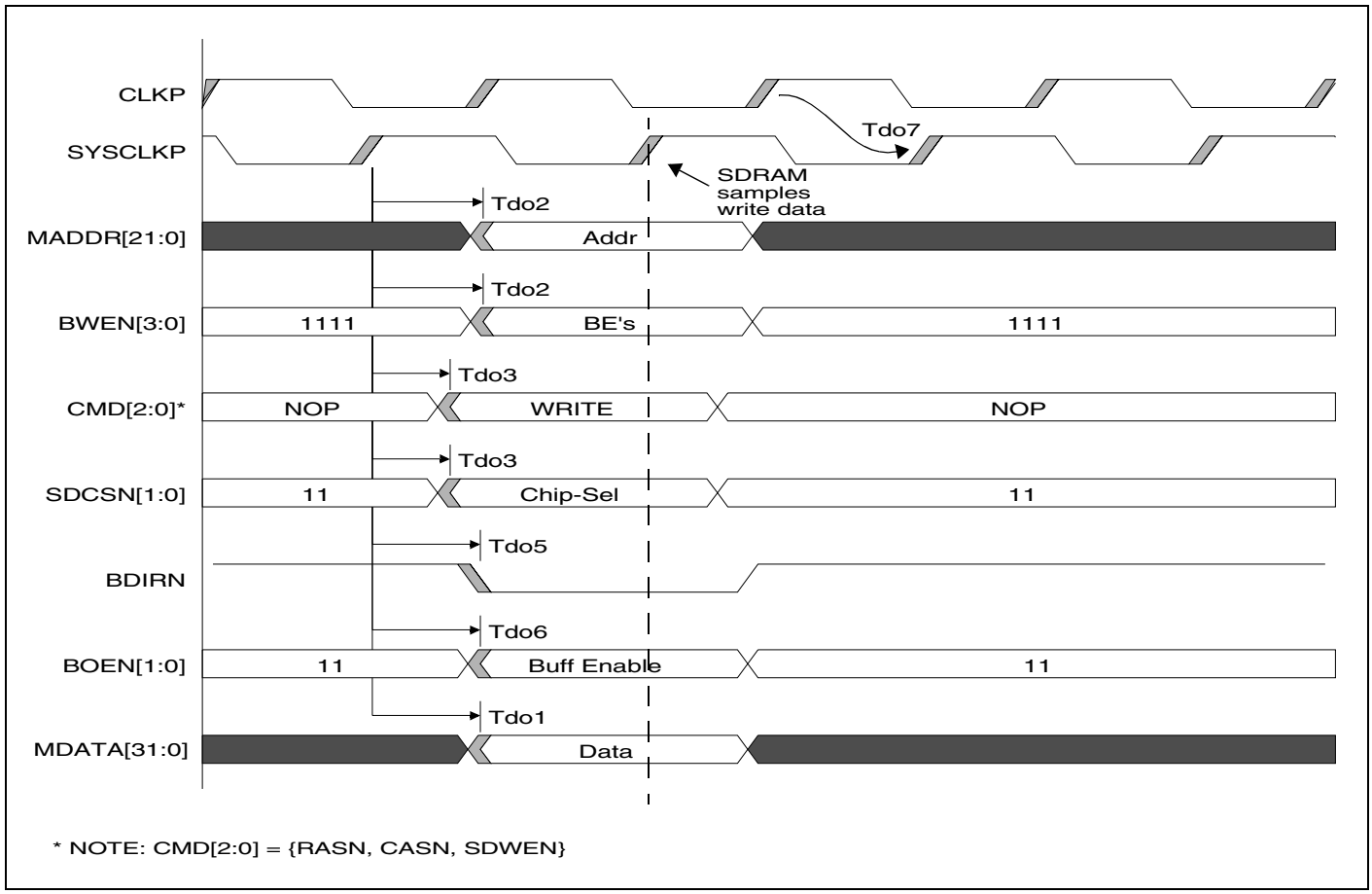


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
ATM Interface, Utopia Mode[1, 2]											
RXCLKP, TXCLKP[1]	Tperiod1	none	—	40	—	40	—	40	ns	25 MHz Utopia	Figure 14
	Thigh1,Tlow1		16	—	16	—	16	—	ns		
	Trise1,Tfall1		—	4	—	4	—	4	ns		
RXCLKP, TXCLKP[1]	Tperiod1	none	—	30	—	30	—	30	ns	33 MHz Utopia	
	Thigh1,Tlow1		12	—	12	—	12	—	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
RXCLKP, TXCLKP	Tperiod1	none	—	20	—	20	—	20	ns	50 MHz Utopia	
	Thigh,Tlow1		8	—	8	—	8	—	ns		
	Trise1,Tfall1		—	2	—	2	—	2	ns		
TXFULLN	Tsu2	TXCLKP rising	2	—	2	—	2	—	ns		
	Thld2		2	—	2	—	2	—	ns		
TXDATA[7:0], TXSOC, TXENBN, TXADDR[1:0]	Tdo3	TXCLKP rising	4	8	4	8	4	8	ns		
RXDATA[7:0], RXEMP-TYN, RXSOC	Tsu4	RXCLKP rising	3	—	3	—	3	—	ns		
	Thld4		2	—	2	—	2	—	ns		
RXADDR[1:0], RXENBN	Tdo5	RXCLKP rising	3	8	3	8	3	8	ns		

Table 8 ATM AC Timing Characteristics

1. ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

2. All Utopia Mode pins are multiplexed on the ATM interface pins as described in Table 9.

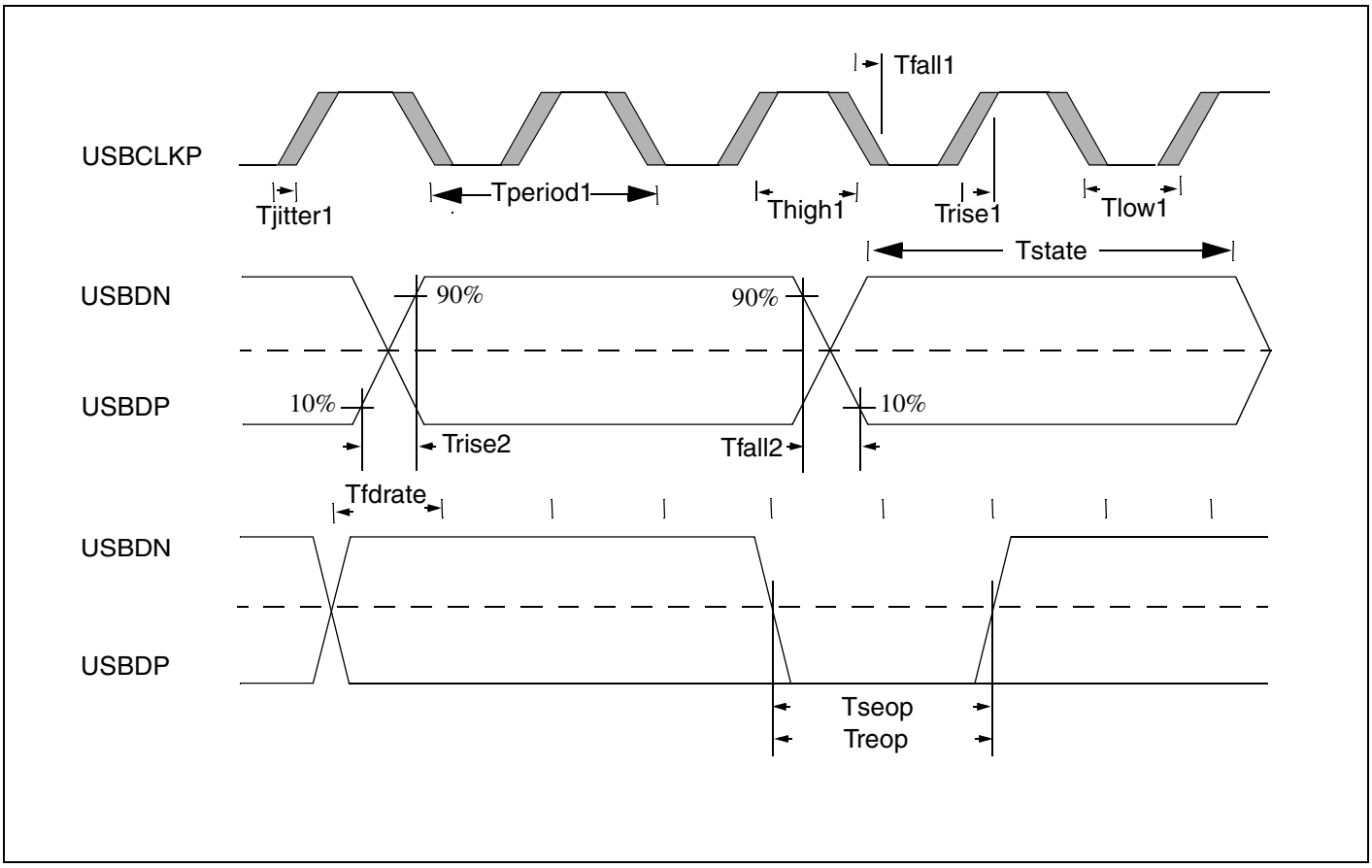


Figure 17 USB AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
UART											
U0SINP, U0RIN, U0DCDN, U0DSRN, U0CTSN, U1SINP, U1DSRN, U1CTSN	Tsu[1]	CLKP rising	5	—	5	—	5	—	ns		
	Thld[1]		3	—	3	—	3	—	ns		
U0SOUTP, U0DTRN, U0RTSN, U1SOUTP, U1DTRN, U1RTSN	Tdo[1]	CLKP rising	1	12	1	12	1	12	ns		
[1] These are asynchronous signals and the values are provided for ATE (test) only.											

Table 12 UART AC Timing Characteristics

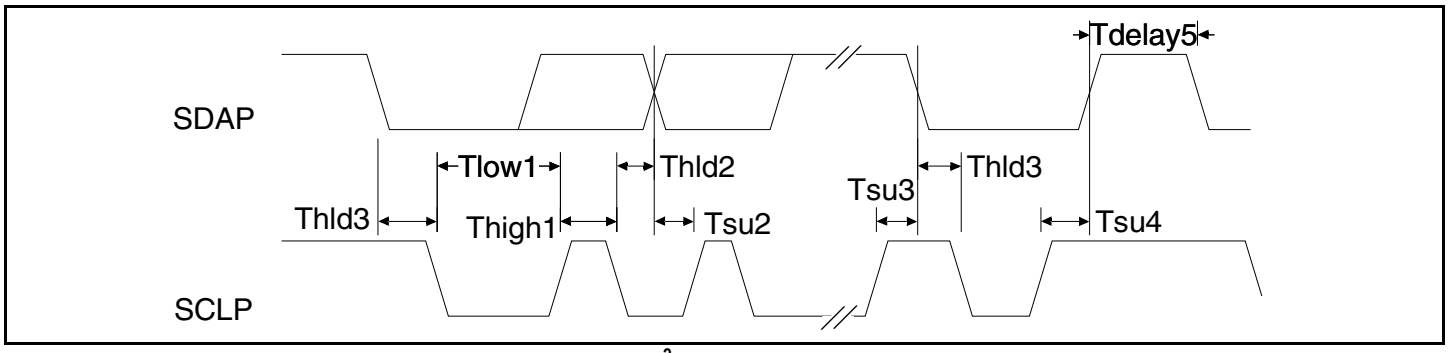


Figure 18 I^2C AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
GPIOP											
GPIOP[31:0][1]	Tsu1	CLKP rising	4	—	4	—	4	—	ns		Figure 19
	Thld1		1.4	—	1.4	—	1.4	—	ns		
	Tdo1		2	8	2	8	2	8	ns		
GPIOP[35:32][2]	Tsu1		3	—	3	—	3	—	ns		
	Thld1		1	—	1	—	1	—	ns		
	Tdo1		3	8	3	8	3	8	ns		

[1] GPIOP[31:0] are controlled through the GPIO interface. GPIO[31:0] are asynchronous signals, the values are provided for ATE (test) only.
[2] GPIOP[35:32] are controlled through the TDM interface.

Table 14 GPIOP AC Timing Characteristics

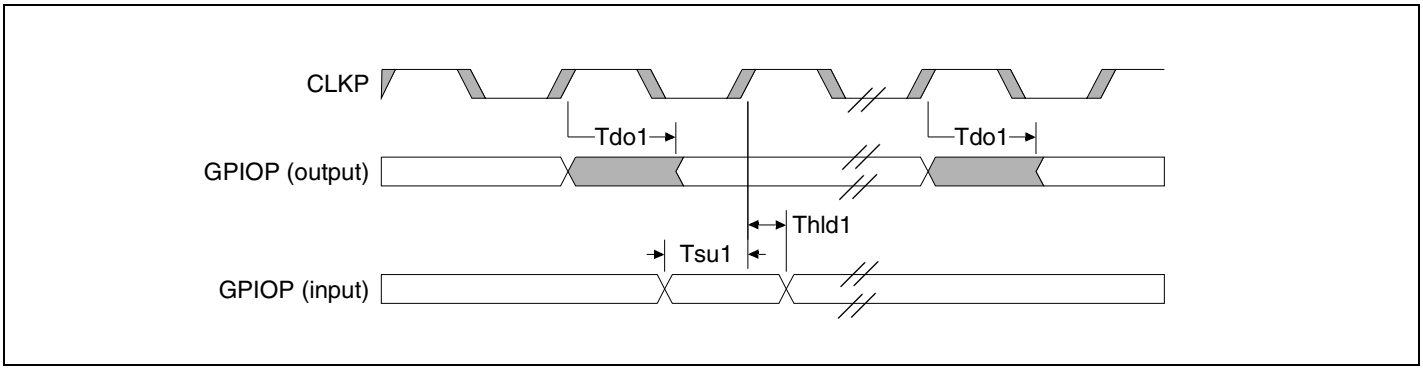


Figure 19 GPIOP AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
EJTAG and JTAG											
JTAG_TCK	Tperiod1	none	100	—	100	—	100	—	ns		Figure 20
	Thigh1, Tlow1		40	—	40	—	40	—	ns		
	Trise1, Tfall1		—	5	—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	7.5	10.0	6.7	10.0	5.6	10.0	ns		
	Thigh2, Tlow2		2.5	—	2.5	—	2.5	—	ns		
	Trise2, Tfall2		—	3.5	—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2	12.0	2	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 15 JTAG AC Timing Characteristics

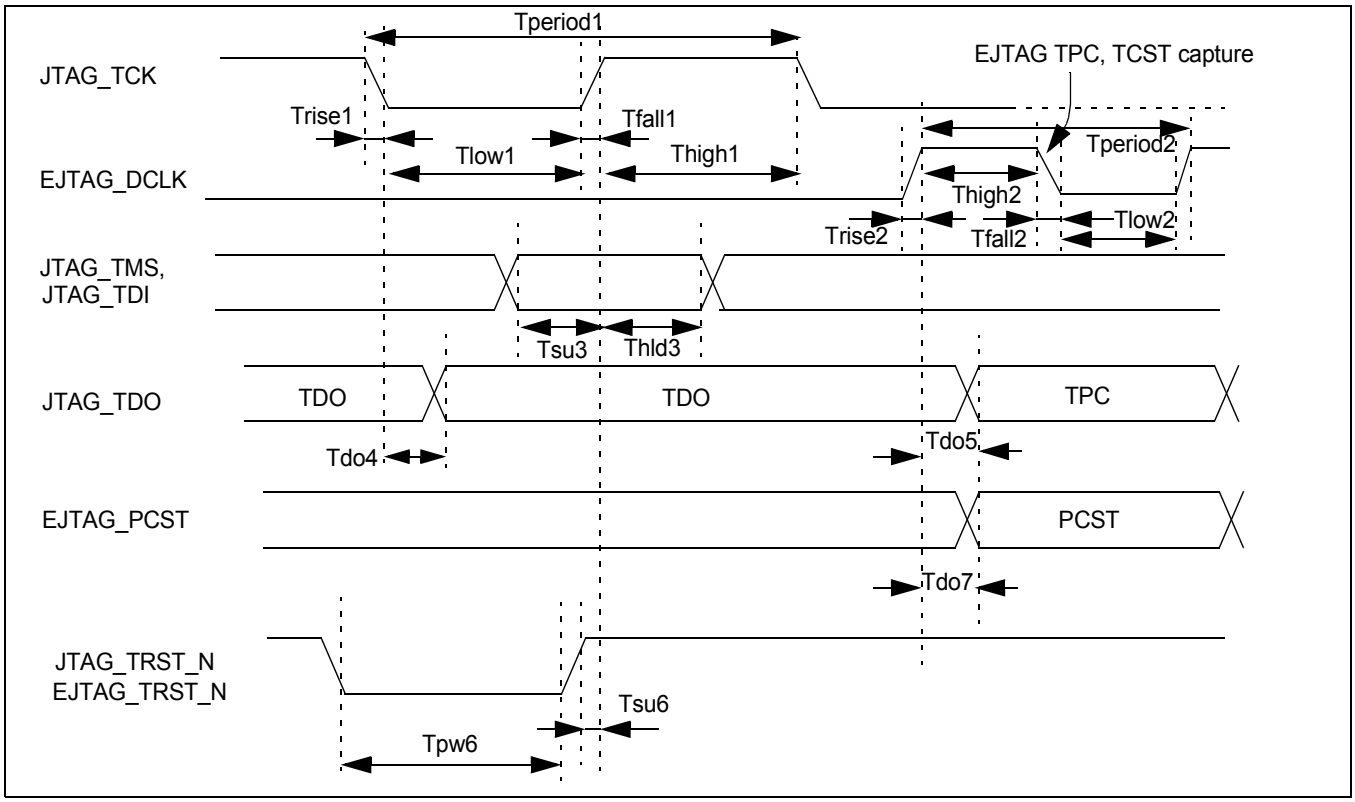


Figure 20 JTAG AC Timing Waveform

Table 16 shows the pin numbering for the Standard EJTAG connector. All the even numbered pins are connected to ground. Multiplexing of pin functions should be considered when connecting EJTAG_TRST_N and EJTAG_PCST.

For details on using the JTAG connector, see the JTAG chapters in the RC32355 user reference manual.

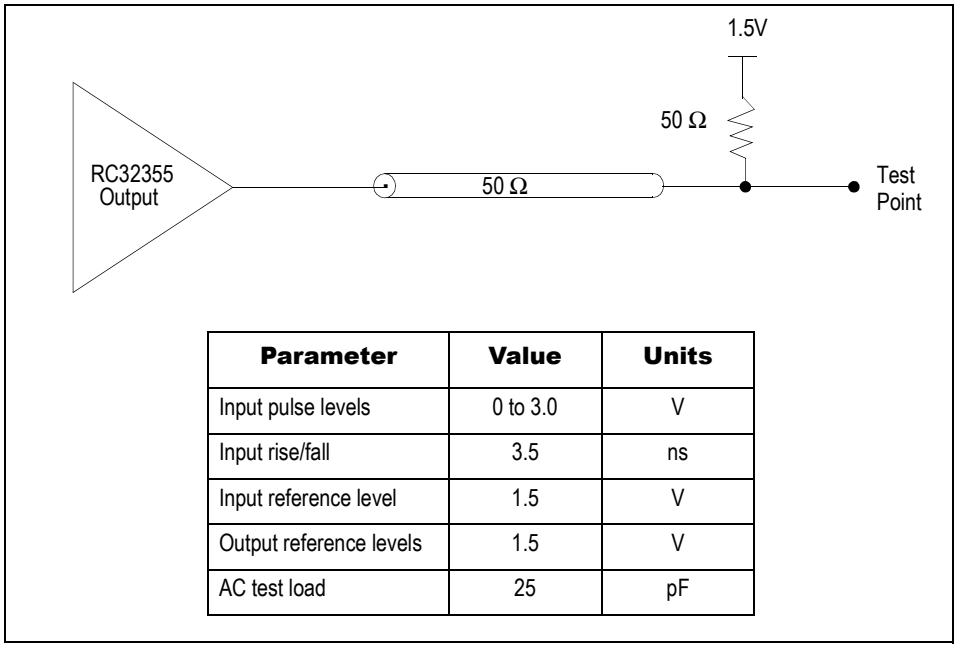
PIN	SIGNAL	RC32355 I/O	TERMINATION[1]
1	EJTAG_TRST_N	Input	10 kΩ pull-down resistor. A pull-down resistor will hold the EJTAG controller in reset when not in use if the EJTAG_TRST_N function is selected with the boot configuration vector. Refer to the User Manual.
3	JTAG_TDI	Input	10 kΩ pull-up resistor
5	JTAG_TDO	Output	33 Ω series resistor
7	JTAG_TMS	Input	10 kΩ pull-up resistor
9	JTAG_TCK	Input	10 kΩ pull-up resistor[2]
11	System Reset	Input	10 kΩ pull-up resistor is used if it is combined with the system cold reset control, COLDRSTN.
13	EJTAG_PCST[0]	Output	33 Ω series resistor
15	EJTAG_PCST[1]	Output	33 Ω series resistor
17	EJTAG_PCST[2]	Output	33 Ω series resistor
19	EJTAG_DCLK	Output	33 Ω series resistor
21	Debug Boot	Input	This can be connected to the boot configuration vector to control debug boot mode if desired. Refer to Table 2 on page 12 and the RC32355 user reference manual.
23	VccI/O	Output	Used to sense the circuit board power. Must be connected to the VCC I/O supply of the circuit board.

Table 16 Pin Numbering of the JTAG and EJTAG Target Connector

1. The value of the series resistor may depend on the actual printed circuit board layout situation.

2. JTAG_TCK pull-up resistor is not required according to the JTAG (IEEE1149) standard. It is indicated here to prevent a floating CMOS input when the EJTAG connector is unconnected.

AC Test Conditions



Parameter	Value	Units
Input pulse levels	0 to 3.0	V
Input rise/fall	3.5	ns
Input reference level	1.5	V
Output reference levels	1.5	V
AC test load	25	pF

Figure 21 Output Loading for AC Timing

Phase-Locked Loop (PLL)

The processor aligns the pipeline clock, PClock, to the master input clock (CLKP) by using an internal phase-locked loop (PLL) circuit that generates aligned clocks. Inherently, PLL circuits are only capable of generating aligned clocks for master input clock (CLKP) frequencies within a limited range.

PLL Analog Filter

The storage capacitor required for the Phase-Locked Loop circuit is contained in the RC32355. However, it is recommended that the system designer provide a filter network of passive components for the PLL power supply.

VccP (PLL circuit power) and VssP (PLL circuit ground) should be isolated from Vcc Core (core power) and Vss (common ground) with a filter circuit such as the one shown in Figure 22.

Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

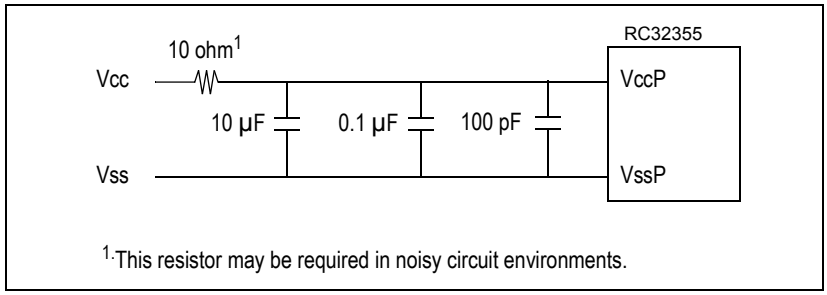


Figure 22 PLL Filter Circuit for Noisy Environments

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V_{ss}[1] V_{ssP}[5]	$V_{cc}I/O$[2]	$V_{cc}Core$[3] $V_{cc}P$[4]
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%
Industrial	-40°C+ 85°C Ambient	0V	3.3V±5%	2.5V±5%

[1] Vss supplies a common ground.
[2] VccI/O is the I/O power.
[3] VccCore is the internal logic power.
[4] VccP is the phase lock loop power.
[5] VssP is the phase lock loop ground.

Table 17 Temperature and Voltage

Capacitive Load Deration

Refer to the RC32355 IBIS Model which can be found at the IDT web site (www.idt.com).

USB Electrical Characteristics

	Parameter	Min	Max	Unit	Conditions
USB Interface					
V_{di}	Differential Input Sensitivity	-0.2		V	I(D+)-(D-)I
V_{cm}	Differential Input Common Mode Range	0.8	2.5	V	
V_{se}	Single ended Receiver Threshold	0.8	2.0	V	
C_{in}	Transceiver Capacitance		20	pF	
I_{li}	Hi-Z State Data Line Leakage	-10	10	µA	$0V < V_{in} < 3.3V$
USB Upstream/Downstream Port					
V_{oh}	Static Output High	2.8	3.6	V	15km ± 5% to Gnd
V_{ol}	Static Output Low		0.3	V	
Z_o	USB Driver Output Impedance	28	44	Ω	Including $R_{ext} = 20\ \Omega$

Table 19 USB Interface Characteristics

Power Consumption

Note: This table is based on a 2:1 CPU pipeline to system (PClock to CLKP) clock ratio.

Parameter		133MHz		150MHz		180MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC} I/O		80	130	100	150	120	170	mA	
$I_{CC\ core}$	Normal mode	400	450	450	500	500	550	mA	C_L = 25pF (affects I/O) $T_a = 25^oC$ VccP = 2.625V (for max. values) V_{cc} core = 2.625V (for max. values) V_{cc} I/O = 3.46V (for max. values) VccP = 2.5V (for typical values) V_{cc} core = 2.5V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	320	370	360	410	400	450	mA	
Power Dissipation	Normal mode	1.26	1.63	1.46	1.86	1.73	2.03	W	
	Standby mode[1]	1.06	1.42	1.22	1.59	1.47	1.77	W	

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions; however, other logic continues to function. Standby mode reduces power consumption by 0.6 mA per MHz of the CPU pipeline clock, PClock.

Table 20 RC32355 Power Consumption

Power Curve

The following graph contains a power curve that shows power consumption at various bus frequencies.

Note: The system clock (CLKP) can be multiplied by 2, 3, or 4 to obtain the CPU pipeline clock (PClock) speed.

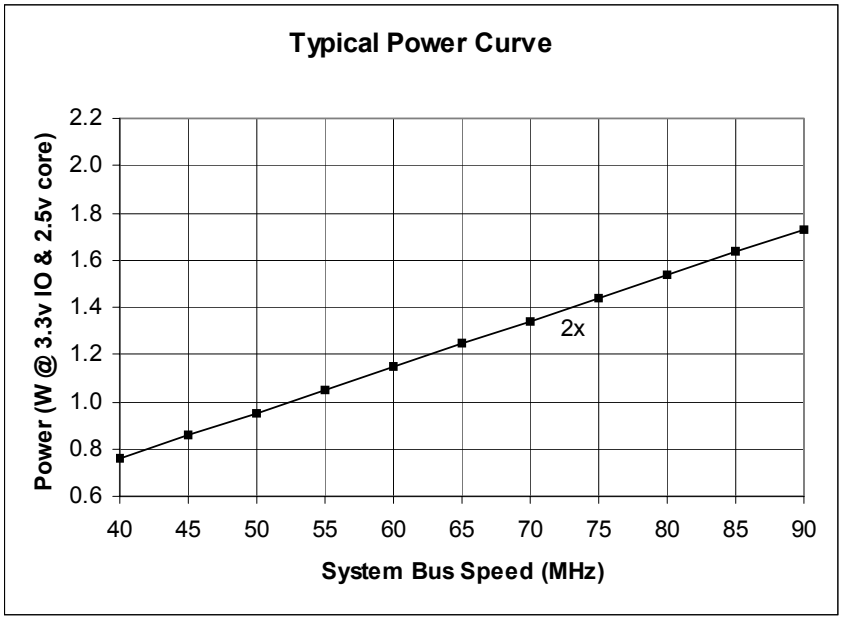


Figure 23 Typical Power Usage

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O Supply Voltage	-0.3	3.465	V
V_{CC}Core	Core Supply Voltage	-0.3	3.0	V
V_{CC}P	PLL Supply Voltage	-0.3	3.0	V
Vimin	Input Voltage - undershoot	-0.6	—	V
Vi	I/O Input Voltage	Gnd	V_{CC}I/O+0.6	V
Ta, Industrial	Ambient Operating Temperature	-40	85	degrees C
Tstg	Storage Temperature	-40	125	degrees C

Table 21 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 17. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Package Pin-out — 208-Pin PQFP

The following table lists the pin numbers and signal names for the RC32355.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	ATMOUTP[0]		53	JTAG_TDO		105	BGN		157	MDATA[28]	
2	ATMOUTP[1]		54	GPIOP[16]	1	106	CSN[0]		158	MDATA[13]	
3	ATMINP[02]		55	GPIOP[17]	1	107	CSN[1]		159	MDATA[29]	
4	ATMOUTP[2]		56	GPIOP[18]	1	108	CSN[2]		160	Vcc I/O	
5	Vss		57	Vss		109	Vcc I/O		161	MDATA[14]	
6	ATMOUTP[3]		58	JTAG_TCK		110	CSN[3]		162	Vss	
7	ATMINP[03]		59	GPIOP[19]	1	111	Vss		163	MDATA[30]	
8	ATMOUTP[4]		60	GPIOP[20]	1	112	OEN		164	MDATA[15]	
9	Vcc I/O		61	Vcc I/O		113	RWN		165	MDATA[31]	
10	ATMOUTP[5]		62	GPIOP[21]	1	114	BDIRN		166	CLKP	
11	ATMINP[04]		63	JTAG_TDI		115	BOEN[0]		167	WAITACKN	
12	ATMOUTP[6]		64	GPIOP[22]	1	116	BOEN[1]		168	MADDR[00]	
13	ATMOUTP[7]		65	GPIOP[23]	2	117	BWEN[0]		169	MADDR[11]	
14	ATMINP[05]		66	GPIOP[24]	1	118	Vcc I/O		170	MADDR[01]	
15	ATMOUTP[8]		67	JTAG_TMS		119	BWEN[1]		171	Vcc I/O	
16	ATMOUTP[9]		68	GPIOP[25]	2	120	Vss		172	MADDR[12]	
17	Vss		69	GPIOP[26]	1	121	BWEN[2]		173	Vss	
18	ATMINP[06]		70	Vss		122	Vcc Core		174	MADDR[02]	
19	Vcc Core		71	GPIOP[27]	1	123	BWEN[3]		175	MADDR[13]	
20	GPIOP[00]	1	72	COLDRSTN		124	MDATA[00]		176	MADDR[03]	
21	GPIOP[01]	1	73	GPIOP[28]	1	125	MDATA[16]		177	MADDR[14]	
22	ATMINP[07]		74	GPIOP[29]	1	126	MDATA[01]		178	MADDR[04]	
23	GPIOP[02]	2	75	GPIOP[30]	1	127	MDATA[17]		179	MADDR[15]	
24	GPIOP[03]	1	76	GPIOP[31]	2	128	MDATA[02]		180	Vcc I/O	
25	ATMINP[08]		77	USBCLKP		129	Vcc I/O		181	MADDR[05]	
26	Vcc I/O		78	Vcc I/O		130	MDATA[18]		182	Vcc Core	
27	GPIOP[04]	2	79	USBDN		131	Vss		183	SYSCLKP	
28	GPIOP[05]	1	80	USBDP		132	MDATA[03]		184	Vss	
29	ATMINP[09]		81	Vss		133	MDATA[19]		185	MADDR[16]	
30	VccP[1]		82	MIICRSP		134	MDATA[04]		186	MADDR[06]	
31	VssP[1]		83	MIICOLP		135	MDATA[20]		187	MADDR[17]	
32	ATMINP[10]		84	MIITXDP[0]		136	MDATA[05]		188	MADDR[07]	
33	GPIOP[06]	1	85	MIITXDP[1]		137	MDATA[21]		189	MADDR[18]	
34	Vss		86	Vcc Core		138	Vcc Core		190	MADDR[08]	

Table 22: 208-pin QFP Package Pin-Out (Part 1 of 2)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
35	GPIOP[07]	1	87	MIITXDP[2]		139	MDATA[06]		191	Vcc I/O	
36	ATMINP [11]		88	MIITXDP[3]		140	Vcc I/O		192	MADDR[19]	
37	GPIOP[08]	2	89	MIITXENP		141	MDATA[22]		193	Vss	
38	Vcc Core		90	MIITXCLKP		142	Vss		194	MADDR[09]	
39	GPIOP[09]	2	91	MIITXERP		143	MDATA[07]		195	MADDR[20]	
40	GPIOP[10]	2	92	MIIRXERP		144	MDATA[23]		196	MADDR[10]	
41	GPIOP[11]	2	93	MIIRXCLKP		145	SDCLKINP		197	MADDR[21]	
42	GPIOP[12]	2	94	MIIRXDVP		146	MDATA[08]		198	CASN	
43	Vcc I/O		95	Vcc I/O		147	MDATA[24]		199	RASN	
44	GPIOP[13]	2	96	MIIRXDP[0]		148	MDATA[09]		200	SDWEN	
45	Vss		97	MIIRXDP[1]		149	MDATA[25]		201	Vcc I/O	
46	GPIOP[14]	1	98	MIIRXDP[2]		150	MDATA[10]		202	SDCSN[0]	
47	GPIOP[15]	1	99	MIIRXDP[3]		151	Vcc I/O		203	Vss	
48	GPIOP[35]	1	100	Vss		152	MDATA[26]		204	SDCSN[1]	
49	GPIOP[34]	1	101	MIIDCP		153	Vss		205	ATMINP[00]	
50	GPIOP[33]	1	102	MIIDIOP		154	MDATA[11]		206	ATMIOP[0]	
51	GPIOP[32]	1	103	RSTN		155	MDATA[27]		207	ATMIOP[1]	
52	INSTP		104	BRN		156	MDATA[12]		208	ATMINP[01]	

[1] VccP and VssP are the Phase Lock Loop (PLL) power and ground. PLL power and ground should be supplied through a special filter circuit.

Table 22: 208-pin QFP Package Pin-Out (Part 2 of 2)

Alternate Pin Functions

Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		51	GPIOP[32]	TDMDOP	
21	GPIOP[01]	U0SINP		54	GPIOP[16]	CSN[4]	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	55	GPIOP[17]	CSN[5]	
24	GPIOP[03]	U0DCRN		56	GPIOP[18]	DMAREQN	
27	GPIOP[04]	U0DTRN	CPUP	59	GPIOP[19]	DMADONEN	
28	GPIOP[05]	U0DSRN		60	GPIOP[20]	USBSOF	
33	GPIOP[06]	U0RTSN		62	GPIOP[21]	CKENP	
35	GPIOP[07]	U0CTSN		64	GPIOP[22]	TXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	65	GPIOP[23]	TXADDR[1]	DMAP[0]
39	GPIOP[09]	U1SINP	DMAP[2]	66	GPIOP[24]	RXADDR[0]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	69	GPIOP[26]	TDMTEN	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	71	GPIOP[27]	MADDR[22]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	73	GPIOP[28]	MADDR[23]	
46	GPIOP[14]	SDAP		74	GPIOP[29]	MADDR[24]	
47	GPIOP[15]	SCLP		75	GPIOP[30]	MADDR[25]	
48	GPIOP[35]	TDMCLKP		76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
49	GPIOP[34]	TDMFP					
50	GPIOP[33]	TDMDIP					

Table 23 Alternate Pin Functions

Package Drawing - page two