Renesas Electronics America Inc - IDT79RC32T355-133DHG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t355-133dhg

Device Overview

The RC32355 is a “System on a Chip” which contains a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

The RC32355 meets the requirements of various embedded communications and digital consumer applications. It is a single chip solution that incorporates most of the generic system functionalities and application specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

CPU Execution Core

The RC32355 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The DSP instructions enable the RC32300 to implement 33.6 and 56kbps modem functionality in software, removing the need for external dedicated hardware. Cache locking guarantees real-time performance by holding critical DSP code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

Memory and I/O Controller

The RC32355 incorporates a flexible memory and peripheral device controller providing support for SDRAM, Flash ROM, SRAM, dual-port memory, and other I/O devices. It can interface directly to 8-bit boot ROM for a very low cost system implementation. It enables access to very high bandwidth external memory (380 MB/sec peak) at very low system costs. It also offers various trade-offs in cost / performance for the main memory architecture. The timers implemented on the RC32355 satisfy the requirements of most RTOS.

DMA Controller

The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The DMA controller supports scatter / gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

TDM Bus Interface

The RC32355 incorporates an industry standard TDM bus interface to directly access external devices such as telephone CODECs and quality audio A/Ds and D/As. This feature is critical for applications, such as cable modems and xDSL modems, that need to carry voice along with data to support Voice Over IP capability.

Ethernet Interface

The RC32355 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line interface with an MII interface. It supports up to 4 MAC addresses. In a SOHO router, the high performance RC32300 CPU core routes the data between the Ethernet and the ATM interface. In other applications, such as high speed modems, the Ethernet interface can be used to connect to the PC.

USB Device Interface

The RC32355 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC.

ATM SAR

The RC32355 includes a configurable ATM SAR that supports a UTOPIA level 1 or a UTOPIA level 2 interface. The ATM SAR is implemented as a hybrid between software and hardware. A hardware block provides the necessary low level blocks (like CRC generation and checking and cell buffering) while the software is used for higher level SARing functions. In xDSL modem applications, the UTOPIA port interfaces directly to an xDSL chip set. In SOHO routers or in a line card for a Layer 3 switch, it provides access to an ATM network.

Enhanced JTAG Interface for ICE

For low-cost In-Circuit Emulation (ICE), the RC32300 CPU core includes an Enhanced JTAG (EJTAG) interface. This interface consists of two operation modes: Run-Time Mode and Real-Time Mode.

The Run-Time Mode provides a standard JTAG interface for on-chip debugging, and the Real-Time Mode provides additional status pins—PCST[2:0]—which are used in conjunction with the JTAG pins for real-time trace information at the processor internal clock or any division of the pipeline clock.

Pin Description Table

The following table lists the functions of the pins provided on the RC32355. Some of the functions listed may be multiplexed onto the same pin.

To define the active polarity of a signal, a suffix will be used. Signals ending with an "N" should be interpreted as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level.

Note: The input pads of the RC32355 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as BRN) which, if left floating, could adversely affect the RC32355's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Name	Type	I/O Type	Description
System			
CLKP	I	Input	**System Clock input.** This is the system master clock input. The RISCore 32300 pipeline frequency is a multiple (x2, x3, or x4) of this clock frequency. All other logic runs at this frequency or less.
COLDRSTN	I	STI[1]	**Cold Reset.** The assertion of this signal low initiates a cold reset. This causes the RC32355 state to be initialized, boot configuration to be loaded, and the internal processor PLL to lock onto the system clock (CLKP).
RSTN	I/O	Low Drive with STI	**Reset.** This bidirectional signal is either driven low or tri-stated, an external pull-up is required to supply the high state. The RC32355 drives RSTN low during a reset (to inform the external system that a reset is taking place) and then tri-states it. The external system can drive RSTN low to initiate a warm reset, and then should tri-state it.
SYSCLKP	O	High Drive	**System clock output.** This is a buffered and delayed version of the system clock input (CLKP). All SDRAM transactions are synchronous to this clock. This pin should be externally connected to the SDRAMs and to the RC32355 SDCLKINP pin (SDRAM clock input).
Memory and Peripheral Bus			
MADDR[25:0]	O	[21:0] High Drive [25:22] Low Drive with STI	**Memory Address Bus.** 26-bit address bus for memory and peripheral accesses. MADDR[20:17] are used for the SODIMM data mask enables if SODIMM mode is selected. MADDR[22] Primary function: General Purpose I/O, GPIOP[27]. MADDR[23] Primary function: General Purpose I/O, GPIOP[28]. MADDR[24] Primary function: General Purpose I/O, GPIOP[29]. MADDR[25] Primary function: General Purpose I/O, GPIOP[30].
MDATA[31:0]	I/O	High Drive	**Memory Data Bus.** 32-bit data bus for memory and peripheral accesses.
BDIRN	O	High Drive	**External Buffer Direction.** External transceiver direction control for the memory and peripheral data bus, MDATA[31:0]. It is asserted low during any read transaction, and remains high during write transactions.
BOEN[1:0]	O	High Drive	**External Buffer Output Enable.** These signals provide two output enable controls for external data bus transceivers on the memory and peripheral data bus, MDATA. BOEN[0] is asserted low during external device read transactions. BOEN[1] is asserted low during SDRAM read transactions.
BRN	I	STI	**External Bus Request.** This signal is asserted low by an external master device to request ownership of the memory and peripheral bus.
BGN	O	Low Drive	**External Bus Grant.** This signal is asserted low by RC32355 to indicate that RC32355 has relinquished ownership of the local memory and peripheral bus to an external master.
WAITACKN	I	STI	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted low during a memory and peripheral device bus transaction to extend the bus cycle. When configured as transfer acknowledge, this signal is asserted low during a memory and peripheral device bus transaction to signal the completion of the transaction.
CSN[5:0]	O	[3:0] High Drive [5:4] Low Drive	**Device Chip Select.** These signals are used to select an external device on the memory and peripheral bus during device transactions. Each bit is asserted low during an access to the selected external device. CSN[4] Primary function: General purpose I/O, GPIOP[16]. CSN[5] Primary function: General purpose I/O, GPIOP[17].

Table 1 Pin Descriptions (Part 1 of 8)

Name	Type	I/O Type	Description
RWN	O	High Drive	**Read or Write.** This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device, a low level indicates a write to an external device.
OEN	O	High Drive	**Output Enable.** This signal is asserted low when data should be driven by an external device during device read transactions on the memory and peripheral bus.
BWEN[3:0]	O	High Drive	**SDRAM Byte Enable Mask or Memory and I/O Byte Write Enables.** These signals are used as data input/output masks during SDRAM transactions and as byte write enable signals during device controller transactions on the memory and peripheral bus. They are active low. BWEN[0] corresponds to byte lane MDATA[7:0]. BWEN[1] corresponds to byte lane MDATA[15:8]. BWEN[2] corresponds to byte lane MDATA[23:16]. BWEN[3] corresponds to byte lane MDATA[31:24].
SDCSN[1:0]	O	High Drive	**SDRAM Chip Select.** These signals are used to select the SDRAM device on the memory and peripheral bus. Each bit is asserted low during an access to the selected SDRAM.
RASN	O	High Drive	**SDRAM Row Address Strobe**. The row address strobe asserted low during memory and peripheral bus SDRAM transactions.
CASN	O	High Drive	**SDRAM Column Address Strobe.** The column address strobe asserted low during memory and peripheral bus SDRAM transactions.
SDWEN	O	High Drive	**SDRAM Write Enable.** Asserted low during memory and peripheral bus SDRAM write transactions.
CKENP	O	Low Drive	**SDRAM Clock Enable.** Asserted high during active SDRAM clock cycles. Primary function: General Purpose I/O, GPIOP[21].
SDCLKINP	I	STI	**SDRAM Clock Input.** This clock input is a delayed version of SYSCLKP. SDRAM read data is sampled into the RC32355 on the rising edge of this clock.
ATM Interface			
ATMINP[11:0]	I	STI	**ATM PHY Inputs.** These pins are the inputs for the ATM interface.
ATMIOP[1:0]	I/O	Low Drive with STI	**ATM PHY Bidirectional Signals.** These pins are the bidirectional pins for the ATM interface.
ATMOUTP[9:0]	O	Low Drive	**ATM PHY Outputs.** These pins are the outputs for the ATM interface.
TXADDR[1:0]	O	Low Drive	**ATM Transmit Address [1:0]**. 2-bit address bus used for transmission in Utopia-2 mode. TXADDR[0] Primary function: General purpose I/O, GPIOP[22]. TXADDR[1] Primary function: General purpose I/O, GPIOP[23].
RXADDR[1:0]	O	Low Drive	**ATM Receive Address [1:0]**. 2-bit address bus for receiving in Utopia-2 mode. RXADDR[0] Primary function: General purpose I/O, GPIOP[24]. RXADDR[1] Primary function: General purpose I/O, GPIOP[25].
TDM Bus			
TDMDOP	O	High Drive	**TDM Serial Data Output.** Serial data is driven by the RC32355 on this signal during an active output time slot. During inactive time slots this signal is tri-stated. Primary function: General purpose I/O, GPIOP[32].
TDMDIP	I	STI	**TDM Serial Data Input.** Serial data is received by the RC32355 on this signal during active input time slots. Primary function: General purpose I/O, GPIOP[33].
TDMFP	I/O	High Drive	**TDM Frame Signal.** A transition on this signal, the active polarity of which is programmable, delineates the start of a new TDM bus frame. TDMFP is driven if the RC32355 is a master, and is received if it is a slave. Primary function: General purpose I/O, GPIOP[34].
TDMCLKP	I	STI	**TDM Clock.** This input clock controls the rate at which data is sent and received on the TDM bus. Primary function: General purpose I/O, GPIOP[35].

Table 1 Pin Descriptions (Part 2 of 8)

Name	Type	I/O Type	Description
TDMTEN	O	Low Drive	**TDM External Buffer Enable.** This signal controls an external tri-state buffer output enable connected to the TDM output data, TDMDOP. It is asserted low when the RC32355 is driving data on TDMDOP. Primary function: General Purpose I/O, GPIOP[26]
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
GPIOP[5]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data set ready, U0DSRN.
GPIOP[6]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 request to send, U0RTSN.
GPIOP[7]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 clear to send, U0CTSN.
GPIOP[8]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial output, U1SOUTP. 2nd Alternate function: Active DMA channel code, DMAP[3].
GPIOP[9]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial input, U1SINP. 2nd Alternate function: Active DMA channel code, DMAP[2].
GPIOP[10]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[0].
GPIOP[11]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data set ready, U1DSRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[1].
GPIOP[12]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 request to send, U1RTSN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[2].
GPIOP[13]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 clear to send, U1CTSN. 2nd Alternate function: ICE PC trace clock, EJTAG_DCLK.
GPIOP[14]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface data, SDAP.
GPIOP[15]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface clock, SCLP.
GPIOP[16]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[4].

Table 1 Pin Descriptions (Part 3 of 8)

Name	Type	I/O Type	Description
DMAREQN	I	STI	**External DMA Device Request**. The external DMA device asserts this pin low to request DMA service. Primary function: General purpose I/O, GPIOP[18]. At reset, this pin defaults to primary function GPIOP[18].
DMADONEN	I	STI	**External DMA Device Done**. The external DMA device asserts this signal low to inform the RC32355 that it is done with the current DMA transaction. Primary function: General purpose I/O, GPIOP[19]. At reset, this pin defaults to primary function GPIOP[19].
USB			
USBCLKP	I	STI	**USB Clock.** 48 MHz clock input used as time base for the USB interface.
USBDN	I/O	USB	**USB D- Data Line.** This is the negative differential USB data signal.
USBDP	I/O	USB	**USB D+ Data Line.** This is the positive differential USB data signal.
USBSOF	O	Low Drive	**USB start of frame.** Primary function: General Purpose I/O, GPIOP[20]. At reset, this pin defaults to primary function GPIOP[20].
Ethernet			
MIICOLP	I	STI	**MII Collision Detected.** This signal is asserted by the ethernet PHY when a collision is detected.
MIICRSP	I	STI	**MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MIIMDCP	O	Low Drive	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIOP	I/O	Low Drive with STI	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
MIIRXCLKP	I	STI	**MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MIIRXDP[3:0]	I	STI	**MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MIIRXDVP	I	STI	**MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MIIRXERP	I	STI	**MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MIITXCLKP	I	STI	**MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXDP[3:0]	O	Low Drive	**MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MIITXENP	O	Low Drive	**MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MIITXERP	O	Low Drive	**MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
I^2C			
SCLP	I/O	Low Drive with STI	**I^2C Interface Clock**. An external pull-up is required on SCLP, see the I^2C spec.[2] Primary function: General purpose I/O, GPIOP[15]. At reset, this pin defaults to primary function GPIOP[15].
SDAP	I/O	Low Drive with STI	**I^2C Interface Data Pin.** An external pull-up is required on SDAP, see the I^2C spec.[2] Primary function: General purpose I/O, GPIOP[14]. At reset, this pin defaults to primary function GPIOP[14].
EJTAG			
JTAG_TCK	I	STI	**JTAG Clock.** This is an input test clock, used to shift data into or out of the boundary scan logic. This signal requires an external resistor, listed in Table 16.
JTAG_TDI	I	STI	**JTAG Data Input.** This is the serial data shifted into the boundary scan logic. This signal requires an external resistor, listed in Table 16. This is also used to input EJTAG_DINTN during EJTAG/ICE mode. EJTAG_DINTN is an interrupt to switch the PC trace mode off.
JTAG_TDO	O	Low Drive	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic. When no data is being shifted out, this signal is tri-stated. This signal requires an external resistor, listed in Table 16. This is also used to output the EJTAG_TPC during EJTAG/ICE mode. EJTAG_TPC is the non-sequential program counter output.

Table 1 Pin Descriptions (Part 5 of 8)

Name	Type	I/O Type	Description
U1CTSN	I	STI	**UART channel 1 clear to send.** Primary function: General Purpose I/O, GPIOP[13]. At reset, this pin defaults to primary function GPIOP[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 8 of 8)

1. Schmitt Trigger Input.
2. 2I^2C - Bus Specification by Philips Semiconductors.

Boot Configuration Vector

The boot configuration vector is read into the RC32355 during cold reset. The vector defines parameters in the RC32355 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Signal	Name/Description
MDATA[2:0]	**Clock Multiplier**. This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	**Endian.** This bit specifies the endianness of RC32355. 0x0 - little endian 0x1 - big endian
MDATA[4]	**Reserved.** Must be set to 0.
MDATA[5]	**Debug Boot Mode**. When this bit is set, the RC32355 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	**Boot Device Width**. This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	**EJTAG/ICE Interface Enable**. When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIOP[31, 13:10] pins behaves as GPIOP 0x1 - GPIOP[31] pin behaves as EJTAG_TRST_N, GPIOP[12:10] pins behave as EJTAG_PCST[2:0], and GPIOP[13] pin behaves as EJTAG_DCLK
MDATA[9]	**Fast Reset**. When this bit is set, RC32355 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32355 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32355 drives RSTN for 64 clock cycles (test only)
MDATA[10]	**DMA Debug Enable**. When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIOP[8, 9, 25, 23] pins behave as GPIOP 0x1 - GPIOP[8, 9, 25, 23] pins behave as DMAP[3:0]

Table 2 Boot Configuration Vector Encoding (Part 1 of 2)

Logic Diagram

The following Logic Diagram shows the primary pin functions of the RC32355.

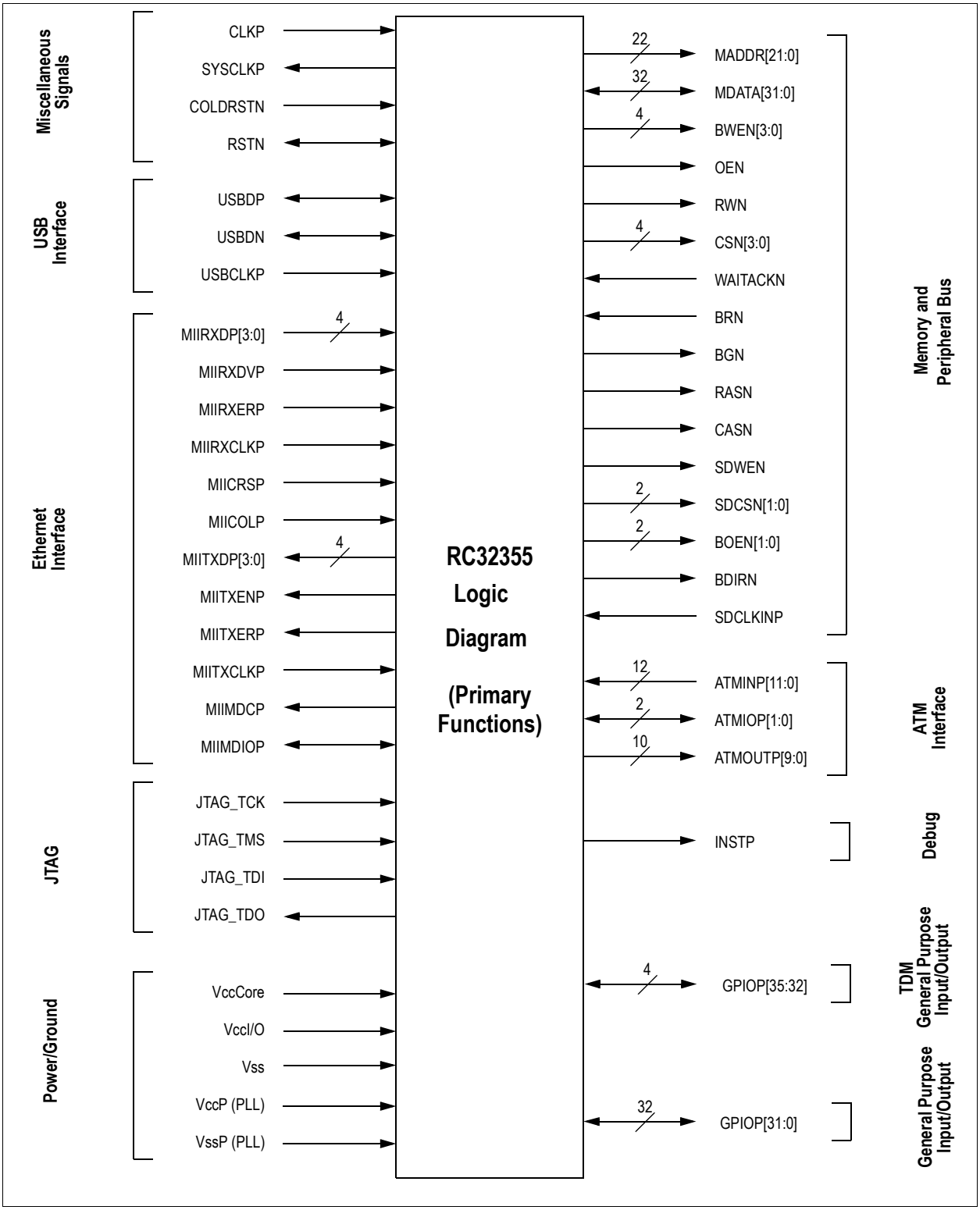


Figure 3 Logic Diagram

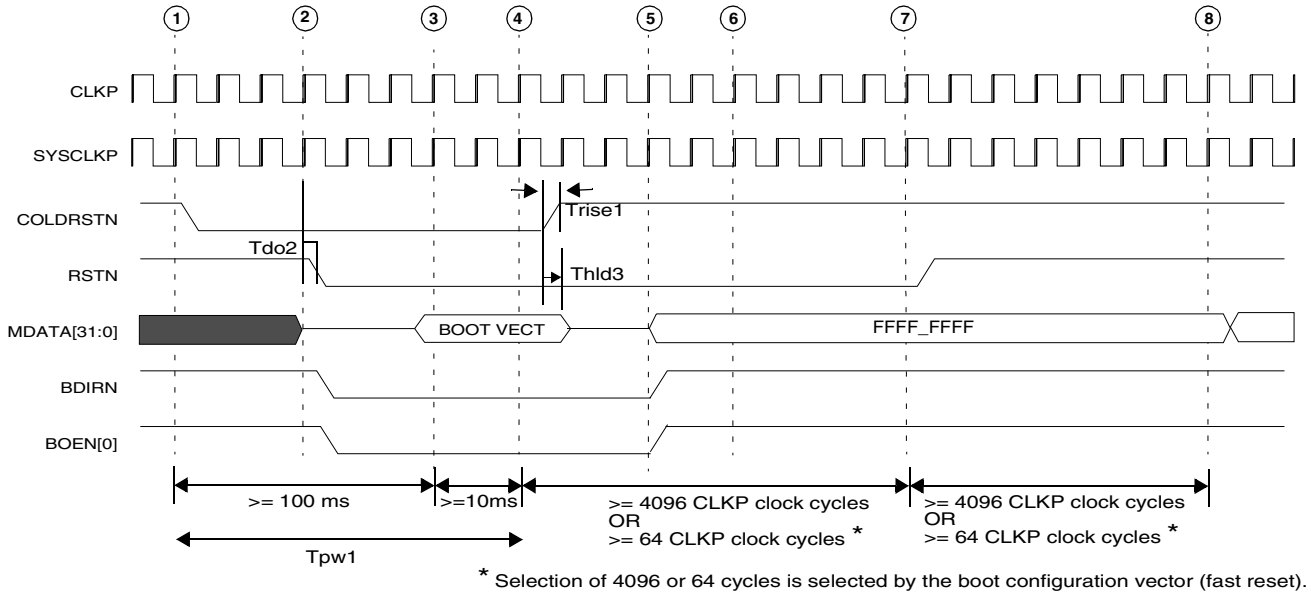
AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%,V_{cc} Core = +2.5V±5%, V_{cc}P = +2.5V±5%)

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Reset and System											
COLDRSTN	Tpw1	none	110	—	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	—	5.0	ns		
RSTN[1]	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5.0	8.0	5.0	8.0	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7.0	3.5	7.0	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	3.5	6.6	ns		
DMAREQN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	3.3	5.8	ns		

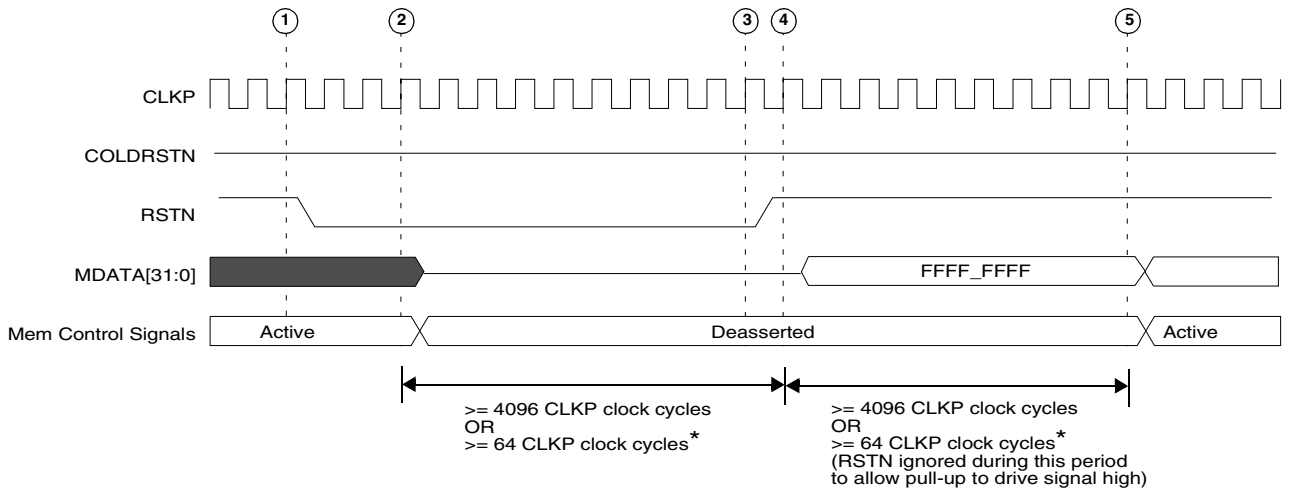
[1] RSTN is a bidirectional signal. It is treated as an asynchronous input.
[2] DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.

Table 5 Reset and System AC Timing Characteristics



1. COLDRSTN asserted by external logic.
2. The RC32355 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32355 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32355 stops sampling the boot configuration vector.
5. The RC32355 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLKP may be held constant after this point if Hold SYSCLKP Constant is selected in the boot configuration vector.
7. RSTN negated by RC32355.
8. CPU begins executing by taking MIPS reset exception, and the RC32355 starts sampling RSTN as a warm reset input.

Figure 6 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32355 asserts RSTN output low in response.
2. The RC32355 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32355 deasserts RSTN.
4. The RC32355 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

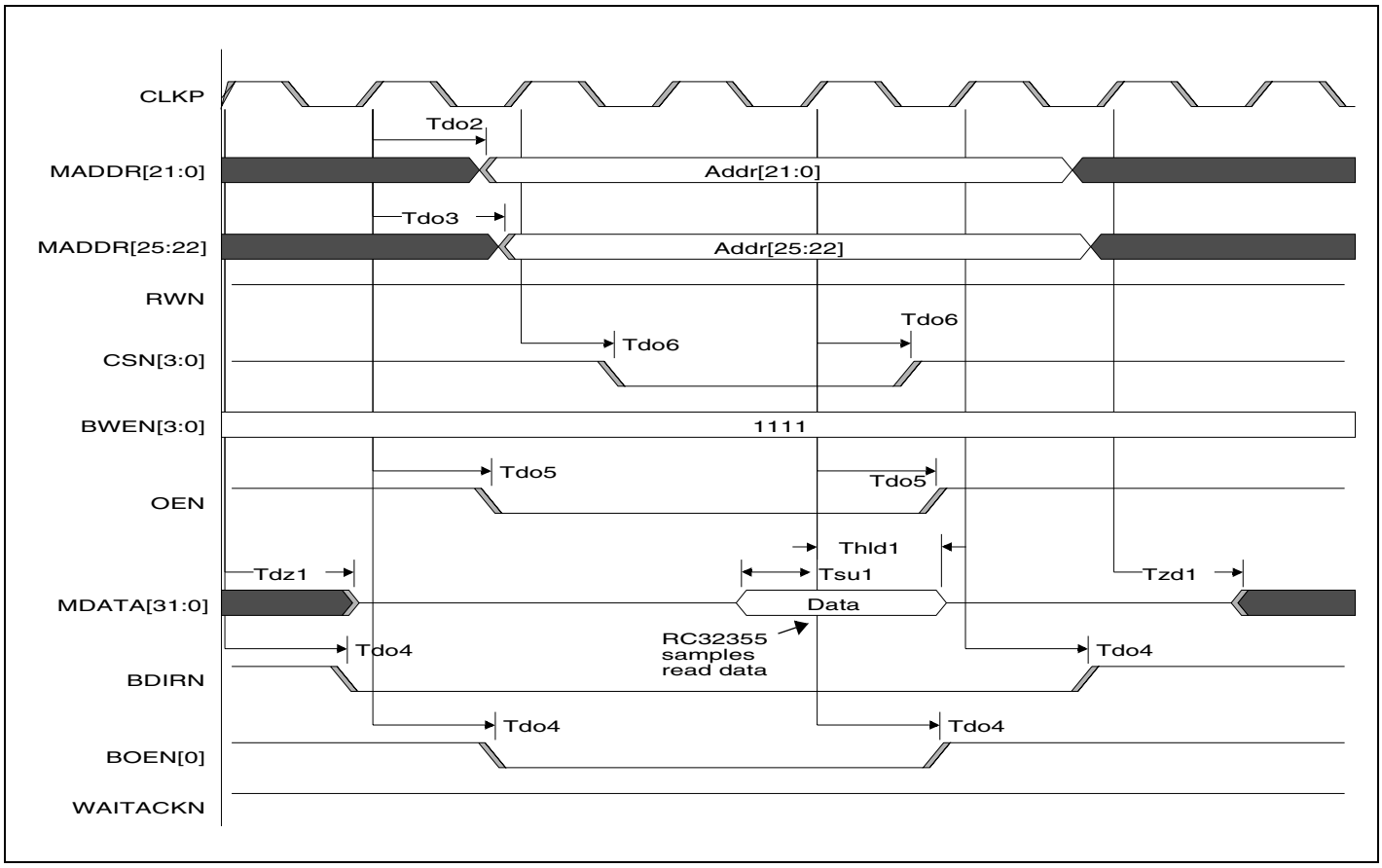


Figure 11 Memory and Peripheral Bus AC Timing Waveform - Device Read Access

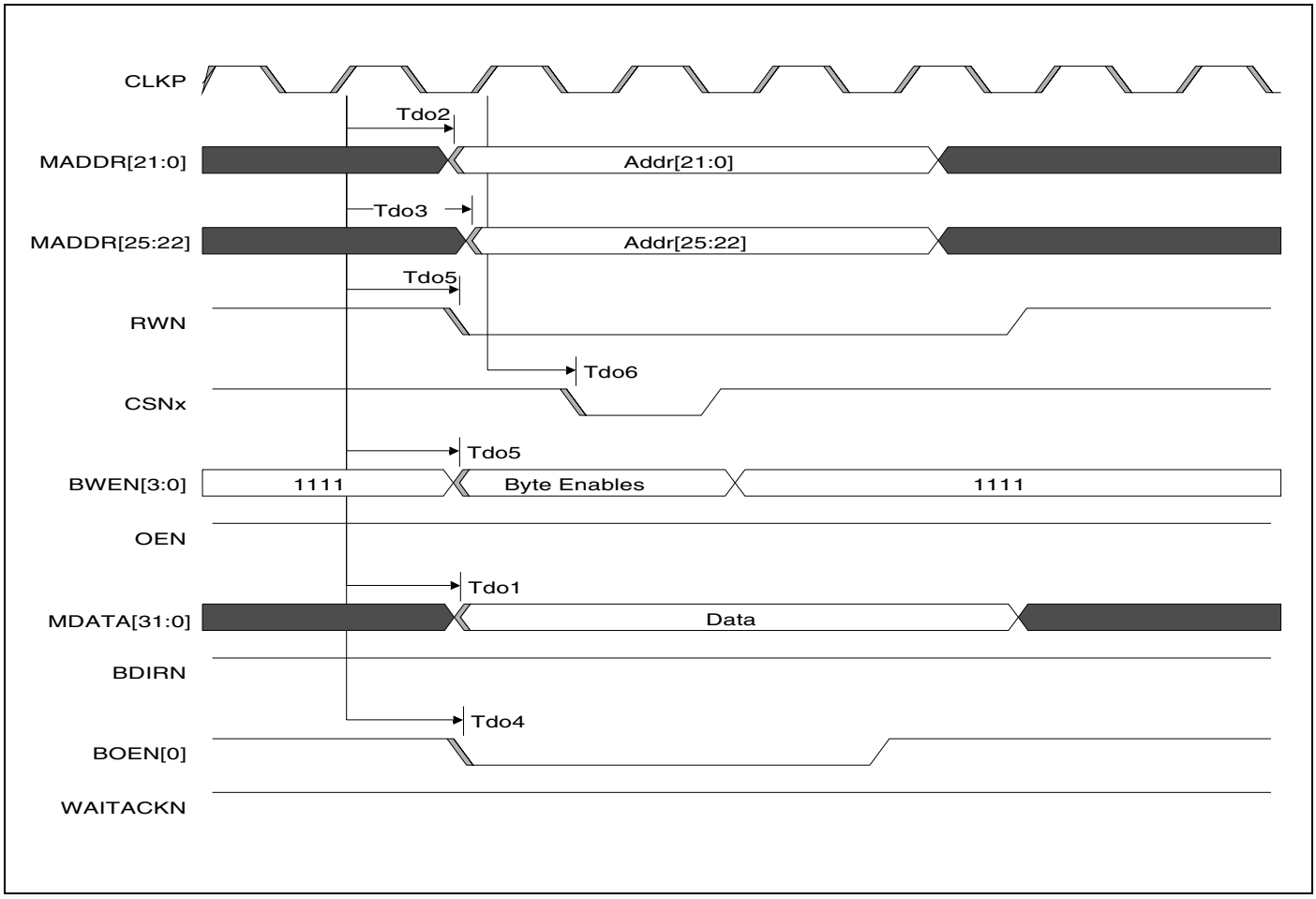


Figure 12 Memory AC and Peripheral Bus Timing Waveform - Device Write Access

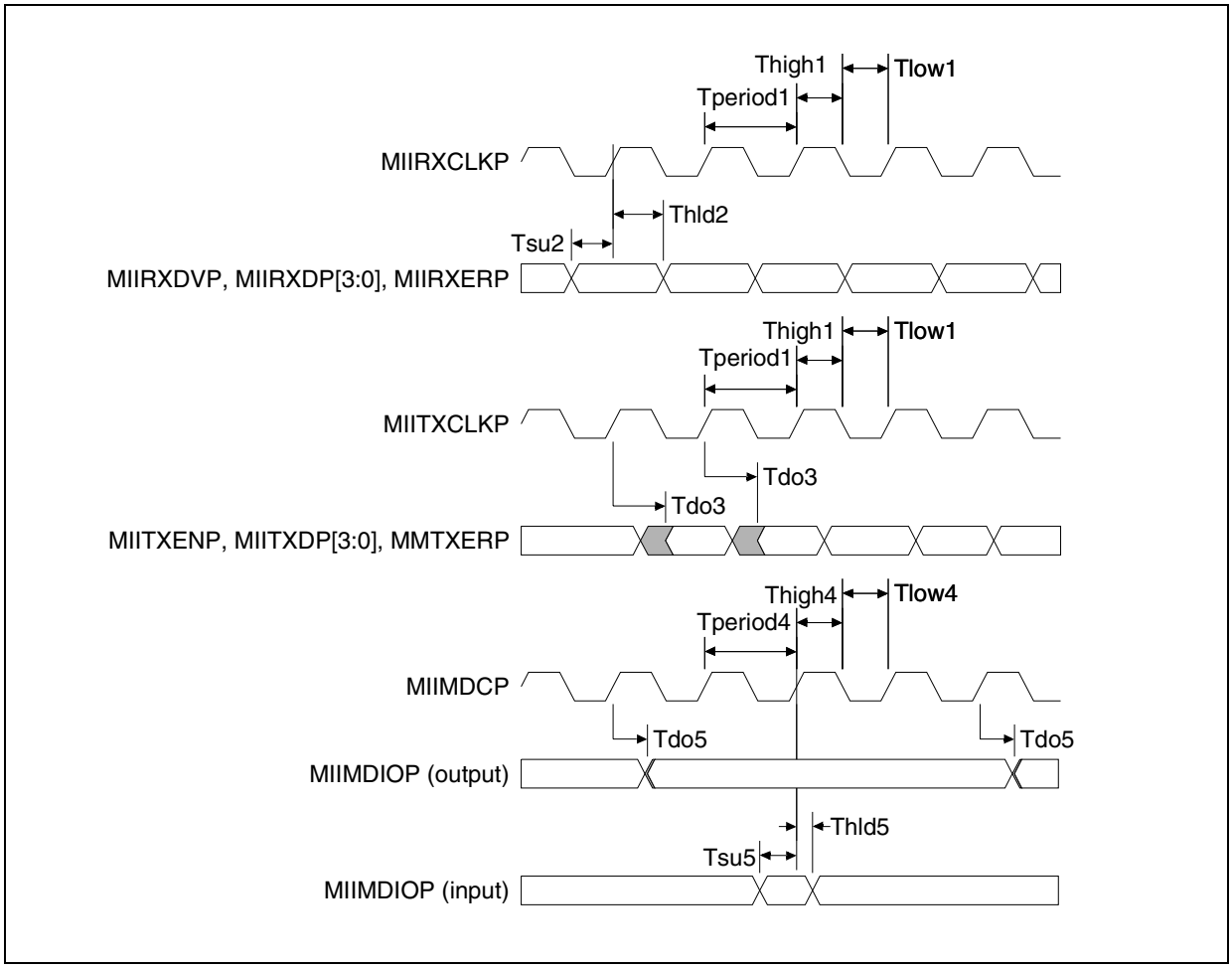


Figure 13 Ethernet AC Timing Waveform

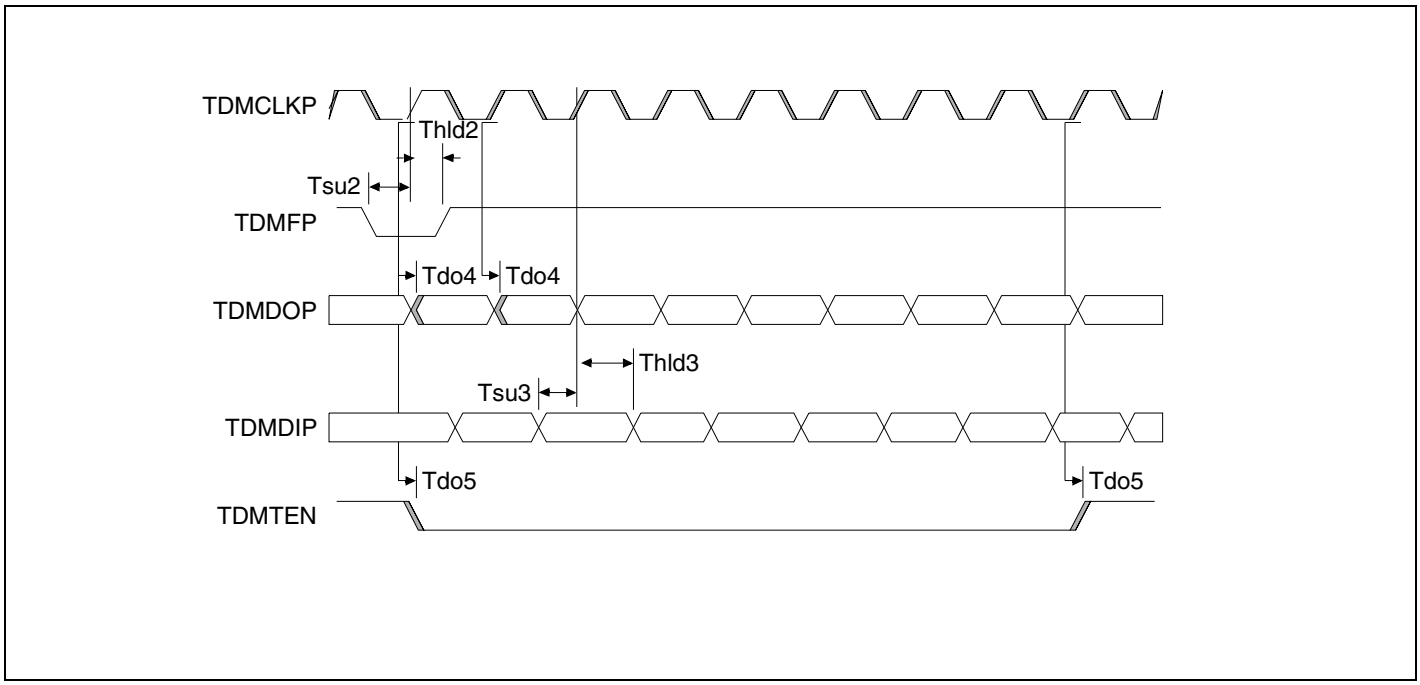


Figure 16 TDM AC Timing Waveform, Slave Mode

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
EJTAG and JTAG											
JTAG_TCK	Tperiod1	none	100	—	100	—	100	—	ns		Figure 20
	Thigh1, Tlow1		40	—	40	—	40	—	ns		
	Trise1, Tfall1		—	5	—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	7.5	10.0	6.7	10.0	5.6	10.0	ns		
	Thigh2, Tlow2		2.5	—	2.5	—	2.5	—	ns		
	Trise2, Tfall2		—	3.5	—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2	12.0	2	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 15 JTAG AC Timing Characteristics

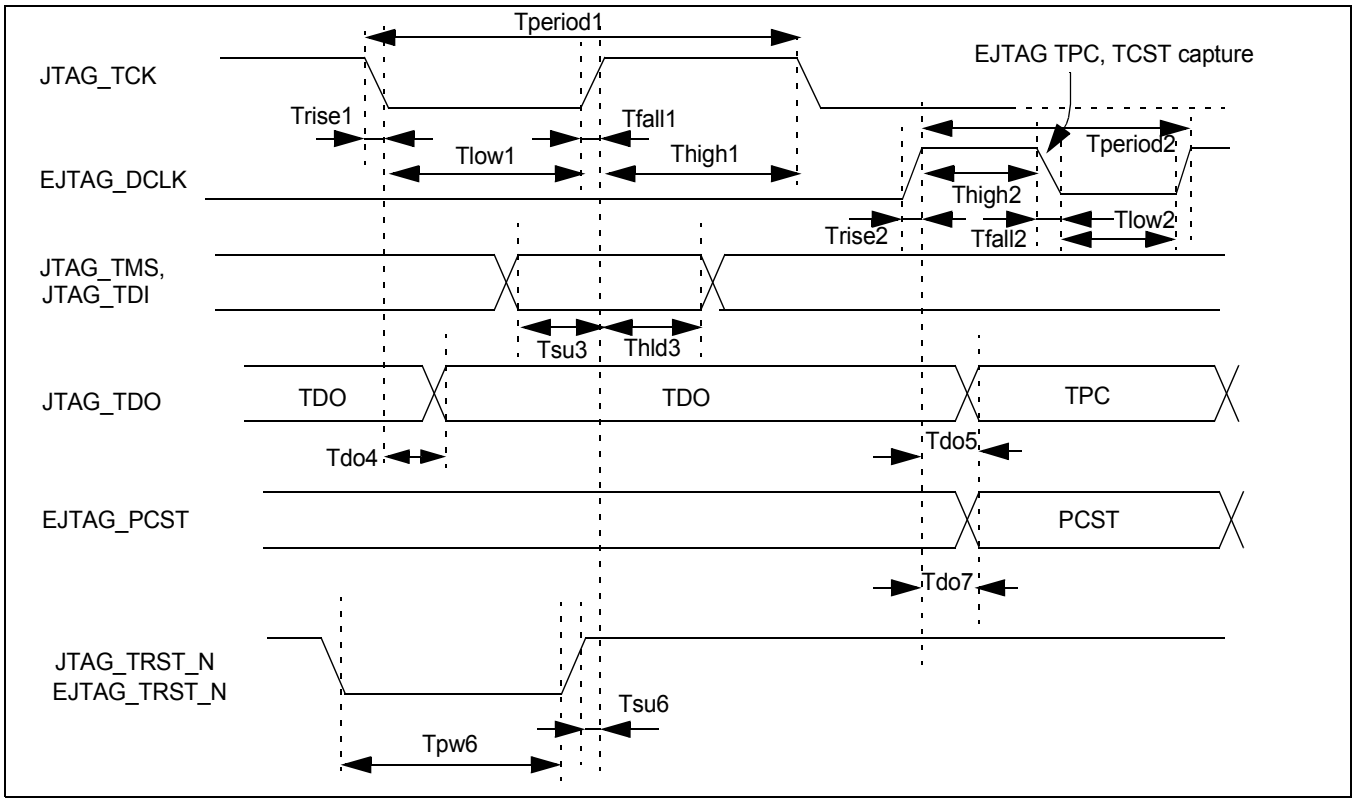


Figure 20 JTAG AC Timing Waveform

Table 16 shows the pin numbering for the Standard EJTAG connector. All the even numbered pins are connected to ground. Multiplexing of pin functions should be considered when connecting EJTAG_TRST_N and EJTAG_PCST.

For details on using the JTAG connector, see the JTAG chapters in the RC32355 user reference manual.

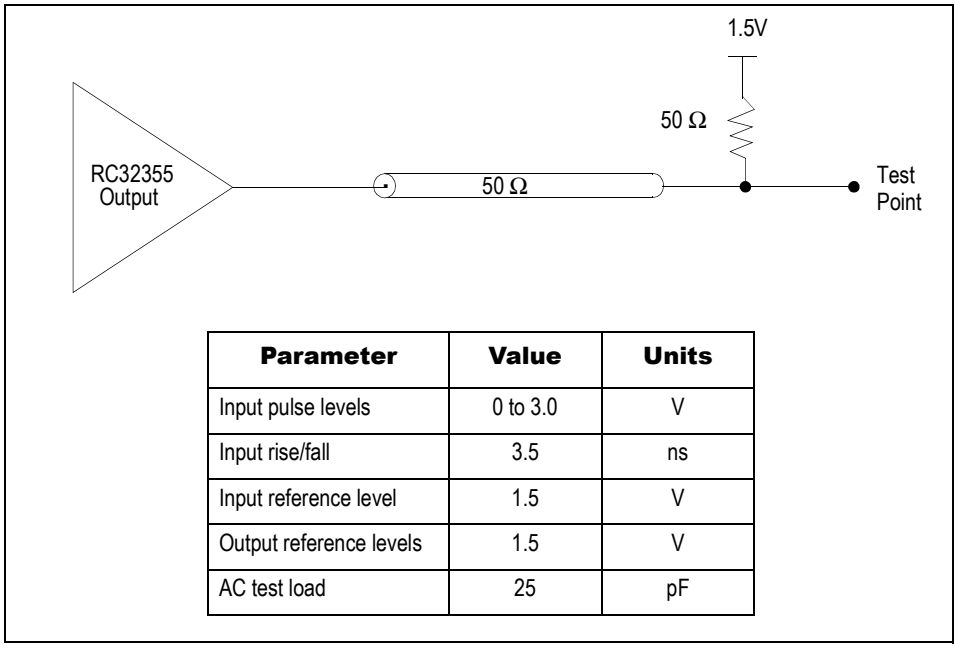
PIN	SIGNAL	RC32355 I/O	TERMINATION[1]
1	EJTAG_TRST_N	Input	10 kΩ pull-down resistor. A pull-down resistor will hold the EJTAG controller in reset when not in use if the EJTAG_TRST_N function is selected with the boot configuration vector. Refer to the User Manual.
3	JTAG_TDI	Input	10 kΩ pull-up resistor
5	JTAG_TDO	Output	33 Ω series resistor
7	JTAG_TMS	Input	10 kΩ pull-up resistor
9	JTAG_TCK	Input	10 kΩ pull-up resistor[2]
11	System Reset	Input	10 kΩ pull-up resistor is used if it is combined with the system cold reset control, COLDRSTN.
13	EJTAG_PCST[0]	Output	33 Ω series resistor
15	EJTAG_PCST[1]	Output	33 Ω series resistor
17	EJTAG_PCST[2]	Output	33 Ω series resistor
19	EJTAG_DCLK	Output	33 Ω series resistor
21	Debug Boot	Input	This can be connected to the boot configuration vector to control debug boot mode if desired. Refer to Table 2 on page 12 and the RC32355 user reference manual.
23	VccI/O	Output	Used to sense the circuit board power. Must be connected to the VCC I/O supply of the circuit board.

Table 16 Pin Numbering of the JTAG and EJTAG Target Connector

1. The value of the series resistor may depend on the actual printed circuit board layout situation.

2. JTAG_TCK pull-up resistor is not required according to the JTAG (IEEE1149) standard. It is indicated here to prevent a floating CMOS input when the EJTAG connector is unconnected.

AC Test Conditions



Parameter	Value	Units
Input pulse levels	0 to 3.0	V
Input rise/fall	3.5	ns
Input reference level	1.5	V
Output reference levels	1.5	V
AC test load	25	pF

Figure 21 Output Loading for AC Timing

Phase-Locked Loop (PLL)

The processor aligns the pipeline clock, PClock, to the master input clock (CLKP) by using an internal phase-locked loop (PLL) circuit that generates aligned clocks. Inherently, PLL circuits are only capable of generating aligned clocks for master input clock (CLKP) frequencies within a limited range.

PLL Analog Filter

The storage capacitor required for the Phase-Locked Loop circuit is contained in the RC32355. However, it is recommended that the system designer provide a filter network of passive components for the PLL power supply.

VccP (PLL circuit power) and VssP (PLL circuit ground) should be isolated from Vcc Core (core power) and Vss (common ground) with a filter circuit such as the one shown in Figure 22.

Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

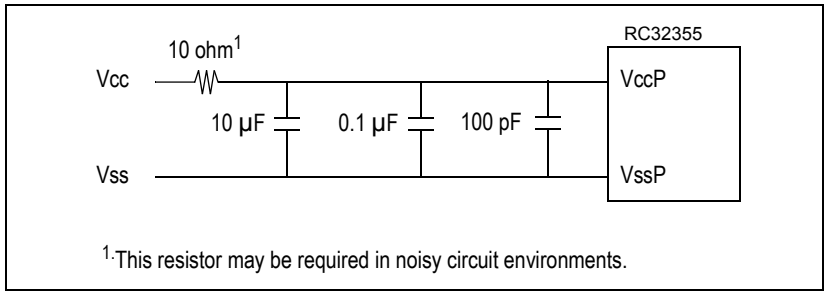


Figure 22 PLL Filter Circuit for Noisy Environments

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V_{ss}[1] V_{ssP}[5]	$V_{cc}I/O$[2]	$V_{cc}Core$[3] $V_{cc}P$[4]
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%
Industrial	-40°C+ 85°C Ambient	0V	3.3V±5%	2.5V±5%

[1] Vss supplies a common ground.
[2] VccI/O is the I/O power.
[3] VccCore is the internal logic power.
[4] VccP is the phase lock loop power.
[5] VssP is the phase lock loop ground.

Table 17 Temperature and Voltage

Capacitive Load Deration

Refer to the RC32355 IBIS Model which can be found at the IDT web site (www.idt.com).

USB Electrical Characteristics

	Parameter	Min	Max	Unit	Conditions
USB Interface					
V_{di}	Differential Input Sensitivity	-0.2		V	I(D+)-(D-)I
V_{cm}	Differential Input Common Mode Range	0.8	2.5	V	
V_{se}	Single ended Receiver Threshold	0.8	2.0	V	
C_{in}	Transceiver Capacitance		20	pF	
I_{li}	Hi-Z State Data Line Leakage	-10	10	µA	$0V < V_{in} < 3.3V$
USB Upstream/Downstream Port					
V_{oh}	Static Output High	2.8	3.6	V	15km ± 5% to Gnd
V_{ol}	Static Output Low		0.3	V	
Z_o	USB Driver Output Impedance	28	44	Ω	Including $R_{ext} = 20\ \Omega$

Table 19 USB Interface Characteristics

Power Consumption

Note: This table is based on a 2:1 CPU pipeline to system (PClock to CLKP) clock ratio.

Parameter		133MHz		150MHz		180MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC} I/O		80	130	100	150	120	170	mA	
$I_{CC\ core}$	Normal mode	400	450	450	500	500	550	mA	C_L = 25pF (affects I/O) $T_a = 25^oC$ VccP = 2.625V (for max. values) V_{cc} core = 2.625V (for max. values) V_{cc} I/O = 3.46V (for max. values) VccP = 2.5V (for typical values) V_{cc} core = 2.5V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	320	370	360	410	400	450	mA	
Power Dissipation	Normal mode	1.26	1.63	1.46	1.86	1.73	2.03	W	
	Standby mode[1]	1.06	1.42	1.22	1.59	1.47	1.77	W	

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions; however, other logic continues to function. Standby mode reduces power consumption by 0.6 mA per MHz of the CPU pipeline clock, PClock.

Table 20 RC32355 Power Consumption

Package Pin-out — 208-Pin PQFP

The following table lists the pin numbers and signal names for the RC32355.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	ATMOUTP[0]		53	JTAG_TDO		105	BGN		157	MDATA[28]	
2	ATMOUTP[1]		54	GPIOP[16]	1	106	CSN[0]		158	MDATA[13]	
3	ATMINP[02]		55	GPIOP[17]	1	107	CSN[1]		159	MDATA[29]	
4	ATMOUTP[2]		56	GPIOP[18]	1	108	CSN[2]		160	Vcc I/O	
5	Vss		57	Vss		109	Vcc I/O		161	MDATA[14]	
6	ATMOUTP[3]		58	JTAG_TCK		110	CSN[3]		162	Vss	
7	ATMINP[03]		59	GPIOP[19]	1	111	Vss		163	MDATA[30]	
8	ATMOUTP[4]		60	GPIOP[20]	1	112	OEN		164	MDATA[15]	
9	Vcc I/O		61	Vcc I/O		113	RWN		165	MDATA[31]	
10	ATMOUTP[5]		62	GPIOP[21]	1	114	BDIRN		166	CLKP	
11	ATMINP[04]		63	JTAG_TDI		115	BOEN[0]		167	WAITACKN	
12	ATMOUTP[6]		64	GPIOP[22]	1	116	BOEN[1]		168	MADDR[00]	
13	ATMOUTP[7]		65	GPIOP[23]	2	117	BWEN[0]		169	MADDR[11]	
14	ATMINP[05]		66	GPIOP[24]	1	118	Vcc I/O		170	MADDR[01]	
15	ATMOUTP[8]		67	JTAG_TMS		119	BWEN[1]		171	Vcc I/O	
16	ATMOUTP[9]		68	GPIOP[25]	2	120	Vss		172	MADDR[12]	
17	Vss		69	GPIOP[26]	1	121	BWEN[2]		173	Vss	
18	ATMINP[06]		70	Vss		122	Vcc Core		174	MADDR[02]	
19	Vcc Core		71	GPIOP[27]	1	123	BWEN[3]		175	MADDR[13]	
20	GPIOP[00]	1	72	COLDRSTN		124	MDATA[00]		176	MADDR[03]	
21	GPIOP[01]	1	73	GPIOP[28]	1	125	MDATA[16]		177	MADDR[14]	
22	ATMINP[07]		74	GPIOP[29]	1	126	MDATA[01]		178	MADDR[04]	
23	GPIOP[02]	2	75	GPIOP[30]	1	127	MDATA[17]		179	MADDR[15]	
24	GPIOP[03]	1	76	GPIOP[31]	2	128	MDATA[02]		180	Vcc I/O	
25	ATMINP[08]		77	USBCLKP		129	Vcc I/O		181	MADDR[05]	
26	Vcc I/O		78	Vcc I/O		130	MDATA[18]		182	Vcc Core	
27	GPIOP[04]	2	79	USBDN		131	Vss		183	SYSCLKP	
28	GPIOP[05]	1	80	USBDP		132	MDATA[03]		184	Vss	
29	ATMINP[09]		81	Vss		133	MDATA[19]		185	MADDR[16]	
30	VccP[1]		82	MIICRSP		134	MDATA[04]		186	MADDR[06]	
31	VssP[1]		83	MIICOLP		135	MDATA[20]		187	MADDR[17]	
32	ATMINP[10]		84	MIITXDP[0]		136	MDATA[05]		188	MADDR[07]	
33	GPIOP[06]	1	85	MIITXDP[1]		137	MDATA[21]		189	MADDR[18]	
34	Vss		86	Vcc Core		138	Vcc Core		190	MADDR[08]	

Table 22: 208-pin QFP Package Pin-Out (Part 1 of 2)

Alternate Pin Functions

Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		51	GPIOP[32]	TDMDOP	
21	GPIOP[01]	U0SINP		54	GPIOP[16]	CSN[4]	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	55	GPIOP[17]	CSN[5]	
24	GPIOP[03]	U0DCRN		56	GPIOP[18]	DMAREQN	
27	GPIOP[04]	U0DTRN	CPUP	59	GPIOP[19]	DMADONEN	
28	GPIOP[05]	U0DSRN		60	GPIOP[20]	USBSOF	
33	GPIOP[06]	U0RTSN		62	GPIOP[21]	CKENP	
35	GPIOP[07]	U0CTSN		64	GPIOP[22]	TXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	65	GPIOP[23]	TXADDR[1]	DMAP[0]
39	GPIOP[09]	U1SINP	DMAP[2]	66	GPIOP[24]	RXADDR[0]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	69	GPIOP[26]	TDMTEN	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	71	GPIOP[27]	MADDR[22]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	73	GPIOP[28]	MADDR[23]	
46	GPIOP[14]	SDAP		74	GPIOP[29]	MADDR[24]	
47	GPIOP[15]	SCLP		75	GPIOP[30]	MADDR[25]	
48	GPIOP[35]	TDMCLKP		76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
49	GPIOP[34]	TDMFP					
50	GPIOP[33]	TDMDIP					

Table 23 Alternate Pin Functions

Package Drawing - 208-pin QFP