Renesas Electronics America Inc - IDT79RC32T355-133DHI Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t355-133dhi

- **USB**
  - *Revision 1.1 compliant*
  - *USB slave device controller*
  - *Supports a 6th USB endpoint*
  - *Full speed operation at 12 Mb/s*
  - *Supports control, interrupt, bulk and isochronous endpoints*
  - *Supports USB remote wakeup*
  - *Integrated USB transceiver*
- **TDM**
  - *Serial Time Division Multiplexed (TDM) voice and data interface*
  - *Provides interface to telephone CODECs and DSPs*
  - *Interface to high quality audio A/Ds and D/As with external glue logic*
  - *Support 1 to 128 8-bit time slots*
  - *Compatible with Lucent CHI, GCI, Mitel ST-bus, K2 and SLD busses*
  - *Supports data rates of up to 8.192 Mb/s*
  - *Supports internal or external frame generation*
  - *Supports multiple non-contiguous active input and output time slots*
- **EJTAG**
  - *Run-time Mode provides a standard JTAG interface*
  - *Real-Time Mode provides additional pins for real-time trace information*
- **Ethernet**
  - *Full duplex support for 10 and 100 Mb/s Ethernet*
  - *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
  - *IEEE 802.3u auto-negotiation for automatic speed selection*
  - *Flexible address filtering modes*
  - *64-entry hash table based multicast address filtering*
- **ATM SAR**
  - *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
  - *Supports 25Mb/s and faster ATM*
  - *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
  - *Supports standard 53-byte ATM cells*
  - *Performs HEC generation and checking*
  - *Cell processing discards short cells and clips long cells*
  - *16 cells worth of buffering*
  - *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
  - *Hardware support for CRC-32 generation and checking for AAL5*
  - *Hardware support for CRC-10 generation and checking*
  - *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
  - *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*
- **System Features**
  - *JTAG Interface (IEEE Std. 1149.1 compatible)*
  - *208 pin PQFP package*
  - *2.5V core supply and 3.3V I/O supply*
  - *Up to 180 MHz pipeline frequency and up to 75 MHz bus frequency*

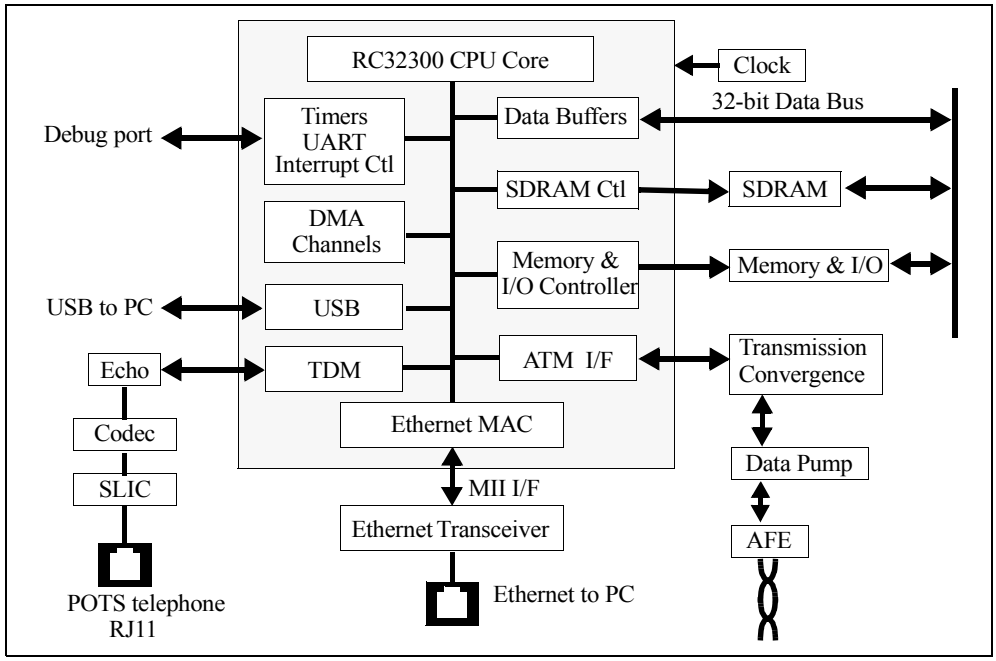


Figure 2 Example of xDSL Residential Gateway Using RC32355

Name	Type	I/O Type	Description
RWN	O	High Drive	**Read or Write.** This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device, a low level indicates a write to an external device.
OEN	O	High Drive	**Output Enable.** This signal is asserted low when data should be driven by an external device during device read transactions on the memory and peripheral bus.
BWEN[3:0]	O	High Drive	**SDRAM Byte Enable Mask or Memory and I/O Byte Write Enables.** These signals are used as data input/output masks during SDRAM transactions and as byte write enable signals during device controller transactions on the memory and peripheral bus. They are active low. BWEN[0] corresponds to byte lane MDATA[7:0]. BWEN[1] corresponds to byte lane MDATA[15:8]. BWEN[2] corresponds to byte lane MDATA[23:16]. BWEN[3] corresponds to byte lane MDATA[31:24].
SDCSN[1:0]	O	High Drive	**SDRAM Chip Select.** These signals are used to select the SDRAM device on the memory and peripheral bus. Each bit is asserted low during an access to the selected SDRAM.
RASN	O	High Drive	**SDRAM Row Address Strobe**. The row address strobe asserted low during memory and peripheral bus SDRAM transactions.
CASN	O	High Drive	**SDRAM Column Address Strobe.** The column address strobe asserted low during memory and peripheral bus SDRAM transactions.
SDWEN	O	High Drive	**SDRAM Write Enable.** Asserted low during memory and peripheral bus SDRAM write transactions.
CKENP	O	Low Drive	**SDRAM Clock Enable.** Asserted high during active SDRAM clock cycles. Primary function: General Purpose I/O, GPIOP[21].
SDCLKINP	I	STI	**SDRAM Clock Input.** This clock input is a delayed version of SYSCLKP. SDRAM read data is sampled into the RC32355 on the rising edge of this clock.
ATM Interface			
ATMINP[11:0]	I	STI	**ATM PHY Inputs.** These pins are the inputs for the ATM interface.
ATMIOP[1:0]	I/O	Low Drive with STI	**ATM PHY Bidirectional Signals.** These pins are the bidirectional pins for the ATM interface.
ATMOUTP[9:0]	O	Low Drive	**ATM PHY Outputs.** These pins are the outputs for the ATM interface.
TXADDR[1:0]	O	Low Drive	**ATM Transmit Address [1:0]**. 2-bit address bus used for transmission in Utopia-2 mode. TXADDR[0] Primary function: General purpose I/O, GPIOP[22]. TXADDR[1] Primary function: General purpose I/O, GPIOP[23].
RXADDR[1:0]	O	Low Drive	**ATM Receive Address [1:0]**. 2-bit address bus for receiving in Utopia-2 mode. RXADDR[0] Primary function: General purpose I/O, GPIOP[24]. RXADDR[1] Primary function: General purpose I/O, GPIOP[25].
TDM Bus			
TDMDOP	O	High Drive	**TDM Serial Data Output.** Serial data is driven by the RC32355 on this signal during an active output time slot. During inactive time slots this signal is tri-stated. Primary function: General purpose I/O, GPIOP[32].
TDMDIP	I	STI	**TDM Serial Data Input.** Serial data is received by the RC32355 on this signal during active input time slots. Primary function: General purpose I/O, GPIOP[33].
TDMFP	I/O	High Drive	**TDM Frame Signal.** A transition on this signal, the active polarity of which is programmable, delineates the start of a new TDM bus frame. TDMFP is driven if the RC32355 is a master, and is received if it is a slave. Primary function: General purpose I/O, GPIOP[34].
TDMCLKP	I	STI	**TDM Clock.** This input clock controls the rate at which data is sent and received on the TDM bus. Primary function: General purpose I/O, GPIOP[35].

Table 1 Pin Descriptions (Part 2 of 8)

Name	Type	I/O Type	Description
TDMTEN	O	Low Drive	**TDM External Buffer Enable.** This signal controls an external tri-state buffer output enable connected to the TDM output data, TDMDOP. It is asserted low when the RC32355 is driving data on TDMDOP. Primary function: General Purpose I/O, GPIOP[26]
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
GPIOP[5]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data set ready, U0DSRN.
GPIOP[6]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 request to send, U0RTSN.
GPIOP[7]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 clear to send, U0CTSN.
GPIOP[8]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial output, U1SOUTP. 2nd Alternate function: Active DMA channel code, DMAP[3].
GPIOP[9]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial input, U1SINP. 2nd Alternate function: Active DMA channel code, DMAP[2].
GPIOP[10]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[0].
GPIOP[11]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data set ready, U1DSRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[1].
GPIOP[12]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 request to send, U1RTSN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[2].
GPIOP[13]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 clear to send, U1CTSN. 2nd Alternate function: ICE PC trace clock, EJTAG_DCLK.
GPIOP[14]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface data, SDAP.
GPIOP[15]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface clock, SCLP.
GPIOP[16]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[4].

Table 1 Pin Descriptions (Part 3 of 8)

Name	Type	I/O Type	Description
GPIOP[17]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[5].
GPIOP[18]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: External DMA device request, DMAREQN.
GPIOP[19]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: External DMA device done, DMADONEN.
GPIOP[20]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: USB start of frame, USBSOF.
GPIOP[21]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: SDRAM clock enable CKENP.
GPIOP[22]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: ATM transmit PHY address, TXADDR[0].
GPIOP[23]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: ATM transmit PHY address, TXADDR[1]. 2nd Alternate function: Active DMA channel code, DMAP[0].
GPIOP[24]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: ATM receive PHY address, RXADDR[0].
GPIOP[25]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: ATM receive PHY address, RXADDR[1]. 2nd Alternate function: Active DMA channel code, DMAP[1].
GPIOP[26]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM external buffer enable, TDMTEN.
GPIOP[27]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[22].
GPIOP[28]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[23].
GPIOP[29]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[24].
GPIOP[30]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[25].
GPIOP[31]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1ST Alternate function: DMA finished, DMAFIN. 2nd Alternate function: EJTAG/ICE reset, EJTAG_TRST_N.
GPIOP[32]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface data output, TDMDOP. At reset, this pin defaults to the primary function, GPIOP[32].
GPIOP[33]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface data input, TDMDIP. At reset, this pin defaults to the primary function, GPIOP[33].
GPIOP[34]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface frame signal, TDMFP. At reset, this pin defaults to the primary function, GPIOP[34].
GPIOP[35]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface clock, TDMCLKP. At reset, this pin defaults to the primary function, GPIOP[35].
DMA			
DMAFIN	O	Low	**External DMA finished.** This signal is asserted low by the RC32355 when the number of bytes specified in the DMA descriptor have been transferred to or from an external device. Primary function: General Purpose I/O, GPIOP[31]. At reset, this pin defaults to primary function GPIOP[31]. 2nd Alternate function: EJTAG_TRST_N.

Table 1 Pin Descriptions (Part 4 of 8)

Name	Type	I/O Type	Description
U1CTSN	I	STI	**UART channel 1 clear to send.** Primary function: General Purpose I/O, GPIOP[13]. At reset, this pin defaults to primary function GPIOP[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 8 of 8)

1. Schmitt Trigger Input.
2. 2I^2C - Bus Specification by Philips Semiconductors.

Boot Configuration Vector

The boot configuration vector is read into the RC32355 during cold reset. The vector defines parameters in the RC32355 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Signal	Name/Description
MDATA[2:0]	**Clock Multiplier**. This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	**Endian.** This bit specifies the endianness of RC32355. 0x0 - little endian 0x1 - big endian
MDATA[4]	**Reserved.** Must be set to 0.
MDATA[5]	**Debug Boot Mode**. When this bit is set, the RC32355 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	**Boot Device Width**. This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	**EJTAG/ICE Interface Enable**. When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIOP[31, 13:10] pins behaves as GPIOP 0x1 - GPIOP[31] pin behaves as EJTAG_TRST_N, GPIOP[12:10] pins behave as EJTAG_PCST[2:0], and GPIOP[13] pin behaves as EJTAG_DCLK
MDATA[9]	**Fast Reset**. When this bit is set, RC32355 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32355 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32355 drives RSTN for 64 clock cycles (test only)
MDATA[10]	**DMA Debug Enable**. When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIOP[8, 9, 25, 23] pins behave as GPIOP 0x1 - GPIOP[8, 9, 25, 23] pins behave as DMAP[3:0]

Table 2 Boot Configuration Vector Encoding (Part 1 of 2)

Logic Diagram

The following Logic Diagram shows the primary pin functions of the RC32355.

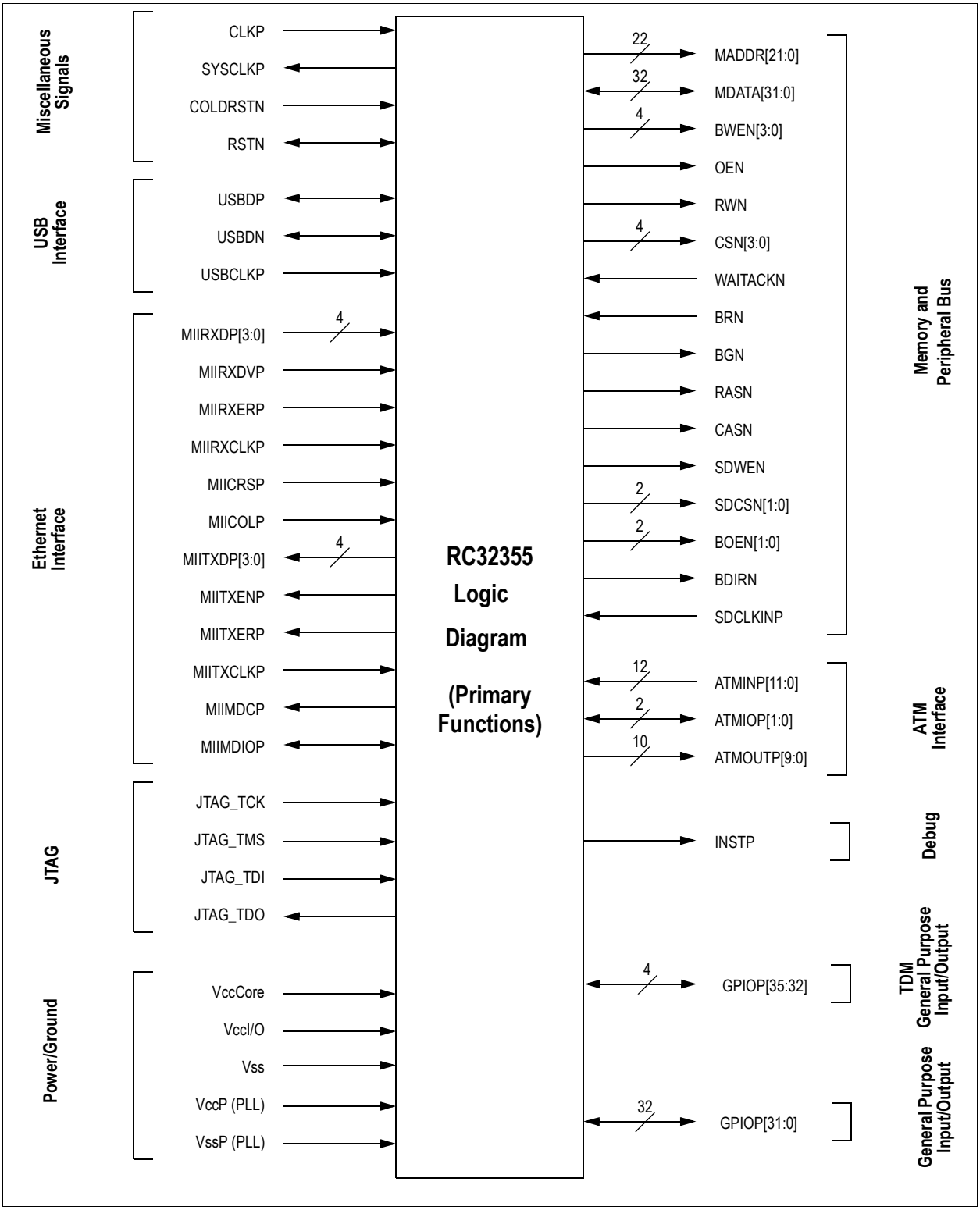


Figure 3 Logic Diagram

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

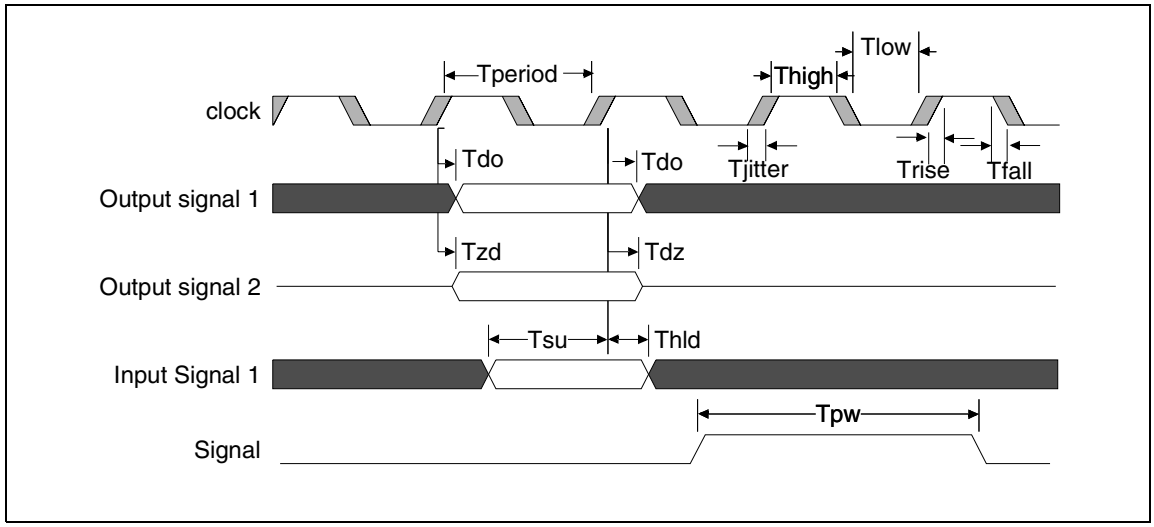
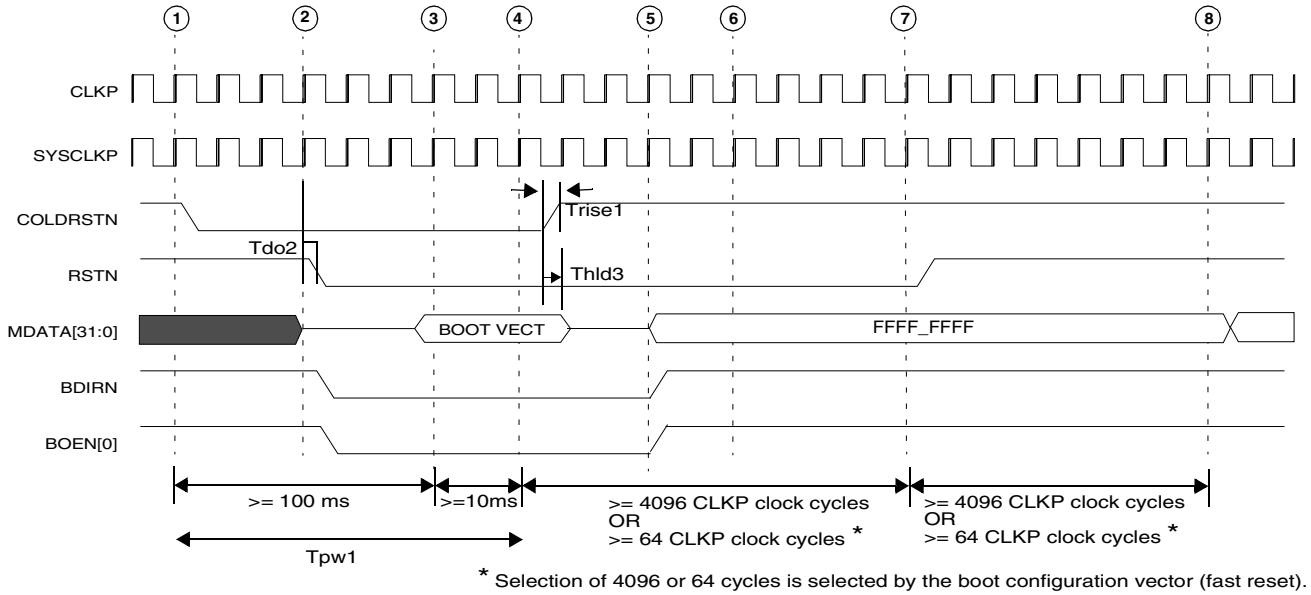


Figure 5 AC Timing Definitions Waveform

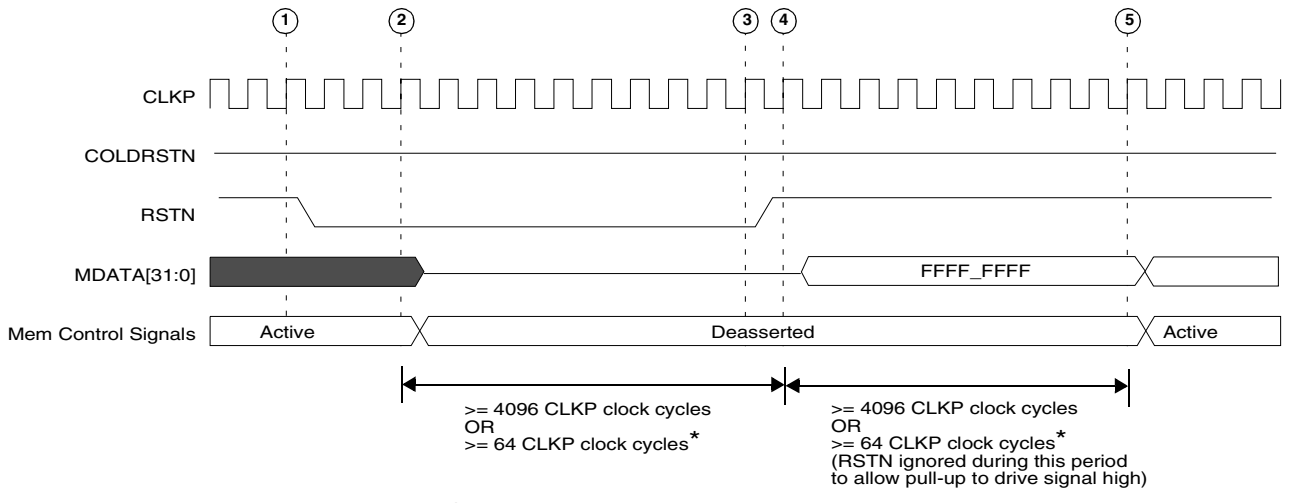
Symbol	Definition
Tperiod	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active.

Table 4 AC Timing Definitions



1. COLDRSTN asserted by external logic.
2. The RC32355 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32355 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32355 stops sampling the boot configuration vector.
5. The RC32355 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLKP may be held constant after this point if Hold SYSCLKP Constant is selected in the boot configuration vector.
7. RSTN negated by RC32355.
8. CPU begins executing by taking MIPS reset exception, and the RC32355 starts sampling RSTN as a warm reset input.

Figure 6 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32355 asserts RSTN output low in response.
2. The RC32355 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32355 deasserts RSTN.
4. The RC32355 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - SDRAM Access											
MDATA[31:0]	Tsu1	SDCLKINP rising	2.5	—	2.5	—	2.5	—	ns		Figure 8 Figure 9 Figure 10
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1	SYSCLKP rising	1.2	5.8	1.2	5.8	1.2	5.8	ns		
	Tdz1		—	5.0	—	5.0	—	5.0	ns		
	Tzd1		1.0	—	1.0	—	1.0	—	ns		
MADDR[20:2], BWEN[3:0]	Tdo2	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CASN, RASN, SDCSN[1:0], SDWEN	Tdo3	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CKENP	Tdo4	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BDIRN	Tdo5	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BOEN[1:0]	Tdo6	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
SYSCLKP rising	Tdo7	CLKP rising	0.5	5.0	0.5	5.0	0.5	5.0	ns		
SDCLKINP	Tperiod8	none	15	50	13.3	50	13.3	50	ns		
	Thigh8,Tlow8		6.0	—	5.4	—	5.4	—	ns		
	Trise8,Tfall8		—	3.0	—	2.5	—	2.5	ns		
	Tdelay8	SYSCLKP rising	0	4.8	0	4.8	0	4.8	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - Device Access											
MDATA[31:0]	Tsu1	CLKP rising	2.5	—	2.5	—	2.5	—	ns		Figure 11 Figure 12
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1		2.0	6.5	2.0	6.5	2.0	6.5	ns		
	Tdz1		—	9.0	—	9.0	—	9.0	ns		
	Tzd1		2.0	—	2.0	—	2.0	—	ns		
WAITACKN, BRN	Tsu	CLKP rising	2.5	—	2.5	—	2.5	—	ns		
	Thld		1.5	—	1.5	—	1.5	—	ns		
MADDR[21:0]	Tdo2	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz2		—	9.0	—	9.0	—	9.0	ns		
	Tzd2		2.0	—	2.0	—	2.0	—	ns		
MADDR[25:22]	Tdo3	CLKP rising	2.5	6.5	2.5	6.5	2.5	6.5	ns		
	Tdz3		—	9.0	—	9.0	—	9.0	ns		
	Tzd3		2.0	—	2.0	—	2.0	—	ns		
BDIRN, BOEN[0]	Tdo4	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz4		—	9.0	—	9.0	—	9.0	ns		
	Tzd4		2.0	—	2.0	—	2.0	—	ns		
BGN, BWEN[3:0], OEN, RWN	Tdo5	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz5		—	9.0	—	9.0	—	9.0	ns		
	Tzd5		2.0	—	2.0	—	2.0	—	ns		
CSN[3:0]	Tdo6	CLKP rising	1.7	5.0	1.7	5.0	1.7	5.0	ns		
	Tdz6		—	9.0	—	9.0	—	9.0	ns		
	Tzd6		2.0	—	2.0	—	2.0	—	ns		
CSN[5:4]	Tdo7	CLKP rising	2.5	6.0	2.5	6.0	2.5	6.0	ns		
	Tdz7		—	9.0	—	9.0	—	9.0	ns		
	Tzd7		2.0	—	2.0	—	2.0	—	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

Note: The RC32355 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32355 are both driving. See the chapters “Device Controller,” “Synchronous DRAM Controller,” and “Bus Arbitration” in the RC32355 User Reference Manual.

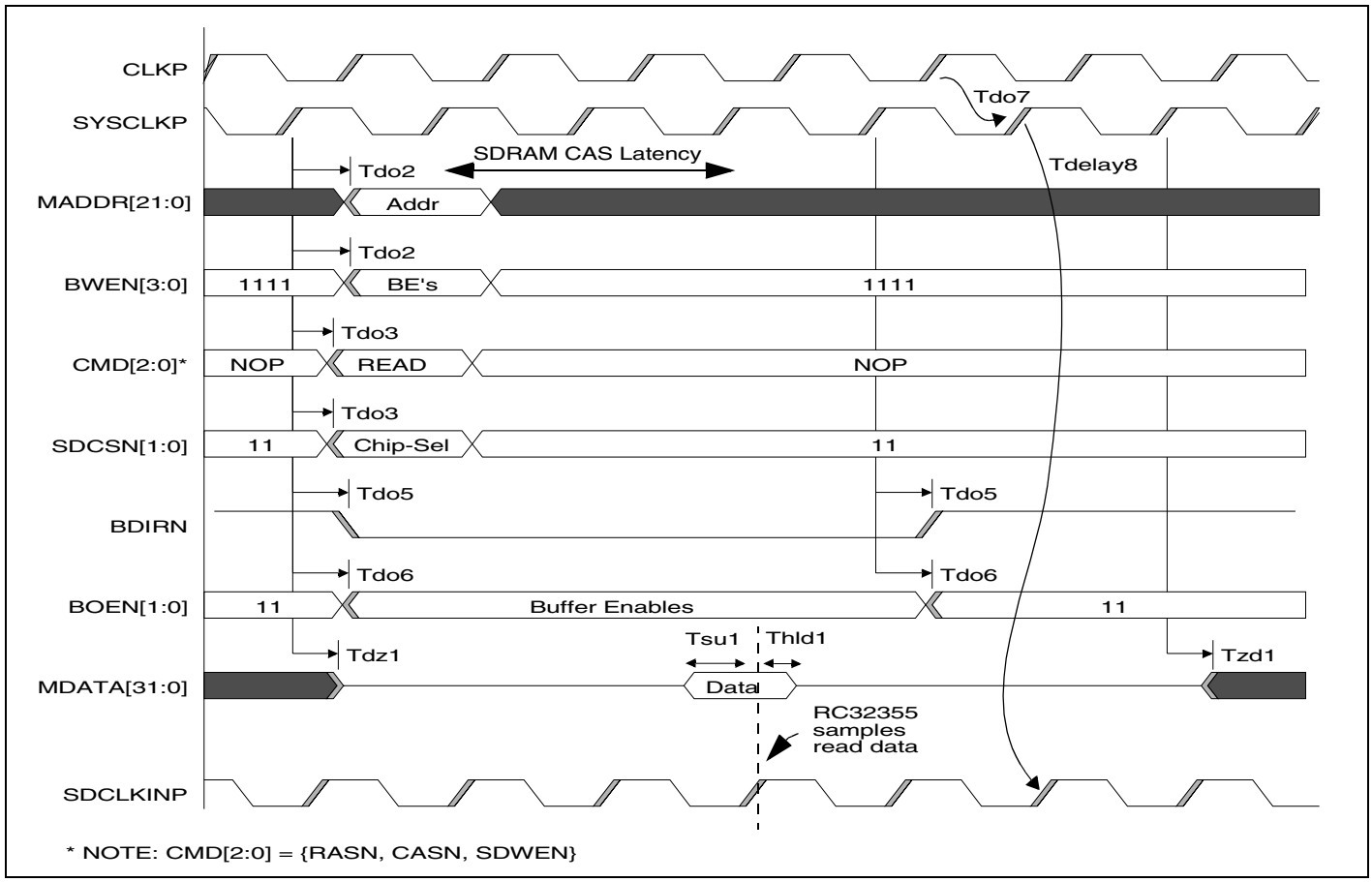


Figure 8 Memory and Peripheral Bus AC Timing Waveform - SDRAM Read Access

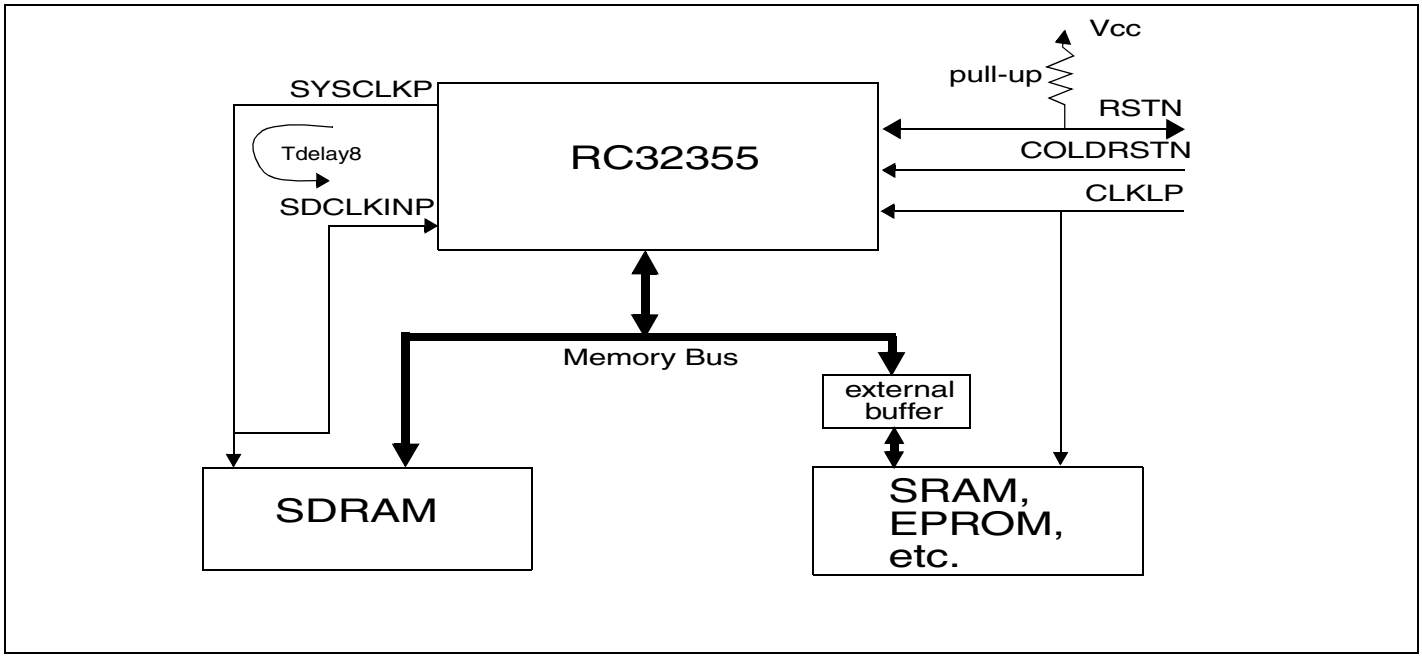


Figure 9 SYSCLKP - SDCLKINP Relationship

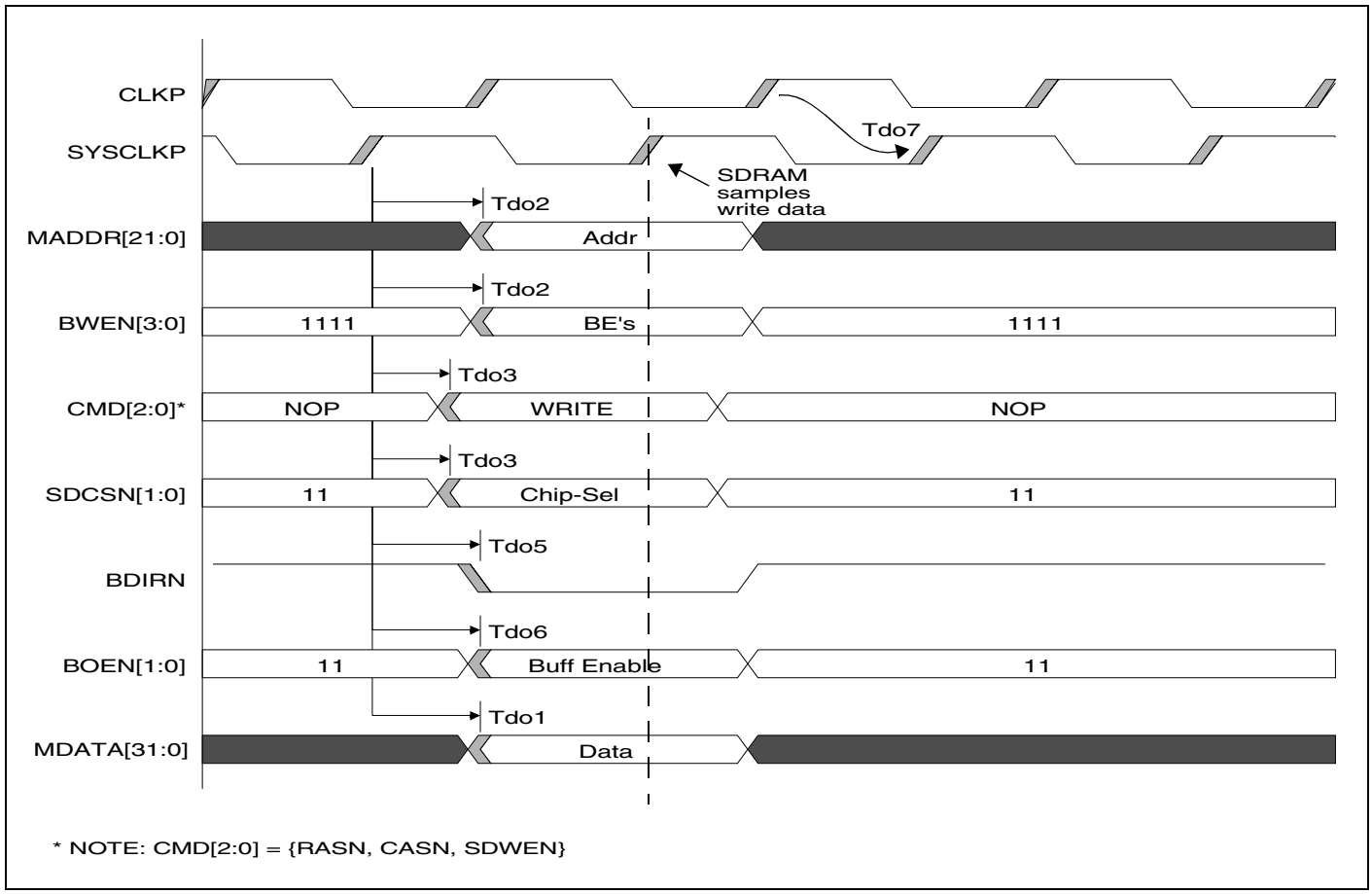


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

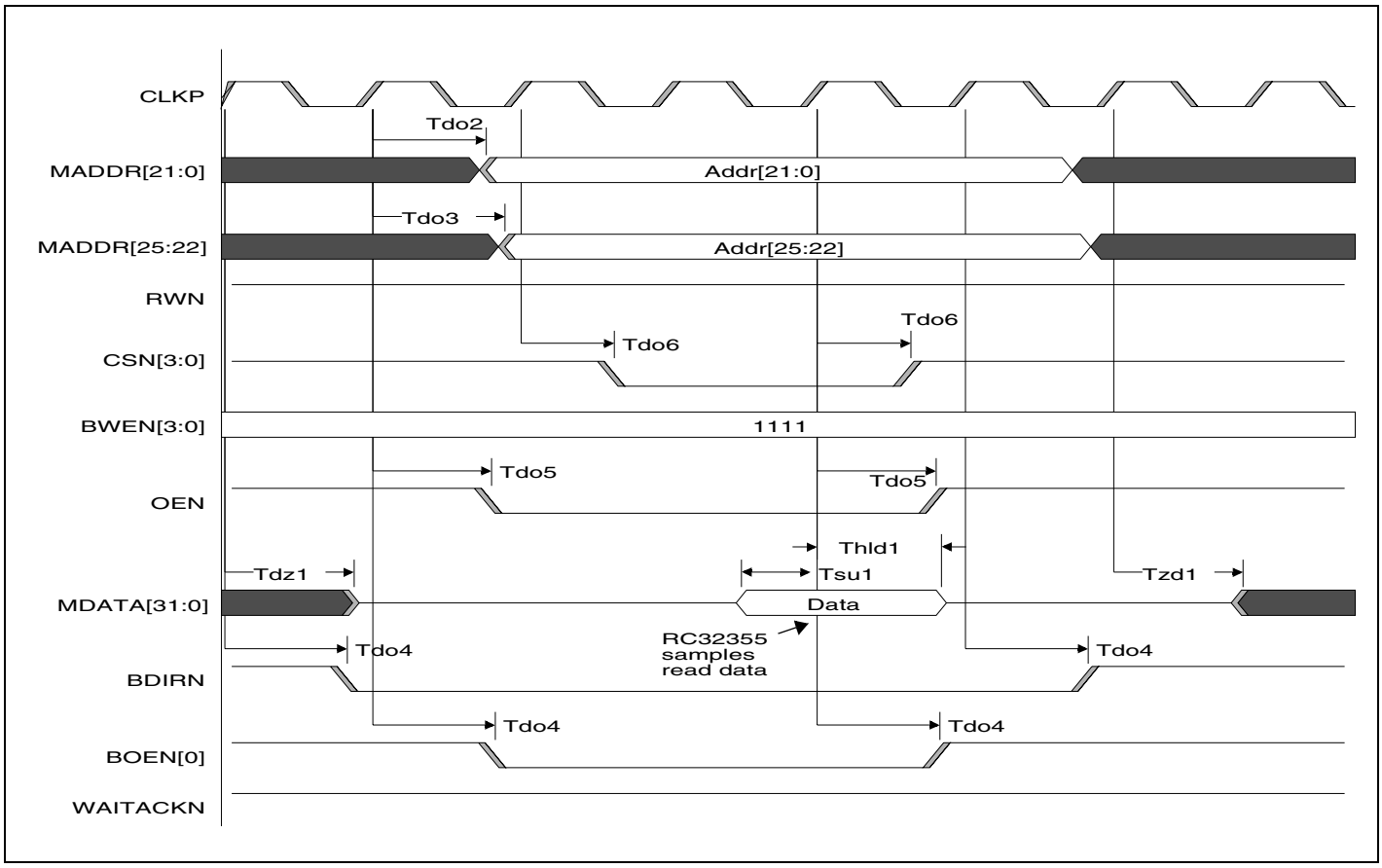


Figure 11 Memory and Peripheral Bus AC Timing Waveform - Device Read Access

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
ATM Interface, Utopia Mode[1, 2]											
RXCLKP, TXCLKP[1]	Tperiod1	none	—	40	—	40	—	40	ns	25 MHz Utopia	Figure 14
	Thigh1,Tlow1		16	—	16	—	16	—	ns		
	Trise1,Tfall1		—	4	—	4	—	4	ns		
RXCLKP, TXCLKP[1]	Tperiod1	none	—	30	—	30	—	30	ns	33 MHz Utopia	
	Thigh1,Tlow1		12	—	12	—	12	—	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
RXCLKP, TXCLKP	Tperiod1	none	—	20	—	20	—	20	ns	50 MHz Utopia	
	Thigh,Tlow1		8	—	8	—	8	—	ns		
	Trise1,Tfall1		—	2	—	2	—	2	ns		
TXFULLN	Tsu2	TXCLKP rising	2	—	2	—	2	—	ns		
	Thld2		2	—	2	—	2	—	ns		
TXDATA[7:0], TXSOC, TXENBN, TXADDR[1:0]	Tdo3	TXCLKP rising	4	8	4	8	4	8	ns		
RXDATA[7:0], RXEMP-TYN, RXSOC	Tsu4	RXCLKP rising	3	—	3	—	3	—	ns		
	Thld4		2	—	2	—	2	—	ns		
RXADDR[1:0], RXENBN	Tdo5	RXCLKP rising	3	8	3	8	3	8	ns		

Table 8 ATM AC Timing Characteristics

1. ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

2. All Utopia Mode pins are multiplexed on the ATM interface pins as described in Table 9.

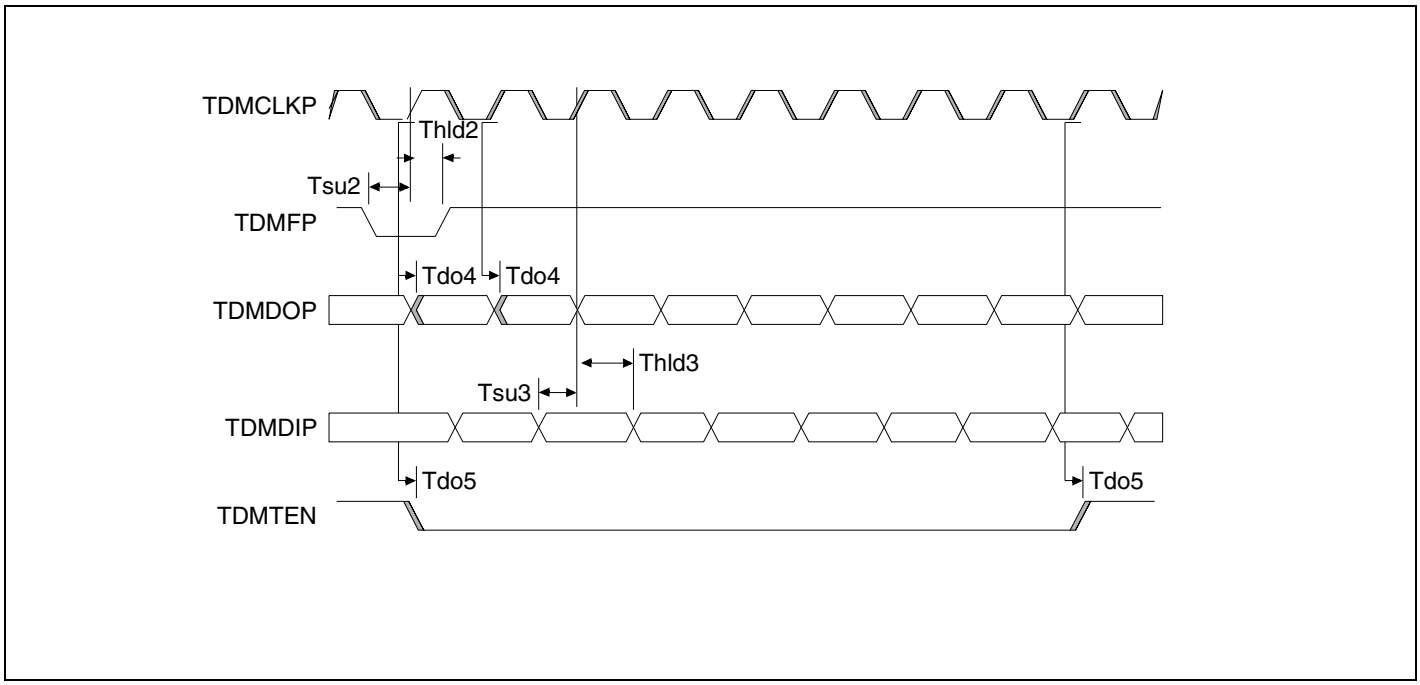


Figure 16 TDM AC Timing Waveform, Slave Mode

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
USB											
USBCLKP[1]	Tperiod1	none	19.79	21.87	19.79	21.87	19.79	21.87	ns		Figure 17
	Thigh1,Tlow1		8.3	—	8.3	—	8.3	—	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
	Tjitter1		—	0.8	—	0.8	—	0.8	ns	1/4th of the minimum Source data jitter	
USBDN, USBDP	Trise2		4	20	4	20	4	20	ns	Universal Serial Bus Specification (USBS) Revision 1.1: Figures 7.6 and 7.7.	
	Tfall2		4	20	4	20	4	20	ns	USBS Revision 1.1: Figures 7.6 and 7.7.	
USBDN and USBDP Rise and Fall Time Matching			90	111.11	90	111.11	90	111.11	%	USBS Revision 1.1: Note 10, Section 7.1.2.	
Data valid period	Tstate		60	—	60	—	60	—	ns		
Skew between USBDN and USBDP			—	0.4	—	0.4	—	0.4	ns	USBS Revision 1.1: Section 7.1.3	
Source data jitter			—	3.5	—	3.5	—	3.5	ns	USBS Revision 1.1: Table 7-6	
Receive data jitter			—	12	—	12	—	12	ns		
Source EOP length	Tseop		160	175	160	175	160	175	ns		
Receive EOP length	Treop		82	—	82	—	82	—	ns		
EOP jitter			-2	5	-2	5	-2	5	ns		
Full-speed Data Rate	Tfdrate		11.97	12.03	11.97	12.03	11.97	12.03	MHz	Average bit rate, USBS Section 7.1.11.	
Frame Interval			0.9995	1.0005	0.9995	1.0005	0.9995	1.0005	ms	USBS Section 7.1.12.	
Consecutive Frame Interval Jitter			—	42	—	42	—	42	ns	Without frame adjustment.	
			—	126	—	126	—	126	ns	With frame adjustment.	

[1] USB clock (USBCLKP) frequency must be less than CLKP frequency.

Table 11 USB AC Timing Characteristics

Table 16 shows the pin numbering for the Standard EJTAG connector. All the even numbered pins are connected to ground. Multiplexing of pin functions should be considered when connecting EJTAG_TRST_N and EJTAG_PCST.

For details on using the JTAG connector, see the JTAG chapters in the RC32355 user reference manual.

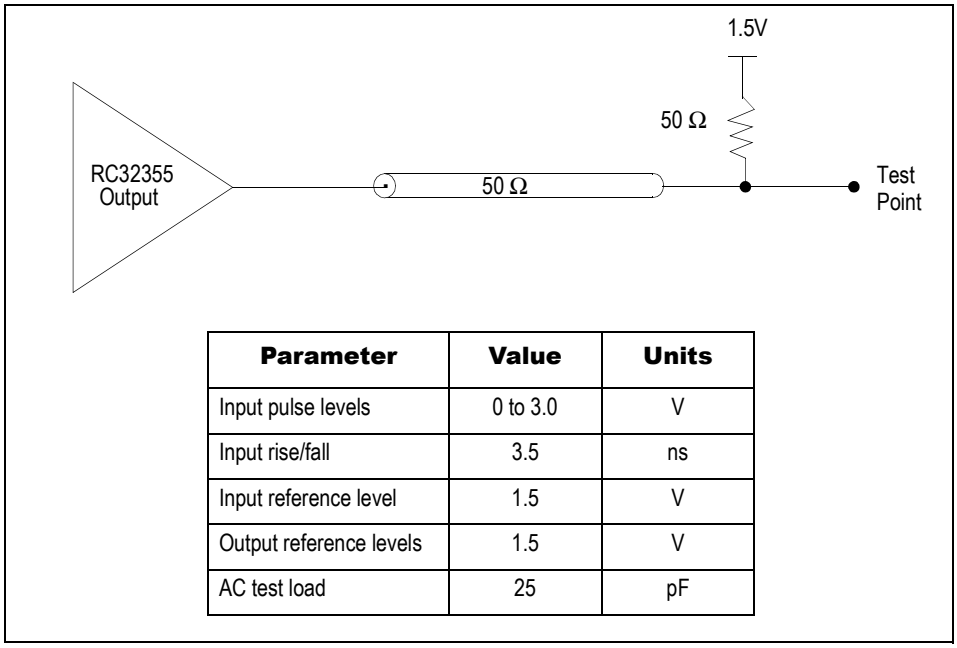
PIN	SIGNAL	RC32355 I/O	TERMINATION[1]
1	EJTAG_TRST_N	Input	10 kΩ pull-down resistor. A pull-down resistor will hold the EJTAG controller in reset when not in use if the EJTAG_TRST_N function is selected with the boot configuration vector. Refer to the User Manual.
3	JTAG_TDI	Input	10 kΩ pull-up resistor
5	JTAG_TDO	Output	33 Ω series resistor
7	JTAG_TMS	Input	10 kΩ pull-up resistor
9	JTAG_TCK	Input	10 kΩ pull-up resistor[2]
11	System Reset	Input	10 kΩ pull-up resistor is used if it is combined with the system cold reset control, COLDRSTN.
13	EJTAG_PCST[0]	Output	33 Ω series resistor
15	EJTAG_PCST[1]	Output	33 Ω series resistor
17	EJTAG_PCST[2]	Output	33 Ω series resistor
19	EJTAG_DCLK	Output	33 Ω series resistor
21	Debug Boot	Input	This can be connected to the boot configuration vector to control debug boot mode if desired. Refer to Table 2 on page 12 and the RC32355 user reference manual.
23	VccI/O	Output	Used to sense the circuit board power. Must be connected to the VCC I/O supply of the circuit board.

Table 16 Pin Numbering of the JTAG and EJTAG Target Connector

1. The value of the series resistor may depend on the actual printed circuit board layout situation.

2. JTAG_TCK pull-up resistor is not required according to the JTAG (IEEE1149) standard. It is indicated here to prevent a floating CMOS input when the EJTAG connector is unconnected.

AC Test Conditions



Parameter	Value	Units
Input pulse levels	0 to 3.0	V
Input rise/fall	3.5	ns
Input reference level	1.5	V
Output reference levels	1.5	V
AC test load	25	pF

Figure 21 Output Loading for AC Timing

Package Pin-out — 208-Pin PQFP

The following table lists the pin numbers and signal names for the RC32355.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	ATMOUTP[0]		53	JTAG_TDO		105	BGN		157	MDATA[28]	
2	ATMOUTP[1]		54	GPIOP[16]	1	106	CSN[0]		158	MDATA[13]	
3	ATMINP[02]		55	GPIOP[17]	1	107	CSN[1]		159	MDATA[29]	
4	ATMOUTP[2]		56	GPIOP[18]	1	108	CSN[2]		160	Vcc I/O	
5	Vss		57	Vss		109	Vcc I/O		161	MDATA[14]	
6	ATMOUTP[3]		58	JTAG_TCK		110	CSN[3]		162	Vss	
7	ATMINP[03]		59	GPIOP[19]	1	111	Vss		163	MDATA[30]	
8	ATMOUTP[4]		60	GPIOP[20]	1	112	OEN		164	MDATA[15]	
9	Vcc I/O		61	Vcc I/O		113	RWN		165	MDATA[31]	
10	ATMOUTP[5]		62	GPIOP[21]	1	114	BDIRN		166	CLKP	
11	ATMINP[04]		63	JTAG_TDI		115	BOEN[0]		167	WAITACKN	
12	ATMOUTP[6]		64	GPIOP[22]	1	116	BOEN[1]		168	MADDR[00]	
13	ATMOUTP[7]		65	GPIOP[23]	2	117	BWEN[0]		169	MADDR[11]	
14	ATMINP[05]		66	GPIOP[24]	1	118	Vcc I/O		170	MADDR[01]	
15	ATMOUTP[8]		67	JTAG_TMS		119	BWEN[1]		171	Vcc I/O	
16	ATMOUTP[9]		68	GPIOP[25]	2	120	Vss		172	MADDR[12]	
17	Vss		69	GPIOP[26]	1	121	BWEN[2]		173	Vss	
18	ATMINP[06]		70	Vss		122	Vcc Core		174	MADDR[02]	
19	Vcc Core		71	GPIOP[27]	1	123	BWEN[3]		175	MADDR[13]	
20	GPIOP[00]	1	72	COLDRSTN		124	MDATA[00]		176	MADDR[03]	
21	GPIOP[01]	1	73	GPIOP[28]	1	125	MDATA[16]		177	MADDR[14]	
22	ATMINP[07]		74	GPIOP[29]	1	126	MDATA[01]		178	MADDR[04]	
23	GPIOP[02]	2	75	GPIOP[30]	1	127	MDATA[17]		179	MADDR[15]	
24	GPIOP[03]	1	76	GPIOP[31]	2	128	MDATA[02]		180	Vcc I/O	
25	ATMINP[08]		77	USBCLKP		129	Vcc I/O		181	MADDR[05]	
26	Vcc I/O		78	Vcc I/O		130	MDATA[18]		182	Vcc Core	
27	GPIOP[04]	2	79	USBDN		131	Vss		183	SYSCLKP	
28	GPIOP[05]	1	80	USBDP		132	MDATA[03]		184	Vss	
29	ATMINP[09]		81	Vss		133	MDATA[19]		185	MADDR[16]	
30	VccP[1]		82	MIICRSP		134	MDATA[04]		186	MADDR[06]	
31	VssP[1]		83	MIICOLP		135	MDATA[20]		187	MADDR[17]	
32	ATMINP[10]		84	MIITXDP[0]		136	MDATA[05]		188	MADDR[07]	
33	GPIOP[06]	1	85	MIITXDP[1]		137	MDATA[21]		189	MADDR[18]	
34	Vss		86	Vcc Core		138	Vcc Core		190	MADDR[08]	

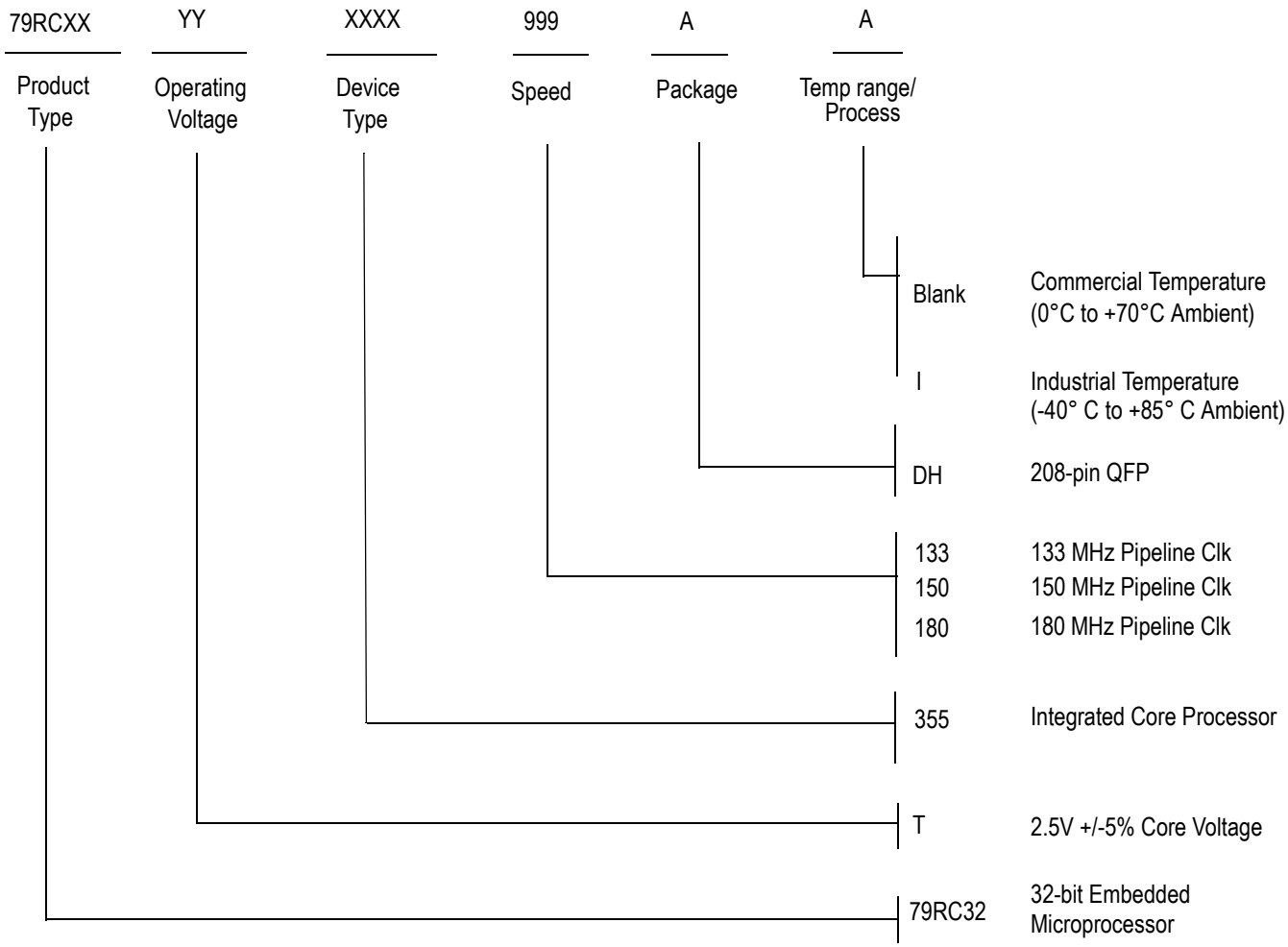
Table 22: 208-pin QFP Package Pin-Out (Part 1 of 2)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
35	GPIOP[07]	1	87	MIITXDP[2]		139	MDATA[06]		191	Vcc I/O	
36	ATMINP [11]		88	MIITXDP[3]		140	Vcc I/O		192	MADDR[19]	
37	GPIOP[08]	2	89	MIITXENP		141	MDATA[22]		193	Vss	
38	Vcc Core		90	MIITXCLKP		142	Vss		194	MADDR[09]	
39	GPIOP[09]	2	91	MIITXERP		143	MDATA[07]		195	MADDR[20]	
40	GPIOP[10]	2	92	MIIRXERP		144	MDATA[23]		196	MADDR[10]	
41	GPIOP[11]	2	93	MIIRXCLKP		145	SDCLKINP		197	MADDR[21]	
42	GPIOP[12]	2	94	MIIRXDVP		146	MDATA[08]		198	CASN	
43	Vcc I/O		95	Vcc I/O		147	MDATA[24]		199	RASN	
44	GPIOP[13]	2	96	MIIRXDP[0]		148	MDATA[09]		200	SDWEN	
45	Vss		97	MIIRXDP[1]		149	MDATA[25]		201	Vcc I/O	
46	GPIOP[14]	1	98	MIIRXDP[2]		150	MDATA[10]		202	SDCSN[0]	
47	GPIOP[15]	1	99	MIIRXDP[3]		151	Vcc I/O		203	Vss	
48	GPIOP[35]	1	100	Vss		152	MDATA[26]		204	SDCSN[1]	
49	GPIOP[34]	1	101	MIIDCP		153	Vss		205	ATMINP[00]	
50	GPIOP[33]	1	102	MIIDIOP		154	MDATA[11]		206	ATMIOP[0]	
51	GPIOP[32]	1	103	RSTN		155	MDATA[27]		207	ATMIOP[1]	
52	INSTP		104	BRN		156	MDATA[12]		208	ATMINP[01]	

[1] VccP and VssP are the Phase Lock Loop (PLL) power and ground. PLL power and ground should be supplied through a special filter circuit.

Table 22: 208-pin QFP Package Pin-Out (Part 2 of 2)

Ordering Information



Valid Combinations

79RC32T355 -133DH, 150DH, 180DH	208-pin QFP package, Commercial Temperature
79RC32T355 -133DHI, 150DHI	208-pin QFP package, Industrial Temperature

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