Renesas Electronics America Inc - IDT79RC32T355-150DH Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t355-150dh

- **USB**
  - *Revision 1.1 compliant*
  - *USB slave device controller*
  - *Supports a 6th USB endpoint*
  - *Full speed operation at 12 Mb/s*
  - *Supports control, interrupt, bulk and isochronous endpoints*
  - *Supports USB remote wakeup*
  - *Integrated USB transceiver*
- **TDM**
  - *Serial Time Division Multiplexed (TDM) voice and data interface*
  - *Provides interface to telephone CODECs and DSPs*
  - *Interface to high quality audio A/Ds and D/As with external glue logic*
  - *Support 1 to 128 8-bit time slots*
  - *Compatible with Lucent CHI, GCI, Mitel ST-bus, K2 and SLD busses*
  - *Supports data rates of up to 8.192 Mb/s*
  - *Supports internal or external frame generation*
  - *Supports multiple non-contiguous active input and output time slots*
- **EJTAG**
  - *Run-time Mode provides a standard JTAG interface*
  - *Real-Time Mode provides additional pins for real-time trace information*
- **Ethernet**
  - *Full duplex support for 10 and 100 Mb/s Ethernet*
  - *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
  - *IEEE 802.3u auto-negotiation for automatic speed selection*
  - *Flexible address filtering modes*
  - *64-entry hash table based multicast address filtering*
- **ATM SAR**
  - *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
  - *Supports 25Mb/s and faster ATM*
  - *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
  - *Supports standard 53-byte ATM cells*
  - *Performs HEC generation and checking*
  - *Cell processing discards short cells and clips long cells*
  - *16 cells worth of buffering*
  - *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
  - *Hardware support for CRC-32 generation and checking for AAL5*
  - *Hardware support for CRC-10 generation and checking*
  - *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
  - *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*
- **System Features**
  - *JTAG Interface (IEEE Std. 1149.1 compatible)*
  - *208 pin PQFP package*
  - *2.5V core supply and 3.3V I/O supply*
  - *Up to 180 MHz pipeline frequency and up to 75 MHz bus frequency*

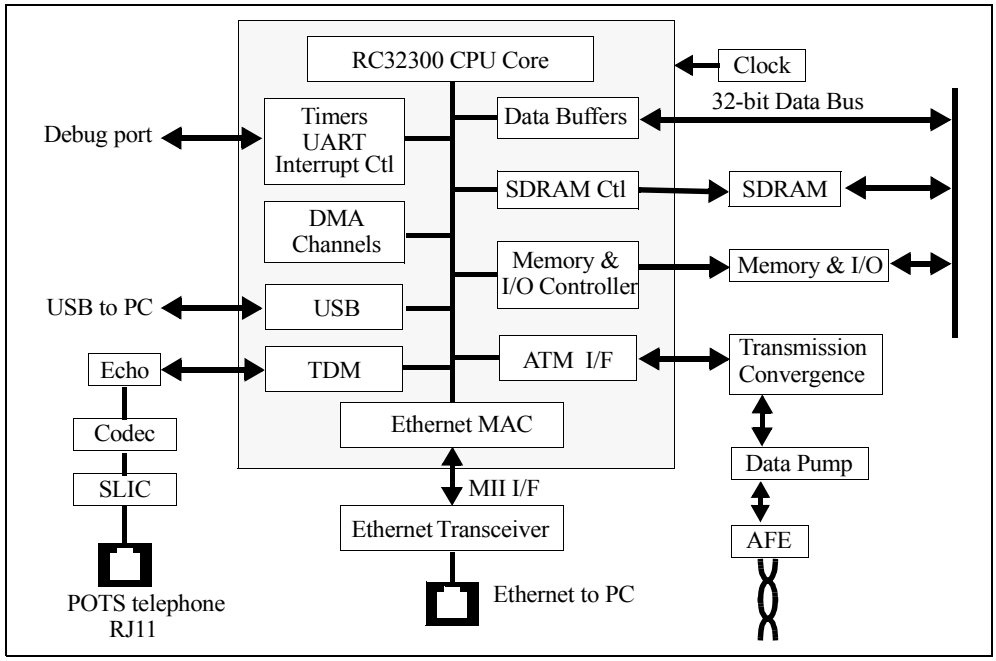


Figure 2 Example of xDSL Residential Gateway Using RC32355

Device Overview

The RC32355 is a “System on a Chip” which contains a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

The RC32355 meets the requirements of various embedded communications and digital consumer applications. It is a single chip solution that incorporates most of the generic system functionalities and application specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

CPU Execution Core

The RC32355 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The DSP instructions enable the RC32300 to implement 33.6 and 56kbps modem functionality in software, removing the need for external dedicated hardware. Cache locking guarantees real-time performance by holding critical DSP code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

Memory and I/O Controller

The RC32355 incorporates a flexible memory and peripheral device controller providing support for SDRAM, Flash ROM, SRAM, dual-port memory, and other I/O devices. It can interface directly to 8-bit boot ROM for a very low cost system implementation. It enables access to very high bandwidth external memory (380 MB/sec peak) at very low system costs. It also offers various trade-offs in cost / performance for the main memory architecture. The timers implemented on the RC32355 satisfy the requirements of most RTOS.

DMA Controller

The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The DMA controller supports scatter / gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

TDM Bus Interface

The RC32355 incorporates an industry standard TDM bus interface to directly access external devices such as telephone CODECs and quality audio A/Ds and D/As. This feature is critical for applications, such as cable modems and xDSL modems, that need to carry voice along with data to support Voice Over IP capability.

Ethernet Interface

The RC32355 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line interface with an MII interface. It supports up to 4 MAC addresses. In a SOHO router, the high performance RC32300 CPU core routes the data between the Ethernet and the ATM interface. In other applications, such as high speed modems, the Ethernet interface can be used to connect to the PC.

USB Device Interface

The RC32355 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC.

ATM SAR

The RC32355 includes a configurable ATM SAR that supports a UTOPIA level 1 or a UTOPIA level 2 interface. The ATM SAR is implemented as a hybrid between software and hardware. A hardware block provides the necessary low level blocks (like CRC generation and checking and cell buffering) while the software is used for higher level SARing functions. In xDSL modem applications, the UTOPIA port interfaces directly to an xDSL chip set. In SOHO routers or in a line card for a Layer 3 switch, it provides access to an ATM network.

Enhanced JTAG Interface for ICE

For low-cost In-Circuit Emulation (ICE), the RC32300 CPU core includes an Enhanced JTAG (EJTAG) interface. This interface consists of two operation modes: Run-Time Mode and Real-Time Mode.

The Run-Time Mode provides a standard JTAG interface for on-chip debugging, and the Real-Time Mode provides additional status pins—PCST[2:0]—which are used in conjunction with the JTAG pins for real-time trace information at the processor internal clock or any division of the pipeline clock.

Name	Type	I/O Type	Description
JTAG_TMS	I	STI	**JTAG Mode Select**. This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 16.
EJTAG_PCST[0]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	**PC trace clock.** This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.
EJTAG_TRST_N	I	STI	**EJTAG Test Reset.** EJTAG_TRST_N is an active-low signal for asynchronous reset of only the EJTAG/ICE controller. EJTAG_TRST_N requires an external pull-up on the board. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary: General Purpose I/O, GPIOP[31] 1st Alternate function: DMA finished output, DMAFIN.
JTAG_TRST_N	I	STI	**JTAG Test Reset.** JTAG_TRST_N is an active-low signal for asynchronous reset of only the JTAG boundary scan controller. JTAG_TRST_N requires an external pull-down on the board that will hold the JTAG boundary scan controller in reset when not in use if selected. JTAG reset enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[2]. 1st Alternate function: UART channel 0 ring indicator, U0RIN.
Debug			
INSTP	O	Low Drive	**Instruction or Data Indicator**. This signal is driven high during CPU instruction fetches and low during CPU data transactions on the memory and peripheral bus.
CPUP	O	Low Drive	**CPU or DMA Transaction Indicator**. This signal is driven high during CPU transactions and low during DMA transactions on the memory and peripheral bus if CPU/DMA Transaction Indicator Enable is enabled. CPU/DMA Status mode enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[4]. 1st Alternate function: UART channel 0 data terminal ready U0DTRN.
DMAP[0]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[23]. 1st Alternate function: TXADDR[1].
DMAP[1]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[25]. 1st Alternate function: RXADDR[1].

Table 1 Pin Descriptions (Part 6 of 8)

Name	Type	I/O Type	Description
U1CTSN	I	STI	**UART channel 1 clear to send.** Primary function: General Purpose I/O, GPIOP[13]. At reset, this pin defaults to primary function GPIOP[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 8 of 8)

1. Schmitt Trigger Input.
2. 2I^2C - Bus Specification by Philips Semiconductors.

Boot Configuration Vector

The boot configuration vector is read into the RC32355 during cold reset. The vector defines parameters in the RC32355 that are essential to operation when cold reset is complete.

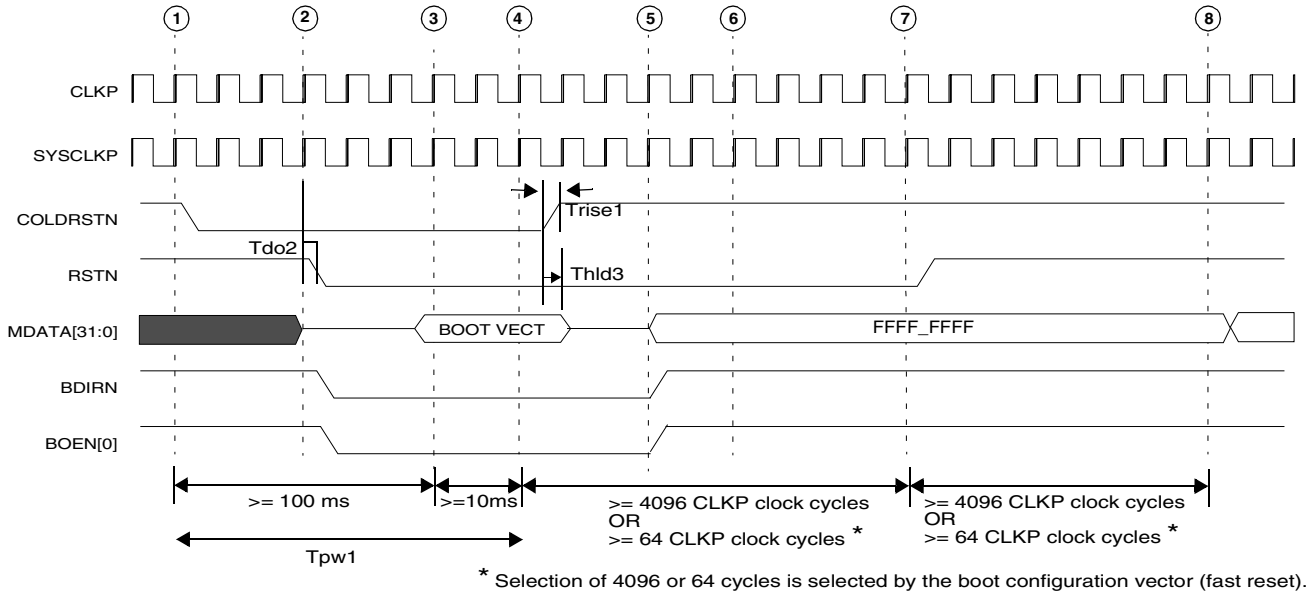
The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Signal	Name/Description
MDATA[2:0]	**Clock Multiplier**. This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	**Endian.** This bit specifies the endianness of RC32355. 0x0 - little endian 0x1 - big endian
MDATA[4]	**Reserved.** Must be set to 0.
MDATA[5]	**Debug Boot Mode**. When this bit is set, the RC32355 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	**Boot Device Width**. This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	**EJTAG/ICE Interface Enable**. When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIOP[31, 13:10] pins behaves as GPIOP 0x1 - GPIOP[31] pin behaves as EJTAG_TRST_N, GPIOP[12:10] pins behave as EJTAG_PCST[2:0], and GPIOP[13] pin behaves as EJTAG_DCLK
MDATA[9]	**Fast Reset**. When this bit is set, RC32355 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32355 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32355 drives RSTN for 64 clock cycles (test only)
MDATA[10]	**DMA Debug Enable**. When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIOP[8, 9, 25, 23] pins behave as GPIOP 0x1 - GPIOP[8, 9, 25, 23] pins behave as DMAP[3:0]

Table 2 Boot Configuration Vector Encoding (Part 1 of 2)

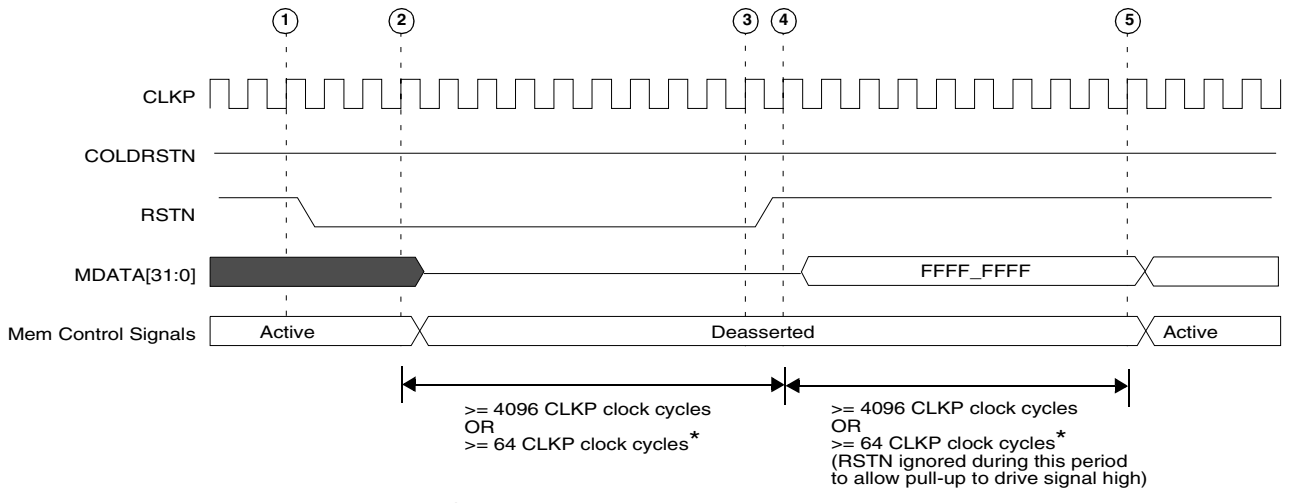
Signal	Name/Description
MDATA[11]	**Hold SYSCLKP Constant**. For systems that do not require a SYSCLKP output and can instead use CLKP, setting this bit to a one causes the SYSCLKP output to be held at a constant level. This may be used to reduce EMI. 0x0 - Allow SYSCLKP to toggle 0x1 - Hold SYSCLKP constant
MDATA[12]	**JTAG Boundary Scan Reset Enable**. When this bit is set, Alternate 2 pin function, JTAG_TRST_N is selected. 0x0 - GPIOP[2] pin behaves as GPIOP 0x1 - GPIOP[2] pin behaves as JTAG_TRST_N
MDATA[13]	**CPU / DMA Transaction Indicator Enable**. When this bit is set, Alternate 2 pin function, CPUP is selected. 0x0 - GPIOP[4] pin behaves as GPIOP 0x1 - GPIOP[4] pin behaves as CPUP
MDATA[15:14]	**Reserved**. These pins must be driven low during boot configuration.

Table 2 Boot Configuration Vector Encoding (Part 2 of 2)



1. COLDRSTN asserted by external logic.
2. The RC32355 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32355 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32355 stops sampling the boot configuration vector.
5. The RC32355 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLKP may be held constant after this point if Hold SYSCLKP Constant is selected in the boot configuration vector.
7. RSTN negated by RC32355.
8. CPU begins executing by taking MIPS reset exception, and the RC32355 starts sampling RSTN as a warm reset input.

Figure 6 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32355 asserts RSTN output low in response.
2. The RC32355 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32355 deasserts RSTN.
4. The RC32355 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Ethernet[1,2]											
MIIRXCLKP, MIITXCLKP	Tperiod1	none	399.96	400.04	399.96	400.04	399.96	400.04	ns	10 Mbps	Figure 13
	Thigh1,Tlow1		140	260	140	260	140	260	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
MIIRXCLKP, MIITXCLKP	Tperiod1	none	39.996	40.004	39.996	40.004	39.996	40.004	ns	100 Mbps	
	Thigh1,Tlow1		14	26	14	26	14	26	ns		
	Trise1,Tfall1		—	2	—	2	—	2	ns		
MIIRXDP[3:0], MIIRXDVP, MIIRXERP	Tsu2	MIIRXCLKP rising	5	—	5	—	5	—	ns		
	Thld2		3	—	3	—	3	—	ns		
MIITXDP[3:0], MIITXENP, MIITXERP	Tdo3	MIITXCLKP rising	7	13	7	13	7	13	ns		
MIIMDCP	Tperiod4	none	30	—	27	—	27	—	ns		
	Thigh4,Tlow4		14	—	13	—	13	—	ns		
	Trise4		—	11	—	11	—	11	ns		
	Tfall4		—	8	—	8	—	8	ns		
MIIMDIOP	Tsu5	MIIMDCP rising	6	—	6	—	6	—	ns		
	Thld5		0.5	—	0.5	—	0.5	—	ns		
	Tdo5		3	7	3	7	3	7	ns		

[1] Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.
[2] MIICOLP and MIICRSP are asynchronous signals.

Table 7 Ethernet AC Timing Characteristics

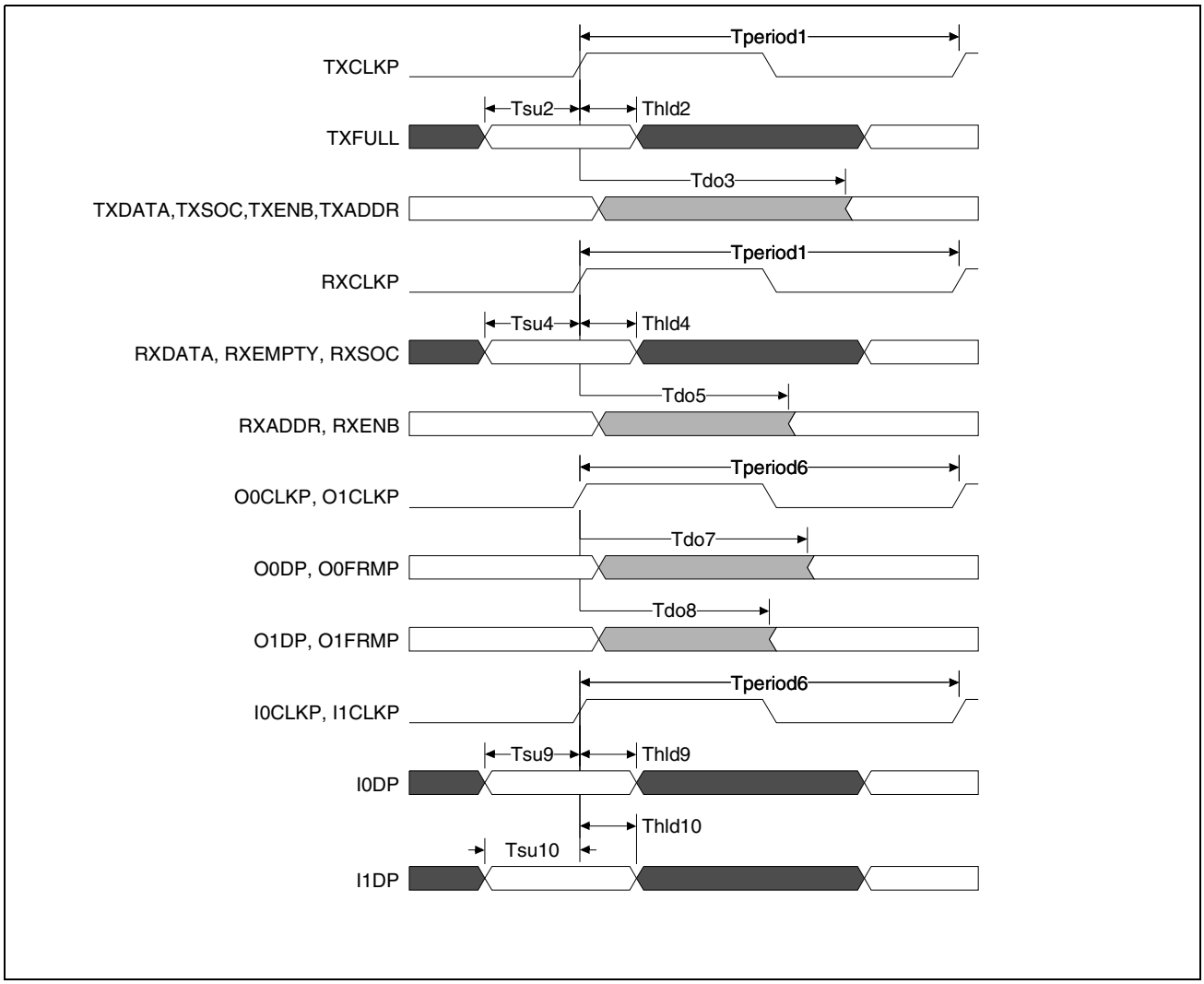


Figure 14 ATM AC Timing Waveform

ATM Pin Name	Utopia Level 1	Utopia Level 2
ATMINP[0]	RXDATA[0]	RXDATA[0]
ATMINP[1]	RXDATA[1]	RXDATA[1]
ATMINP[2]	RXDATA[2]	RXDATA[2]
ATMINP[3]	RXDATA[3]	RXDATA[3]
ATMINP[4]	RXDATA[4]	RXDATA[4]
ATMINP[5]	RXDATA[5]	RXDATA[5]
ATMINP[6]	RXDATA[6]	RXDATA[6]
ATMINP[7]	RXDATA[7]	RXDATA[7]
ATMINP[8]	RXCLKP	RXCLKP
ATMINP[9]	RXEMPTYN	RXEMPTYN
ATMINP[10]	RXSOC	RXSOC
ATMINP[11]	TXFULLN	TXFULLN
ATMIOP[0]	RXENBN	RXENBN
ATMIOP[1]	TXCLKP	TXCLKP
ATMOUTP[0]	TXDATA[0]	TXDATA[0]
ATMOUTP[1]	TXDATA[1]	TXDATA[1]
ATMOUTP[2]	TXDATA[2]	TXDATA[2]
ATMOUTP[3]	TXDATA[3]	TXDATA[3]
ATMOUTP[4]	TXDATA[4]	TXDATA[4]
ATMOUTP[5]	TXDATA[5]	TXDATA[5]
ATMOUTP[6]	TXDATA[6]	TXDATA[6]
ATMOUTP[7]	TXDATA[7]	TXDATA[7]
ATMOUTP[8]	TXSOC	TXSOC
ATMOUTP[9]	TXENBN	TXENBN
GPIOP[22]		TXADDR[0]
GPIOP[23]		TXADDR[1]
GPIOP[24]		RXADDR[0]
GPIOP[25]		RXADDR[1]

Table 9 ATM I/O Pin Multiplexing

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
TDM											
TDMCLKP[1]	Tperiod1	none	—	125	—	62.5	—	62.5	ns		Figure 15 Figure 16
	Thigh1		62.5	—	31.2	—	31.2	—	ns		
	Tlow1		62.5	—	31.2	—	31.2	—	ns		
	Trise1		—	3	—	3	—	3	ns		
	Tfall1		—	3	—	3	—	3	ns		
TDMFP	Tsu2	TDMCLKP rising or falling	4	—	4	—	4	—	ns		
	Thld2		1	—	1	—	1	—	ns		
	Tdo2		2	9	2	9	2	9	ns		
TDMDIP	Tsu3	TDMCLKP rising or falling	4	—	4	—	4	—	ns		
	Thld3		1	—	1	—	1	—	ns		
TDMDOP	Tdo4	TDMCLKP rising or falling	2	9	2	9	2	9	ns		
	Tdz4		—	12	—	12	—	12	ns		
	Tzd4		3	—	3	—	3	—	ns		
TDMTEN	Tdo5	TDMCLKP rising or falling	2	9	2	9	2	9	ns		

[1]The rising or falling edge of TDMCLKP is used as the reference clock edge for the timing depending on the TDM bus mode and protocol selection.

Table 10 TDM AC Timing Characteristics

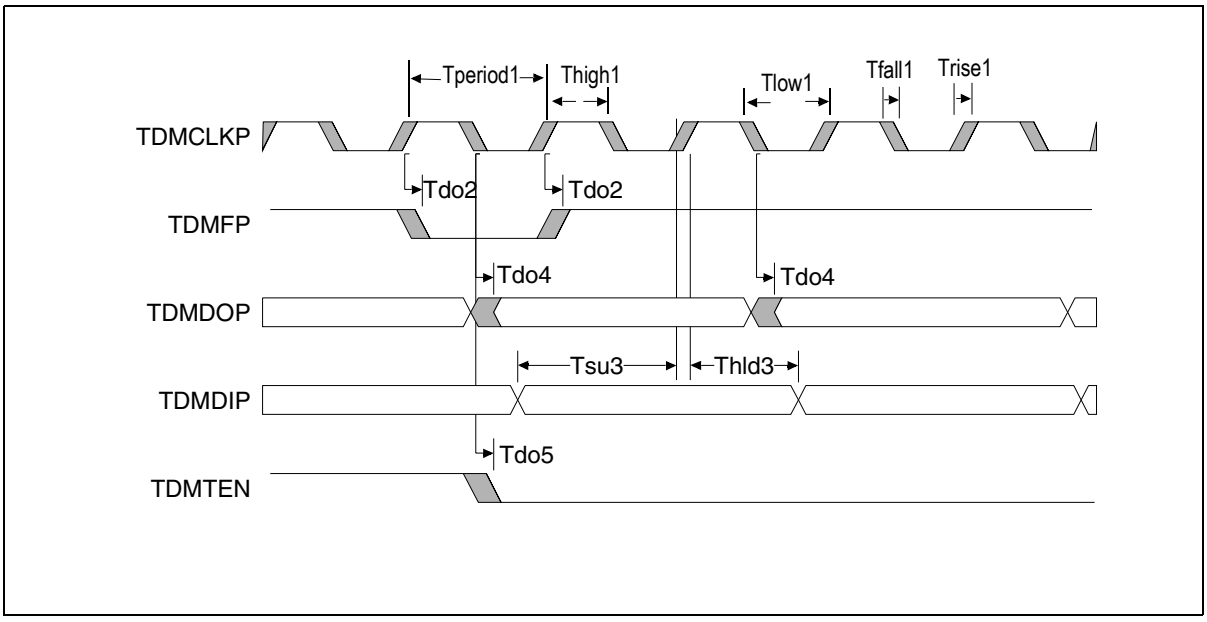


Figure 15 TDM AC Timing Waveform, Master Mode

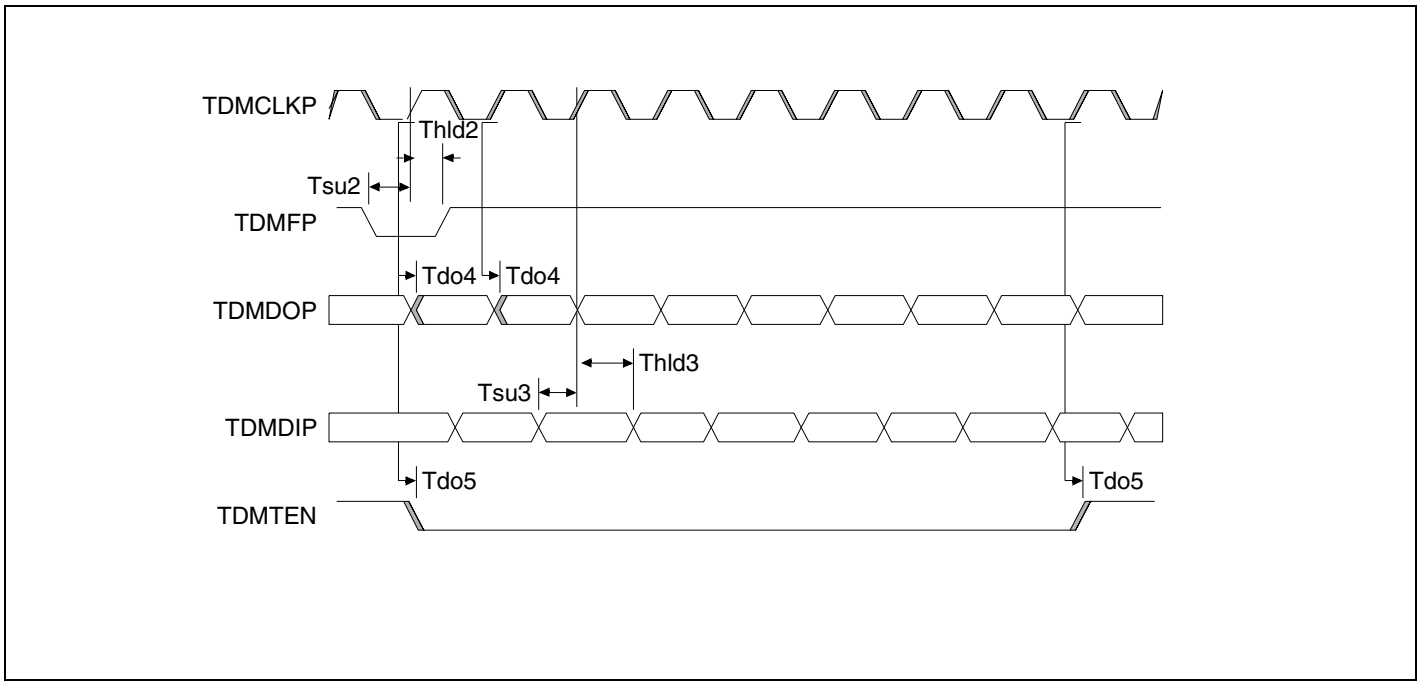


Figure 16 TDM AC Timing Waveform, Slave Mode

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
USB											
USBCLKP[1]	Tperiod1	none	19.79	21.87	19.79	21.87	19.79	21.87	ns		Figure 17
	Thigh1,Tlow1		8.3	—	8.3	—	8.3	—	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
	Tjitter1		—	0.8	—	0.8	—	0.8	ns	1/4th of the minimum Source data jitter	
USBDN, USBDP	Trise2		4	20	4	20	4	20	ns	Universal Serial Bus Specification (USBS) Revision 1.1: Figures 7.6 and 7.7.	
	Tfall2		4	20	4	20	4	20	ns	USBS Revision 1.1: Figures 7.6 and 7.7.	
USBDN and USBDP Rise and Fall Time Matching			90	111.11	90	111.11	90	111.11	%	USBS Revision 1.1: Note 10, Section 7.1.2.	
Data valid period	Tstate		60	—	60	—	60	—	ns		
Skew between USBDN and USBDP			—	0.4	—	0.4	—	0.4	ns	USBS Revision 1.1: Section 7.1.3	
Source data jitter			—	3.5	—	3.5	—	3.5	ns	USBS Revision 1.1: Table 7-6	
Receive data jitter			—	12	—	12	—	12	ns		
Source EOP length	Tseop		160	175	160	175	160	175	ns		
Receive EOP length	Treop		82	—	82	—	82	—	ns		
EOP jitter			-2	5	-2	5	-2	5	ns		
Full-speed Data Rate	Tfdrate		11.97	12.03	11.97	12.03	11.97	12.03	MHz	Average bit rate, USBS Section 7.1.11.	
Frame Interval			0.9995	1.0005	0.9995	1.0005	0.9995	1.0005	ms	USBS Section 7.1.12.	
Consecutive Frame Interval Jitter			—	42	—	42	—	42	ns	Without frame adjustment.	
			—	126	—	126	—	126	ns	With frame adjustment.	

[1] USB clock (USBCLKP) frequency must be less than CLKP frequency.

Table 11 USB AC Timing Characteristics

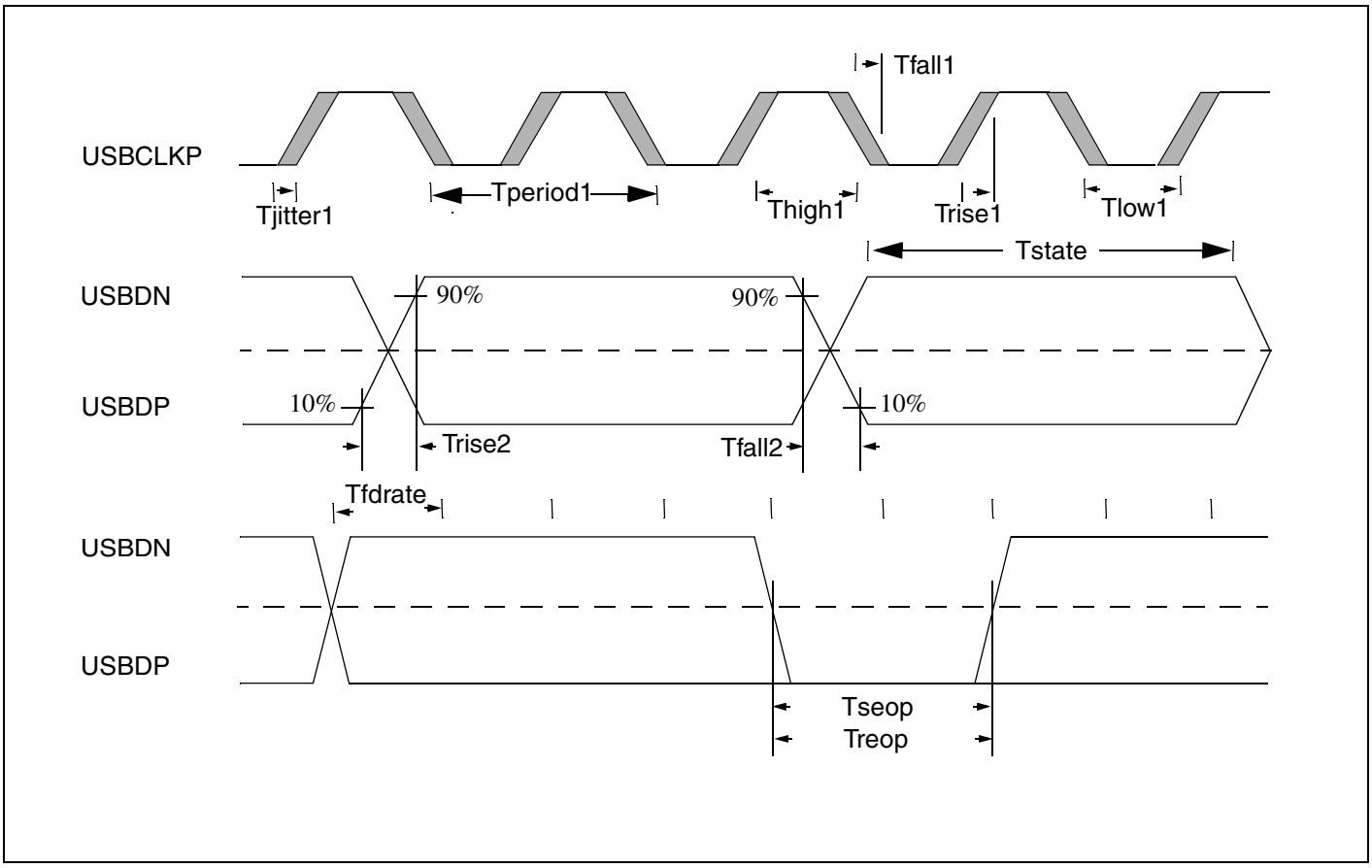


Figure 17 USB AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
UART											
U0SINP, U0RIN, U0DCDN, U0DSRN, U0CTSN, U1SINP, U1DSRN, U1CTSN	Tsu[1]	CLKP rising	5	—	5	—	5	—	ns		
	Thld[1]		3	—	3	—	3	—	ns		
U0SOUTP, U0DTRN, U0RTSN, U1SOUTP, U1DTRN, U1RTSN	Tdo[1]	CLKP rising	1	12	1	12	1	12	ns		
[1] These are asynchronous signals and the values are provided for ATE (test) only.											

Table 12 UART AC Timing Characteristics

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
EJTAG and JTAG											
JTAG_TCK	Tperiod1	none	100	—	100	—	100	—	ns		Figure 20
	Thigh1, Tlow1		40	—	40	—	40	—	ns		
	Trise1, Tfall1		—	5	—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	7.5	10.0	6.7	10.0	5.6	10.0	ns		
	Thigh2, Tlow2		2.5	—	2.5	—	2.5	—	ns		
	Trise2, Tfall2		—	3.5	—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2	12.0	2	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 15 JTAG AC Timing Characteristics

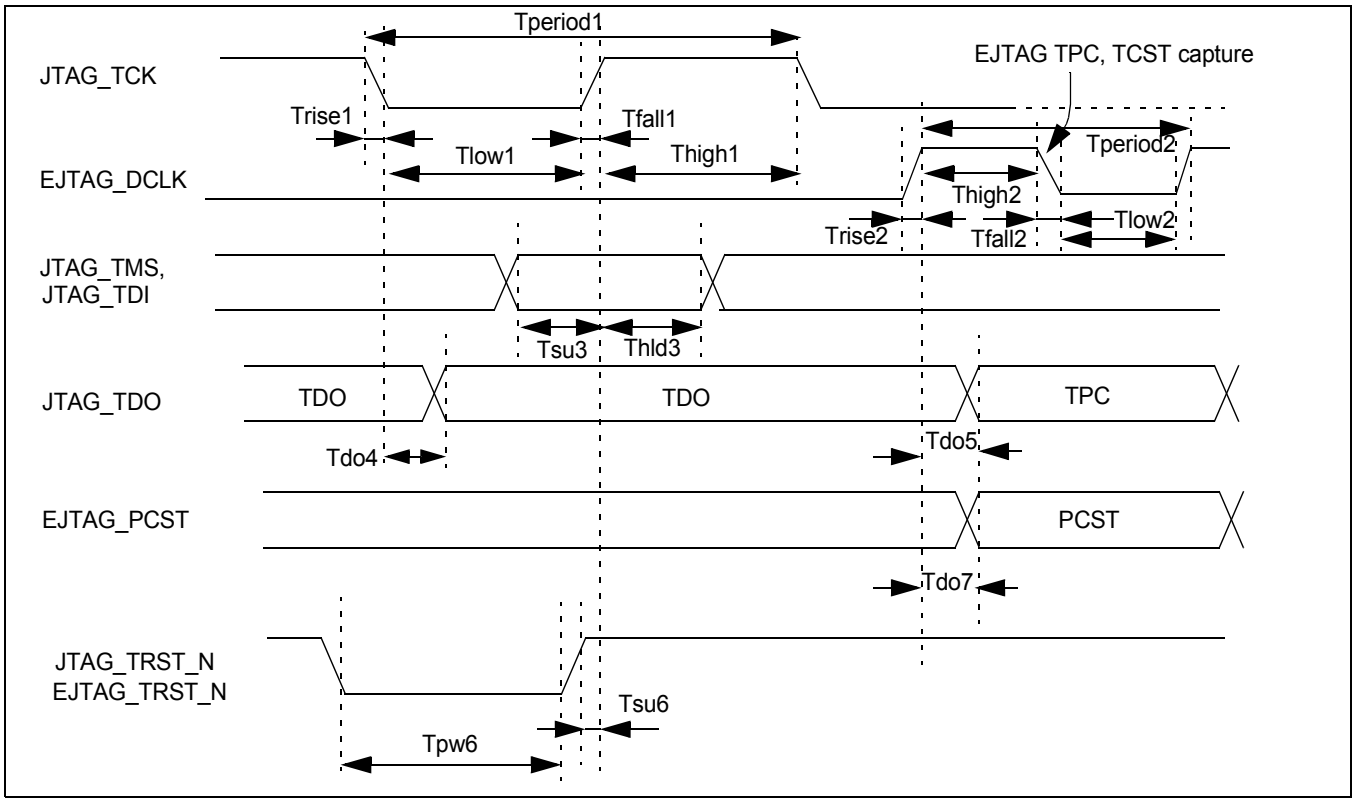


Figure 20 JTAG AC Timing Waveform

Phase-Locked Loop (PLL)

The processor aligns the pipeline clock, PClock, to the master input clock (CLKP) by using an internal phase-locked loop (PLL) circuit that generates aligned clocks. Inherently, PLL circuits are only capable of generating aligned clocks for master input clock (CLKP) frequencies within a limited range.

PLL Analog Filter

The storage capacitor required for the Phase-Locked Loop circuit is contained in the RC32355. However, it is recommended that the system designer provide a filter network of passive components for the PLL power supply.

VccP (PLL circuit power) and VssP (PLL circuit ground) should be isolated from Vcc Core (core power) and Vss (common ground) with a filter circuit such as the one shown in Figure 22.

Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

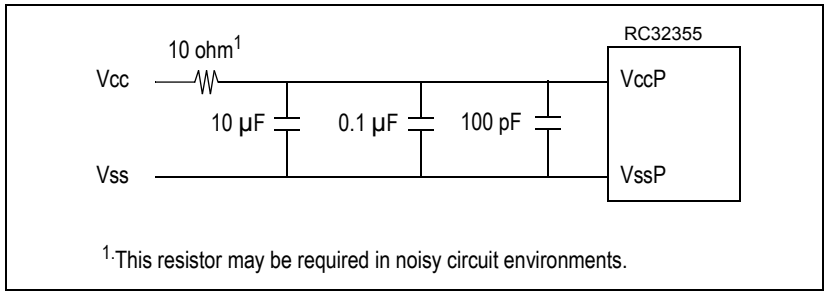


Figure 22 PLL Filter Circuit for Noisy Environments

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V_{ss}[1] V_{ssP}[5]	$V_{cc}I/O$[2]	$V_{cc}Core$[3] $V_{cc}P$[4]
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%
Industrial	-40°C+ 85°C Ambient	0V	3.3V±5%	2.5V±5%

[1] Vss supplies a common ground.
[2] VccI/O is the I/O power.
[3] VccCore is the internal logic power.
[4] VccP is the phase lock loop power.
[5] VssP is the phase lock loop ground.

Table 17 Temperature and Voltage

Capacitive Load Deration

Refer to the RC32355 IBIS Model which can be found at the IDT web site (www.idt.com).

Power-on RampUp

The 2.5V core supply (and 2.5V V_{cc}PLL supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

DC Electrical Characteristics

($T_{ambient}$ = 0°C to +70°C Commercial, $T_{ambient}$ = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%, V_{cc} Core and V_{cc} P = +2.5V±5%)

	Para-meter	Min	Max	Unit	Pin Numbers	Conditions
LOW Drive Output with Schmitt Trigger Input (STI)	I_{OL}	7.3	—	mA	1-4,6-8,10-16,18,20-25,27-29,32,33,35-37, 39-42,44,46-48,50,52,53,56,58-60,62-69, 71-77,82-85,87-94,96-99,101-105,167, 205-208	V_{OL} = 0.4V
	I_{OH}	-8.0	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
HIGH Drive Output with Standard Input	I_{OL}	9.4	—	mA	49,51,54,55,106-108,110,112-117,119, 121,123-128,130,132-137,139,141,143, 150,152,154-159,161,163-166,168-170, 172,174-179,181,185-190,192,194-200, 202,204	V_{OL} = 0.4V
	I_{OH}	-15	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
Clock Drive Output	I_{OL}	39	—	mA	183	V_{OL} = 0.4V
	I_{OH}	-24	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
Capacitance	C_{IN}	—	10	pF	All pins	—
Leakage	I/O_{LEAK}	—	20	µA	All pins	—

Table 18 DC Electrical Characteristics

Power Curve

The following graph contains a power curve that shows power consumption at various bus frequencies.

Note: The system clock (CLKP) can be multiplied by 2, 3, or 4 to obtain the CPU pipeline clock (PClock) speed.

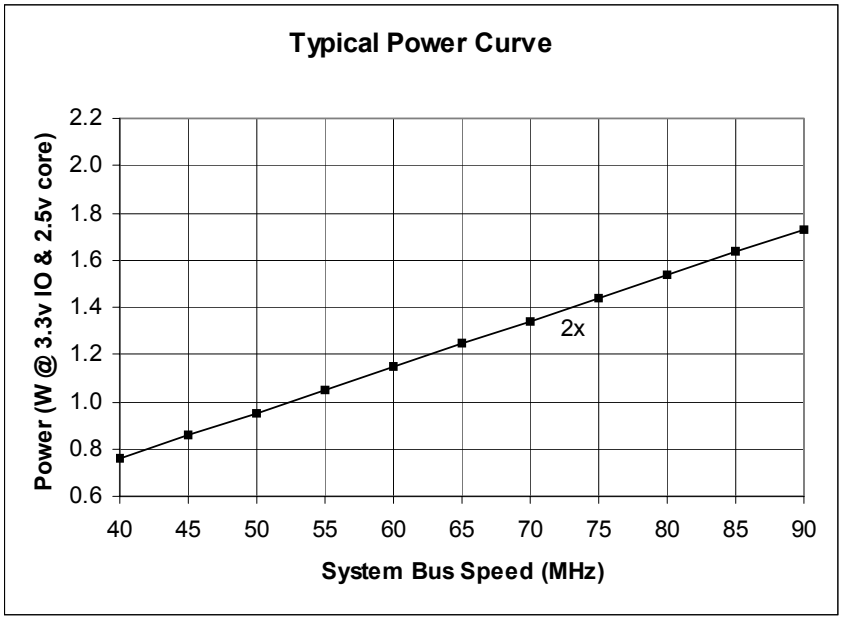


Figure 23 Typical Power Usage

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O Supply Voltage	-0.3	3.465	V
V_{CC}Core	Core Supply Voltage	-0.3	3.0	V
V_{CC}P	PLL Supply Voltage	-0.3	3.0	V
Vimin	Input Voltage - undershoot	-0.6	—	V
Vi	I/O Input Voltage	Gnd	V_{CC}I/O+0.6	V
Ta, Industrial	Ambient Operating Temperature	-40	85	degrees C
Tstg	Storage Temperature	-40	125	degrees C

Table 21 Absolute Maximum Ratings

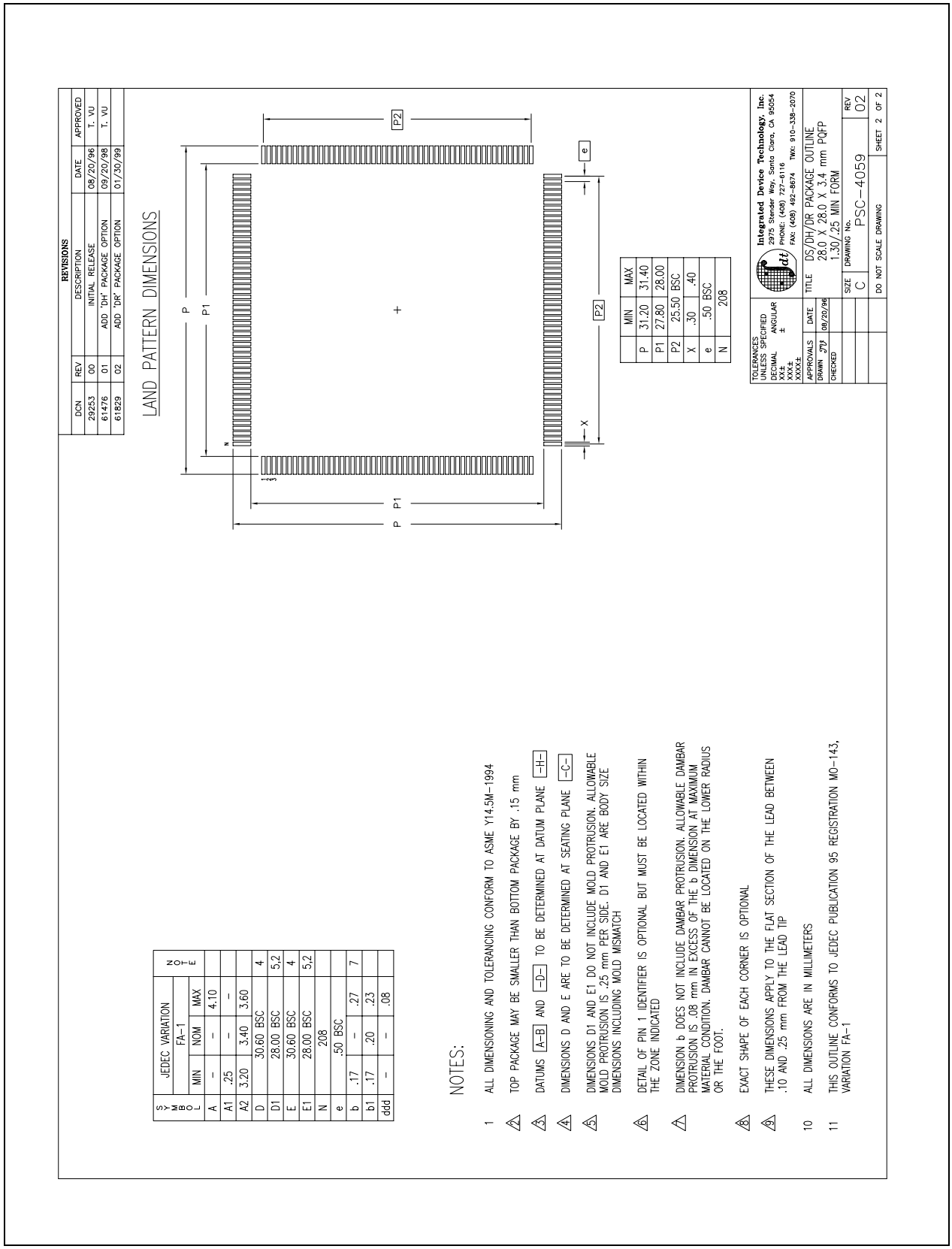
1. Functional and tested operating conditions are given in Table 17. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Alternate Pin Functions

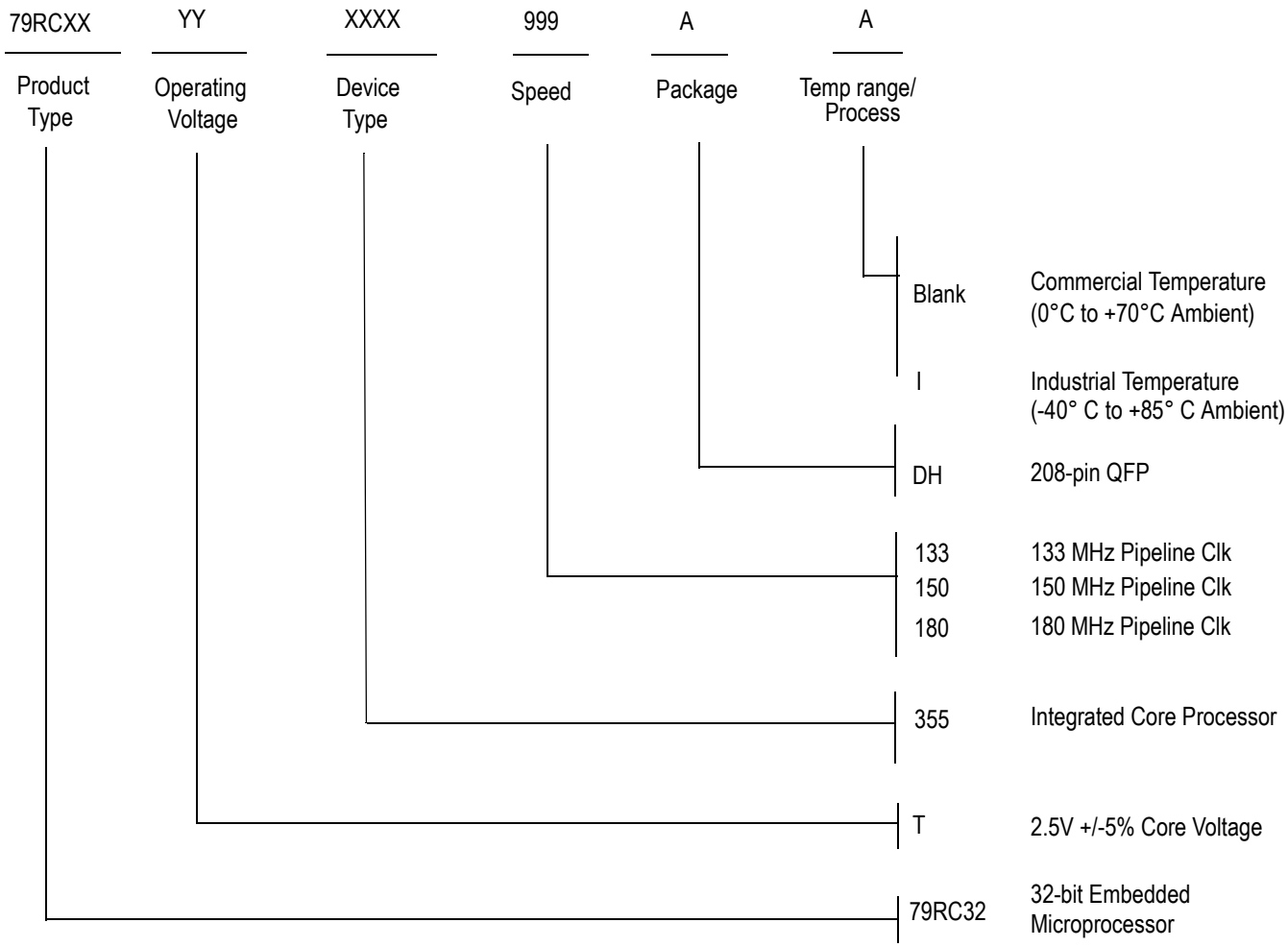
Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		51	GPIOP[32]	TDMDOP	
21	GPIOP[01]	U0SINP		54	GPIOP[16]	CSN[4]	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	55	GPIOP[17]	CSN[5]	
24	GPIOP[03]	U0DCRN		56	GPIOP[18]	DMAREQN	
27	GPIOP[04]	U0DTRN	CPUP	59	GPIOP[19]	DMADONEN	
28	GPIOP[05]	U0DSRN		60	GPIOP[20]	USBSOF	
33	GPIOP[06]	U0RTSN		62	GPIOP[21]	CKENP	
35	GPIOP[07]	U0CTSN		64	GPIOP[22]	TXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	65	GPIOP[23]	TXADDR[1]	DMAP[0]
39	GPIOP[09]	U1SINP	DMAP[2]	66	GPIOP[24]	RXADDR[0]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	69	GPIOP[26]	TDMTEN	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	71	GPIOP[27]	MADDR[22]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	73	GPIOP[28]	MADDR[23]	
46	GPIOP[14]	SDAP		74	GPIOP[29]	MADDR[24]	
47	GPIOP[15]	SCLP		75	GPIOP[30]	MADDR[25]	
48	GPIOP[35]	TDMCLKP		76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
49	GPIOP[34]	TDMFP					
50	GPIOP[33]	TDMDIP					

Table 23 Alternate Pin Functions

Package Drawing - page two



Ordering Information



Valid Combinations

79RC32T355 -133DH, 150DH, 180DH	208-pin QFP package, Commercial Temperature
79RC32T355 -133DHI, 150DHI	208-pin QFP package, Industrial Temperature

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