Renesas Electronics America Inc - IDT79RC32T355-150DHG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t355-150dhg

Device Overview

The RC32355 is a “System on a Chip” which contains a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

The RC32355 meets the requirements of various embedded communications and digital consumer applications. It is a single chip solution that incorporates most of the generic system functionalities and application specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

CPU Execution Core

The RC32355 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The DSP instructions enable the RC32300 to implement 33.6 and 56kbps modem functionality in software, removing the need for external dedicated hardware. Cache locking guarantees real-time performance by holding critical DSP code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

Memory and I/O Controller

The RC32355 incorporates a flexible memory and peripheral device controller providing support for SDRAM, Flash ROM, SRAM, dual-port memory, and other I/O devices. It can interface directly to 8-bit boot ROM for a very low cost system implementation. It enables access to very high bandwidth external memory (380 MB/sec peak) at very low system costs. It also offers various trade-offs in cost / performance for the main memory architecture. The timers implemented on the RC32355 satisfy the requirements of most RTOS.

DMA Controller

The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The DMA controller supports scatter / gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

TDM Bus Interface

The RC32355 incorporates an industry standard TDM bus interface to directly access external devices such as telephone CODECs and quality audio A/Ds and D/As. This feature is critical for applications, such as cable modems and xDSL modems, that need to carry voice along with data to support Voice Over IP capability.

Ethernet Interface

The RC32355 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line interface with an MII interface. It supports up to 4 MAC addresses. In a SOHO router, the high performance RC32300 CPU core routes the data between the Ethernet and the ATM interface. In other applications, such as high speed modems, the Ethernet interface can be used to connect to the PC.

USB Device Interface

The RC32355 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC.

ATM SAR

The RC32355 includes a configurable ATM SAR that supports a UTOPIA level 1 or a UTOPIA level 2 interface. The ATM SAR is implemented as a hybrid between software and hardware. A hardware block provides the necessary low level blocks (like CRC generation and checking and cell buffering) while the software is used for higher level SARing functions. In xDSL modem applications, the UTOPIA port interfaces directly to an xDSL chip set. In SOHO routers or in a line card for a Layer 3 switch, it provides access to an ATM network.

Enhanced JTAG Interface for ICE

For low-cost In-Circuit Emulation (ICE), the RC32300 CPU core includes an Enhanced JTAG (EJTAG) interface. This interface consists of two operation modes: Run-Time Mode and Real-Time Mode.

The Run-Time Mode provides a standard JTAG interface for on-chip debugging, and the Real-Time Mode provides additional status pins—PCST[2:0]—which are used in conjunction with the JTAG pins for real-time trace information at the processor internal clock or any division of the pipeline clock.

Thermal Considerations

The RC32355 consumes less than 2.5 W peak power. It is guaranteed in a ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

March 29, 2001: Initial publication.

September 24, 2001: Removed references to DPI interface. Removed references to “edge-triggered interrupt input” for GPIO pins. Changed 208-pin package designation from DP to DH.

October 10, 2001: Revised AC timing characteristics in Tables 5, 6, 7, 8, 10, 12, and 15. Revised values in Table 18, “DC Electrical Characteristics”; Table 20, “RC32355 Power Consumption”; and Figure 23, “Typical Power Usage.” Changed data sheet from Preliminary to Final.

October 23, 2001: Revised Figure 23, “Typical Power Usage.”

November 1, 2001: Added Input Voltage Undershoot parameter and a footnote to Table 21.

January 30, 2002: In Table 6, changed values from 1.5 to 1.2 for the following signals: MDATA Tdo1, MADDR Tdo2, CASN Tdo3, CKENP Tdo4, BDIRN Tdo5, BOEN Tdo6.

May 20, 2002: Changed values in Table 20, Power Consumption.

September 19, 2002: Added COLDRSTN Trise1 parameter to Table 5, Reset and System AC Timing Characteristics.

December 6, 2002: In Features section, changed UART speed from 115 Kb/s to 1.5 Mb/s.

December 17, 2002: Added V_{OH} parameter to Table 18, DC Electrical Characteristics.

January 27, 2004: Added 180MHz speed grade.

May 25, 2004: In Table 7, signals MIIRXCLK and MIITXCLK, the Min and Max values for 10 Mbps Thigh1/Tlow1 were changed to 140 and 260 respectively and the Min and Max values for 100 Mbps Thigh1/Tlow1 were changed to 14.0 and 26.0 respectively.

Name	Type	I/O Type	Description
TDMTEN	O	Low Drive	**TDM External Buffer Enable.** This signal controls an external tri-state buffer output enable connected to the TDM output data, TDMDOP. It is asserted low when the RC32355 is driving data on TDMDOP. Primary function: General Purpose I/O, GPIOP[26]
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
GPIOP[5]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data set ready, U0DSRN.
GPIOP[6]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 request to send, U0RTSN.
GPIOP[7]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 clear to send, U0CTSN.
GPIOP[8]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial output, U1SOUTP. 2nd Alternate function: Active DMA channel code, DMAP[3].
GPIOP[9]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial input, U1SINP. 2nd Alternate function: Active DMA channel code, DMAP[2].
GPIOP[10]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[0].
GPIOP[11]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data set ready, U1DSRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[1].
GPIOP[12]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 request to send, U1RTSN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[2].
GPIOP[13]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 clear to send, U1CTSN. 2nd Alternate function: ICE PC trace clock, EJTAG_DCLK.
GPIOP[14]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface data, SDAP.
GPIOP[15]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface clock, SCLP.
GPIOP[16]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[4].

Table 1 Pin Descriptions (Part 3 of 8)

Name	Type	I/O Type	Description
GPIOP[17]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[5].
GPIOP[18]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: External DMA device request, DMAREQN.
GPIOP[19]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: External DMA device done, DMADONEN.
GPIOP[20]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: USB start of frame, USBSOF.
GPIOP[21]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: SDRAM clock enable CKENP.
GPIOP[22]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: ATM transmit PHY address, TXADDR[0].
GPIOP[23]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: ATM transmit PHY address, TXADDR[1]. 2nd Alternate function: Active DMA channel code, DMAP[0].
GPIOP[24]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: ATM receive PHY address, RXADDR[0].
GPIOP[25]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: ATM receive PHY address, RXADDR[1]. 2nd Alternate function: Active DMA channel code, DMAP[1].
GPIOP[26]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM external buffer enable, TDMTEN.
GPIOP[27]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[22].
GPIOP[28]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[23].
GPIOP[29]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[24].
GPIOP[30]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[25].
GPIOP[31]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1ST Alternate function: DMA finished, DMAFIN. 2nd Alternate function: EJTAG/ICE reset, EJTAG_TRST_N.
GPIOP[32]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface data output, TDMDOP. At reset, this pin defaults to the primary function, GPIOP[32].
GPIOP[33]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface data input, TDMDIP. At reset, this pin defaults to the primary function, GPIOP[33].
GPIOP[34]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface frame signal, TDMFP. At reset, this pin defaults to the primary function, GPIOP[34].
GPIOP[35]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: TDM interface clock, TDMCLKP. At reset, this pin defaults to the primary function, GPIOP[35].
DMA			
DMAFIN	O	Low	**External DMA finished.** This signal is asserted low by the RC32355 when the number of bytes specified in the DMA descriptor have been transferred to or from an external device. Primary function: General Purpose I/O, GPIOP[31]. At reset, this pin defaults to primary function GPIOP[31]. 2nd Alternate function: EJTAG_TRST_N.

Table 1 Pin Descriptions (Part 4 of 8)

Name	Type	I/O Type	Description
JTAG_TMS	I	STI	**JTAG Mode Select**. This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 16.
EJTAG_PCST[0]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	**PC trace clock.** This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.
EJTAG_TRST_N	I	STI	**EJTAG Test Reset.** EJTAG_TRST_N is an active-low signal for asynchronous reset of only the EJTAG/ICE controller. EJTAG_TRST_N requires an external pull-up on the board. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 16. Primary: General Purpose I/O, GPIOP[31] 1st Alternate function: DMA finished output, DMAFIN.
JTAG_TRST_N	I	STI	**JTAG Test Reset.** JTAG_TRST_N is an active-low signal for asynchronous reset of only the JTAG boundary scan controller. JTAG_TRST_N requires an external pull-down on the board that will hold the JTAG boundary scan controller in reset when not in use if selected. JTAG reset enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[2]. 1st Alternate function: UART channel 0 ring indicator, U0RIN.
Debug			
INSTP	O	Low Drive	**Instruction or Data Indicator**. This signal is driven high during CPU instruction fetches and low during CPU data transactions on the memory and peripheral bus.
CPUP	O	Low Drive	**CPU or DMA Transaction Indicator**. This signal is driven high during CPU transactions and low during DMA transactions on the memory and peripheral bus if CPU/DMA Transaction Indicator Enable is enabled. CPU/DMA Status mode enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[4]. 1st Alternate function: UART channel 0 data terminal ready U0DTRN.
DMAP[0]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[23]. 1st Alternate function: TXADDR[1].
DMAP[1]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[25]. 1st Alternate function: RXADDR[1].

Table 1 Pin Descriptions (Part 6 of 8)

Name	Type	I/O Type	Description
U1CTSN	I	STI	**UART channel 1 clear to send.** Primary function: General Purpose I/O, GPIOP[13]. At reset, this pin defaults to primary function GPIOP[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 8 of 8)

1. Schmitt Trigger Input.
2. 2I^2C - Bus Specification by Philips Semiconductors.

Boot Configuration Vector

The boot configuration vector is read into the RC32355 during cold reset. The vector defines parameters in the RC32355 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Signal	Name/Description
MDATA[2:0]	**Clock Multiplier**. This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	**Endian.** This bit specifies the endianness of RC32355. 0x0 - little endian 0x1 - big endian
MDATA[4]	**Reserved.** Must be set to 0.
MDATA[5]	**Debug Boot Mode**. When this bit is set, the RC32355 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	**Boot Device Width**. This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	**EJTAG/ICE Interface Enable**. When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIOP[31, 13:10] pins behaves as GPIOP 0x1 - GPIOP[31] pin behaves as EJTAG_TRST_N, GPIOP[12:10] pins behave as EJTAG_PCST[2:0], and GPIOP[13] pin behaves as EJTAG_DCLK
MDATA[9]	**Fast Reset**. When this bit is set, RC32355 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32355 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32355 drives RSTN for 64 clock cycles (test only)
MDATA[10]	**DMA Debug Enable**. When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIOP[8, 9, 25, 23] pins behave as GPIOP 0x1 - GPIOP[8, 9, 25, 23] pins behave as DMAP[3:0]

Table 2 Boot Configuration Vector Encoding (Part 1 of 2)

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

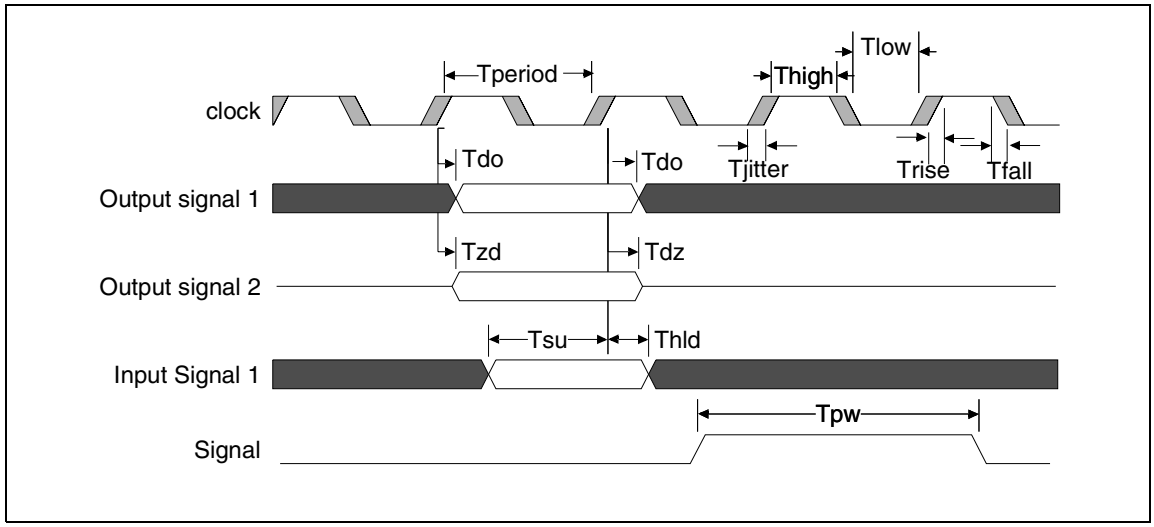


Figure 5 AC Timing Definitions Waveform

Symbol	Definition
Tperiod	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active.

Table 4 AC Timing Definitions

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - SDRAM Access											
MDATA[31:0]	Tsu1	SDCLKINP rising	2.5	—	2.5	—	2.5	—	ns		Figure 8 Figure 9 Figure 10
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1	SYSCLKP rising	1.2	5.8	1.2	5.8	1.2	5.8	ns		
	Tdz1		—	5.0	—	5.0	—	5.0	ns		
	Tzd1		1.0	—	1.0	—	1.0	—	ns		
MADDR[20:2], BWEN[3:0]	Tdo2	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CASN, RASN, SDCSN[1:0], SDWEN	Tdo3	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CKENP	Tdo4	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BDIRN	Tdo5	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BOEN[1:0]	Tdo6	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
SYSCLKP rising	Tdo7	CLKP rising	0.5	5.0	0.5	5.0	0.5	5.0	ns		
SDCLKINP	Tperiod8	none	15	50	13.3	50	13.3	50	ns		
	Thigh8,Tlow8		6.0	—	5.4	—	5.4	—	ns		
	Trise8,Tfall8		—	3.0	—	2.5	—	2.5	ns		
	Tdelay8	SYSCLKP rising	0	4.8	0	4.8	0	4.8	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - Device Access											
MDATA[31:0]	Tsu1	CLKP rising	2.5	—	2.5	—	2.5	—	ns		Figure 11 Figure 12
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1		2.0	6.5	2.0	6.5	2.0	6.5	ns		
	Tdz1		—	9.0	—	9.0	—	9.0	ns		
	Tzd1		2.0	—	2.0	—	2.0	—	ns		
WAITACKN, BRN	Tsu	CLKP rising	2.5	—	2.5	—	2.5	—	ns		
	Thld		1.5	—	1.5	—	1.5	—	ns		
MADDR[21:0]	Tdo2	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz2		—	9.0	—	9.0	—	9.0	ns		
	Tzd2		2.0	—	2.0	—	2.0	—	ns		
MADDR[25:22]	Tdo3	CLKP rising	2.5	6.5	2.5	6.5	2.5	6.5	ns		
	Tdz3		—	9.0	—	9.0	—	9.0	ns		
	Tzd3		2.0	—	2.0	—	2.0	—	ns		
BDIRN, BOEN[0]	Tdo4	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz4		—	9.0	—	9.0	—	9.0	ns		
	Tzd4		2.0	—	2.0	—	2.0	—	ns		
BGN, BWEN[3:0], OEN, RWN	Tdo5	CLKP rising	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz5		—	9.0	—	9.0	—	9.0	ns		
	Tzd5		2.0	—	2.0	—	2.0	—	ns		
CSN[3:0]	Tdo6	CLKP rising	1.7	5.0	1.7	5.0	1.7	5.0	ns		
	Tdz6		—	9.0	—	9.0	—	9.0	ns		
	Tzd6		2.0	—	2.0	—	2.0	—	ns		
CSN[5:4]	Tdo7	CLKP rising	2.5	6.0	2.5	6.0	2.5	6.0	ns		
	Tdz7		—	9.0	—	9.0	—	9.0	ns		
	Tzd7		2.0	—	2.0	—	2.0	—	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

Note: The RC32355 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32355 are both driving. See the chapters “Device Controller,” “Synchronous DRAM Controller,” and “Bus Arbitration” in the RC32355 User Reference Manual.

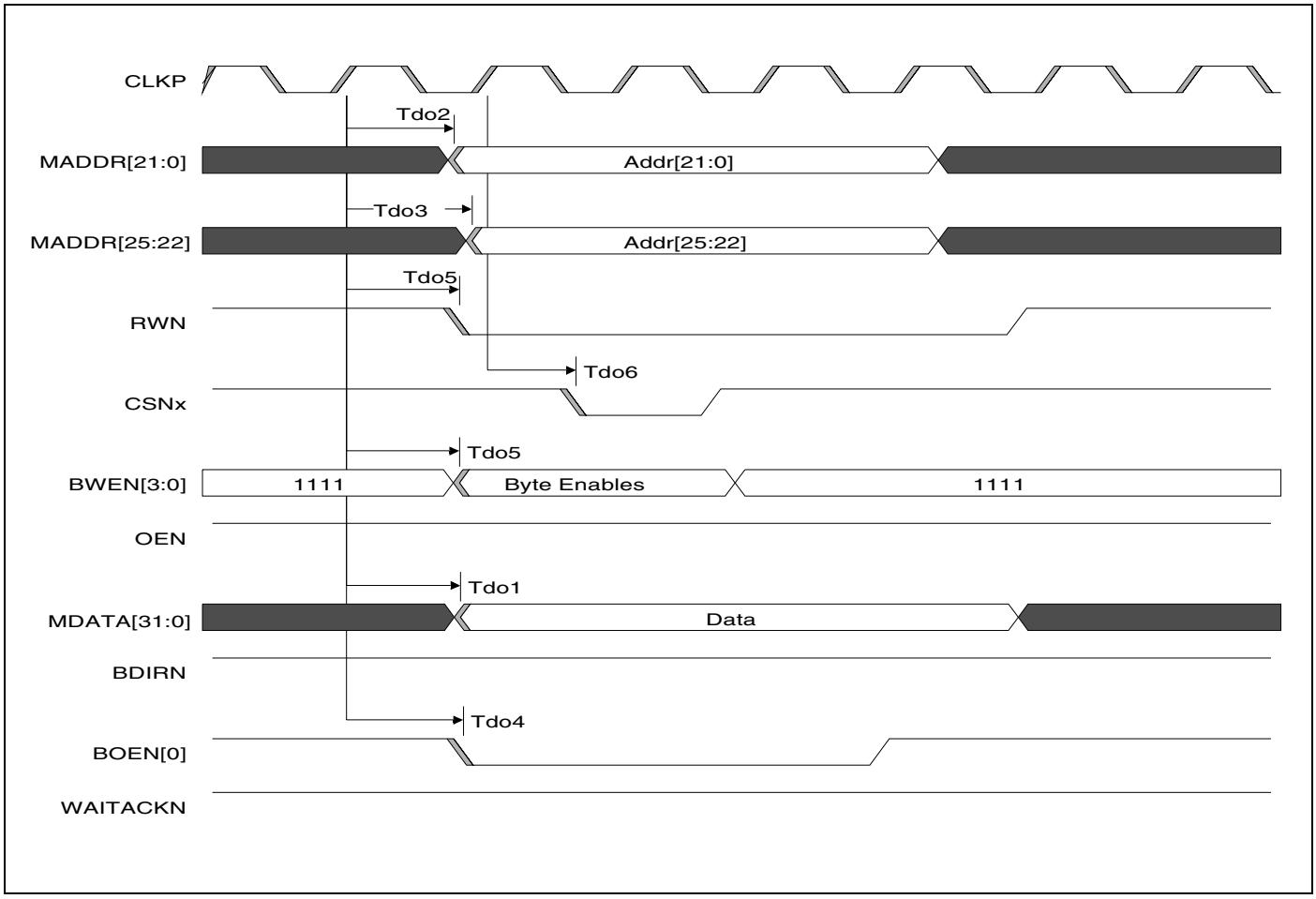


Figure 12 Memory AC and Peripheral Bus Timing Waveform - Device Write Access

ATM Pin Name	Utopia Level 1	Utopia Level 2
ATMINP[0]	RXDATA[0]	RXDATA[0]
ATMINP[1]	RXDATA[1]	RXDATA[1]
ATMINP[2]	RXDATA[2]	RXDATA[2]
ATMINP[3]	RXDATA[3]	RXDATA[3]
ATMINP[4]	RXDATA[4]	RXDATA[4]
ATMINP[5]	RXDATA[5]	RXDATA[5]
ATMINP[6]	RXDATA[6]	RXDATA[6]
ATMINP[7]	RXDATA[7]	RXDATA[7]
ATMINP[8]	RXCLKP	RXCLKP
ATMINP[9]	RXEMPTYN	RXEMPTYN
ATMINP[10]	RXSOC	RXSOC
ATMINP[11]	TXFULLN	TXFULLN
ATMIOP[0]	RXENBN	RXENBN
ATMIOP[1]	TXCLKP	TXCLKP
ATMOUTP[0]	TXDATA[0]	TXDATA[0]
ATMOUTP[1]	TXDATA[1]	TXDATA[1]
ATMOUTP[2]	TXDATA[2]	TXDATA[2]
ATMOUTP[3]	TXDATA[3]	TXDATA[3]
ATMOUTP[4]	TXDATA[4]	TXDATA[4]
ATMOUTP[5]	TXDATA[5]	TXDATA[5]
ATMOUTP[6]	TXDATA[6]	TXDATA[6]
ATMOUTP[7]	TXDATA[7]	TXDATA[7]
ATMOUTP[8]	TXSOC	TXSOC
ATMOUTP[9]	TXENBN	TXENBN
GPIOP[22]		TXADDR[0]
GPIOP[23]		TXADDR[1]
GPIOP[24]		RXADDR[0]
GPIOP[25]		RXADDR[1]

Table 9 ATM I/O Pin Multiplexing

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
TDM											
TDMCLKP[1]	Tperiod1	none	—	125	—	62.5	—	62.5	ns		Figure 15 Figure 16
	Thigh1		62.5	—	31.2	—	31.2	—	ns		
	Tlow1		62.5	—	31.2	—	31.2	—	ns		
	Trise1		—	3	—	3	—	3	ns		
	Tfall1		—	3	—	3	—	3	ns		
TDMFP	Tsu2	TDMCLKP rising or falling	4	—	4	—	4	—	ns		
	Thld2		1	—	1	—	1	—	ns		
	Tdo2		2	9	2	9	2	9	ns		
TDMDIP	Tsu3	TDMCLKP rising or falling	4	—	4	—	4	—	ns		
	Thld3		1	—	1	—	1	—	ns		
TDMDOP	Tdo4	TDMCLKP rising or falling	2	9	2	9	2	9	ns		
	Tdz4		—	12	—	12	—	12	ns		
	Tzd4		3	—	3	—	3	—	ns		
TDMTEN	Tdo5	TDMCLKP rising or falling	2	9	2	9	2	9	ns		

[1]The rising or falling edge of TDMCLKP is used as the reference clock edge for the timing depending on the TDM bus mode and protocol selection.

Table 10 TDM AC Timing Characteristics

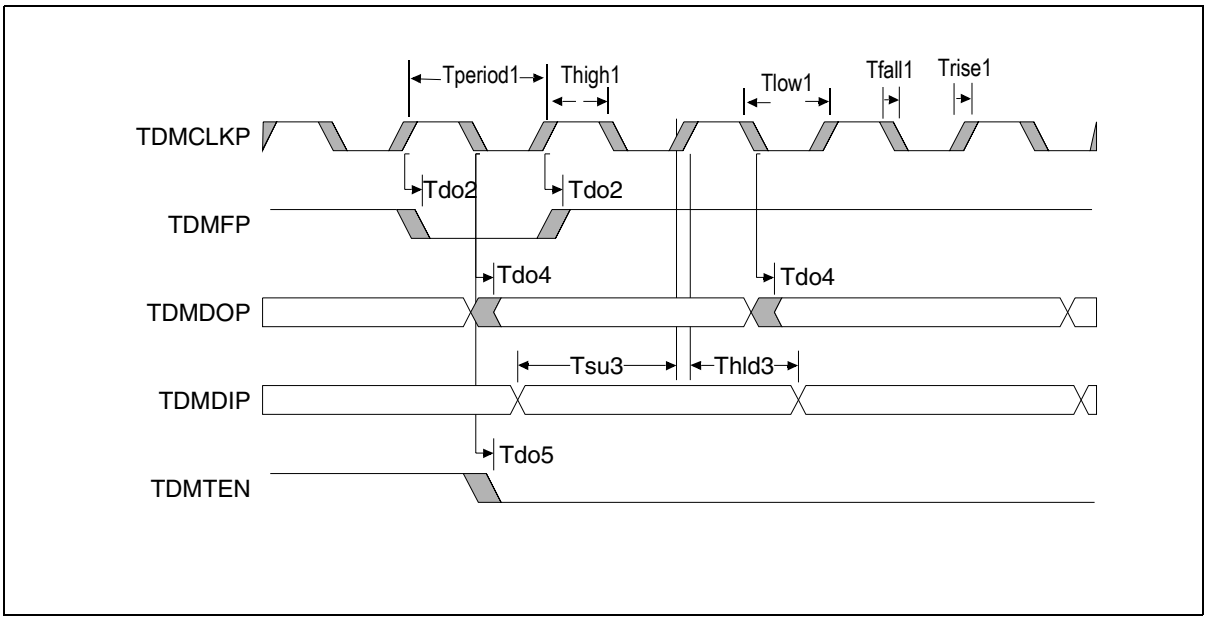


Figure 15 TDM AC Timing Waveform, Master Mode

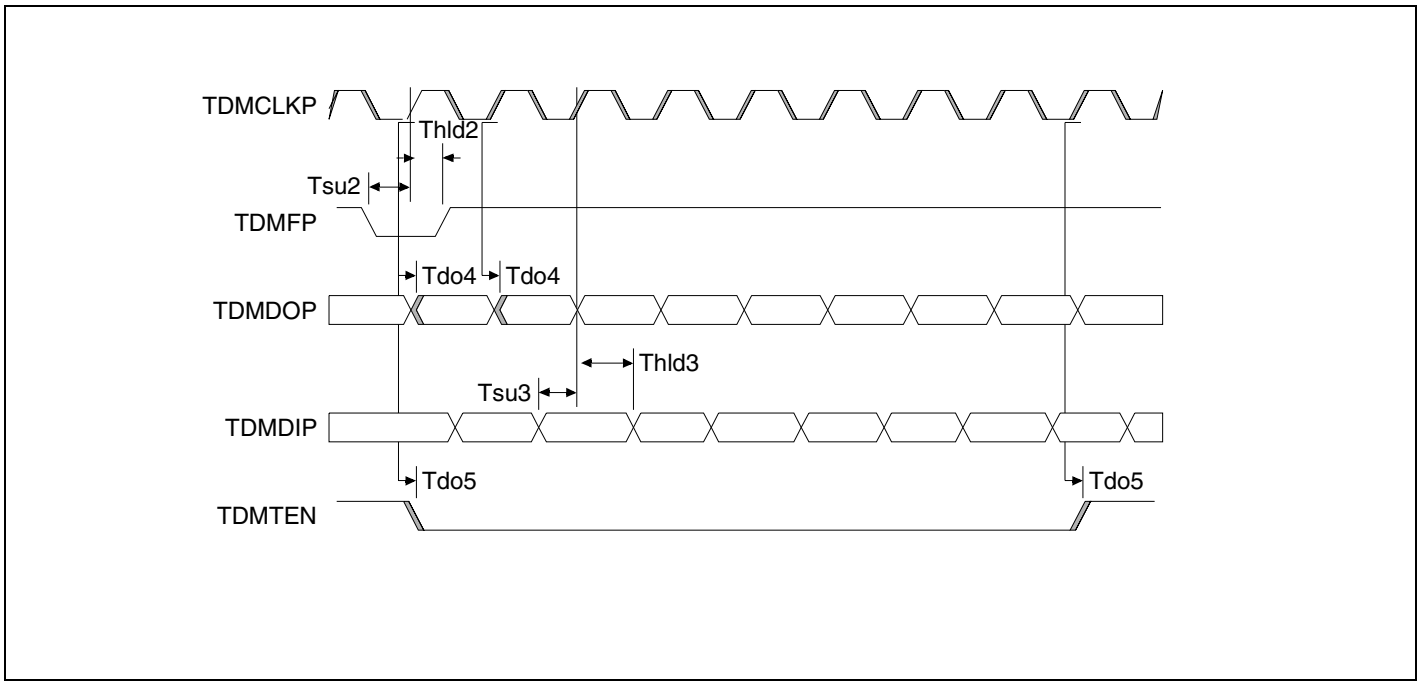


Figure 16 TDM AC Timing Waveform, Slave Mode

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
USB											
USBCLKP[1]	Tperiod1	none	19.79	21.87	19.79	21.87	19.79	21.87	ns		Figure 17
	Thigh1,Tlow1		8.3	—	8.3	—	8.3	—	ns		
	Trise1,Tfall1		—	3	—	3	—	3	ns		
	Tjitter1		—	0.8	—	0.8	—	0.8	ns	1/4th of the minimum Source data jitter	
USBDN, USBDP	Trise2		4	20	4	20	4	20	ns	Universal Serial Bus Specification (USBS) Revision 1.1: Figures 7.6 and 7.7.	
	Tfall2		4	20	4	20	4	20	ns	USBS Revision 1.1: Figures 7.6 and 7.7.	
USBDN and USBDP Rise and Fall Time Matching			90	111.11	90	111.11	90	111.11	%	USBS Revision 1.1: Note 10, Section 7.1.2.	
Data valid period	Tstate		60	—	60	—	60	—	ns		
Skew between USBDN and USBDP			—	0.4	—	0.4	—	0.4	ns	USBS Revision 1.1: Section 7.1.3	
Source data jitter			—	3.5	—	3.5	—	3.5	ns	USBS Revision 1.1: Table 7-6	
Receive data jitter			—	12	—	12	—	12	ns		
Source EOP length	Tseop		160	175	160	175	160	175	ns		
Receive EOP length	Treop		82	—	82	—	82	—	ns		
EOP jitter			-2	5	-2	5	-2	5	ns		
Full-speed Data Rate	Tfdrate		11.97	12.03	11.97	12.03	11.97	12.03	MHz	Average bit rate, USBS Section 7.1.11.	
Frame Interval			0.9995	1.0005	0.9995	1.0005	0.9995	1.0005	ms	USBS Section 7.1.12.	
Consecutive Frame Interval Jitter			—	42	—	42	—	42	ns	Without frame adjustment.	
			—	126	—	126	—	126	ns	With frame adjustment.	

[1] USB clock (USBCLKP) frequency must be less than CLKP frequency.

Table 11 USB AC Timing Characteristics

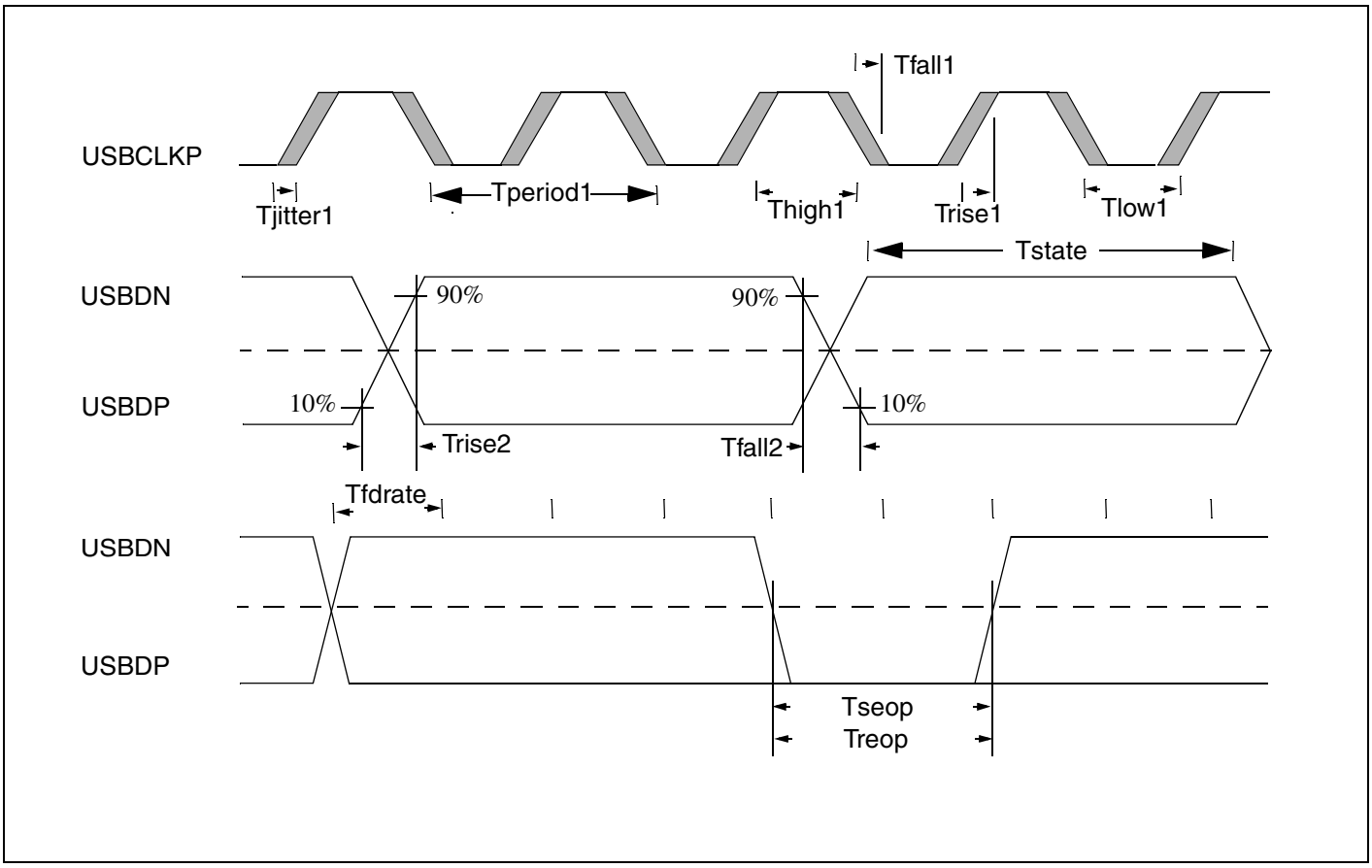


Figure 17 USB AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
UART											
U0SINP, U0RIN, U0DCDN, U0DSRN, U0CTSN, U1SINP, U1DSRN, U1CTSN	Tsu[1]	CLKP rising	5	—	5	—	5	—	ns		
	Thld[1]		3	—	3	—	3	—	ns		
U0SOUTP, U0DTRN, U0RTSN, U1SOUTP, U1DTRN, U1RTSN	Tdo[1]	CLKP rising	1	12	1	12	1	12	ns		
[1] These are asynchronous signals and the values are provided for ATE (test) only.											

Table 12 UART AC Timing Characteristics

Power-on RampUp

The 2.5V core supply (and 2.5V V_{cc}PLL supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

DC Electrical Characteristics

($T_{ambient}$ = 0°C to +70°C Commercial, $T_{ambient}$ = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%, V_{cc} Core and V_{cc} P = +2.5V±5%)

	Para-meter	Min	Max	Unit	Pin Numbers	Conditions
LOW Drive Output with Schmitt Trigger Input (STI)	I_{OL}	7.3	—	mA	1-4,6-8,10-16,18,20-25,27-29,32,33,35-37, 39-42,44,46-48,50,52,53,56,58-60,62-69, 71-77,82-85,87-94,96-99,101-105,167, 205-208	V_{OL} = 0.4V
	I_{OH}	-8.0	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
HIGH Drive Output with Standard Input	I_{OL}	9.4	—	mA	49,51,54,55,106-108,110,112-117,119, 121,123-128,130,132-137,139,141,143, 150,152,154-159,161,163-166,168-170, 172,174-179,181,185-190,192,194-200, 202,204	V_{OL} = 0.4V
	I_{OH}	-15	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
Clock Drive Output	I_{OL}	39	—	mA	183	V_{OL} = 0.4V
	I_{OH}	-24	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
Capacitance	C_{IN}	—	10	pF	All pins	—
Leakage	I/O_{LEAK}	—	20	µA	All pins	—

Table 18 DC Electrical Characteristics

Package Pin-out — 208-Pin PQFP

The following table lists the pin numbers and signal names for the RC32355.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	ATMOUTP[0]		53	JTAG_TDO		105	BGN		157	MDATA[28]	
2	ATMOUTP[1]		54	GPIOP[16]	1	106	CSN[0]		158	MDATA[13]	
3	ATMINP[02]		55	GPIOP[17]	1	107	CSN[1]		159	MDATA[29]	
4	ATMOUTP[2]		56	GPIOP[18]	1	108	CSN[2]		160	Vcc I/O	
5	Vss		57	Vss		109	Vcc I/O		161	MDATA[14]	
6	ATMOUTP[3]		58	JTAG_TCK		110	CSN[3]		162	Vss	
7	ATMINP[03]		59	GPIOP[19]	1	111	Vss		163	MDATA[30]	
8	ATMOUTP[4]		60	GPIOP[20]	1	112	OEN		164	MDATA[15]	
9	Vcc I/O		61	Vcc I/O		113	RWN		165	MDATA[31]	
10	ATMOUTP[5]		62	GPIOP[21]	1	114	BDIRN		166	CLKP	
11	ATMINP[04]		63	JTAG_TDI		115	BOEN[0]		167	WAITACKN	
12	ATMOUTP[6]		64	GPIOP[22]	1	116	BOEN[1]		168	MADDR[00]	
13	ATMOUTP[7]		65	GPIOP[23]	2	117	BWEN[0]		169	MADDR[11]	
14	ATMINP[05]		66	GPIOP[24]	1	118	Vcc I/O		170	MADDR[01]	
15	ATMOUTP[8]		67	JTAG_TMS		119	BWEN[1]		171	Vcc I/O	
16	ATMOUTP[9]		68	GPIOP[25]	2	120	Vss		172	MADDR[12]	
17	Vss		69	GPIOP[26]	1	121	BWEN[2]		173	Vss	
18	ATMINP[06]		70	Vss		122	Vcc Core		174	MADDR[02]	
19	Vcc Core		71	GPIOP[27]	1	123	BWEN[3]		175	MADDR[13]	
20	GPIOP[00]	1	72	COLDRSTN		124	MDATA[00]		176	MADDR[03]	
21	GPIOP[01]	1	73	GPIOP[28]	1	125	MDATA[16]		177	MADDR[14]	
22	ATMINP[07]		74	GPIOP[29]	1	126	MDATA[01]		178	MADDR[04]	
23	GPIOP[02]	2	75	GPIOP[30]	1	127	MDATA[17]		179	MADDR[15]	
24	GPIOP[03]	1	76	GPIOP[31]	2	128	MDATA[02]		180	Vcc I/O	
25	ATMINP[08]		77	USBCLKP		129	Vcc I/O		181	MADDR[05]	
26	Vcc I/O		78	Vcc I/O		130	MDATA[18]		182	Vcc Core	
27	GPIOP[04]	2	79	USBDN		131	Vss		183	SYSCLKP	
28	GPIOP[05]	1	80	USBDP		132	MDATA[03]		184	Vss	
29	ATMINP[09]		81	Vss		133	MDATA[19]		185	MADDR[16]	
30	VccP[1]		82	MIICRSP		134	MDATA[04]		186	MADDR[06]	
31	VssP[1]		83	MIICOLP		135	MDATA[20]		187	MADDR[17]	
32	ATMINP[10]		84	MIITXDP[0]		136	MDATA[05]		188	MADDR[07]	
33	GPIOP[06]	1	85	MIITXDP[1]		137	MDATA[21]		189	MADDR[18]	
34	Vss		86	Vcc Core		138	Vcc Core		190	MADDR[08]	

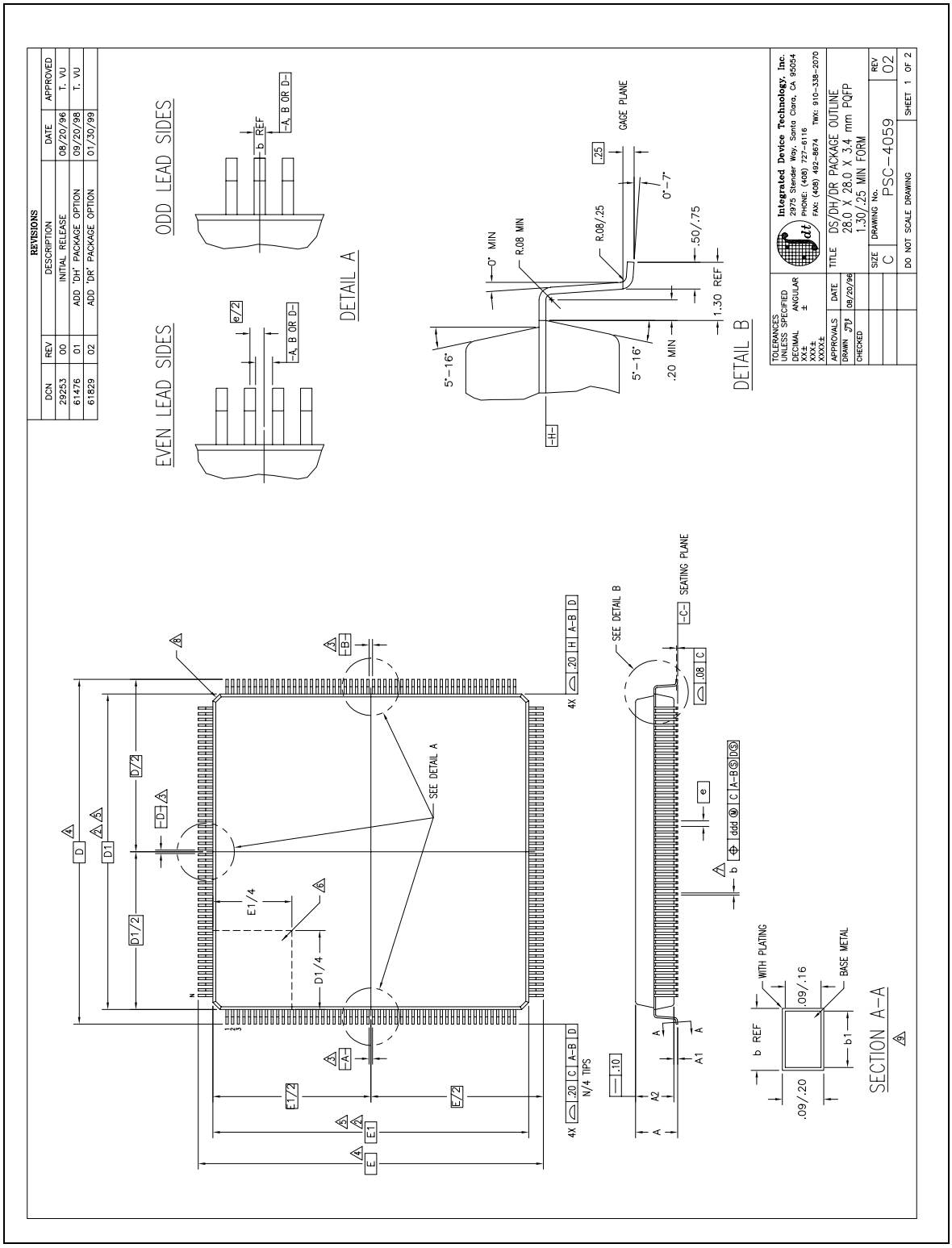
Table 22: 208-pin QFP Package Pin-Out (Part 1 of 2)

Alternate Pin Functions

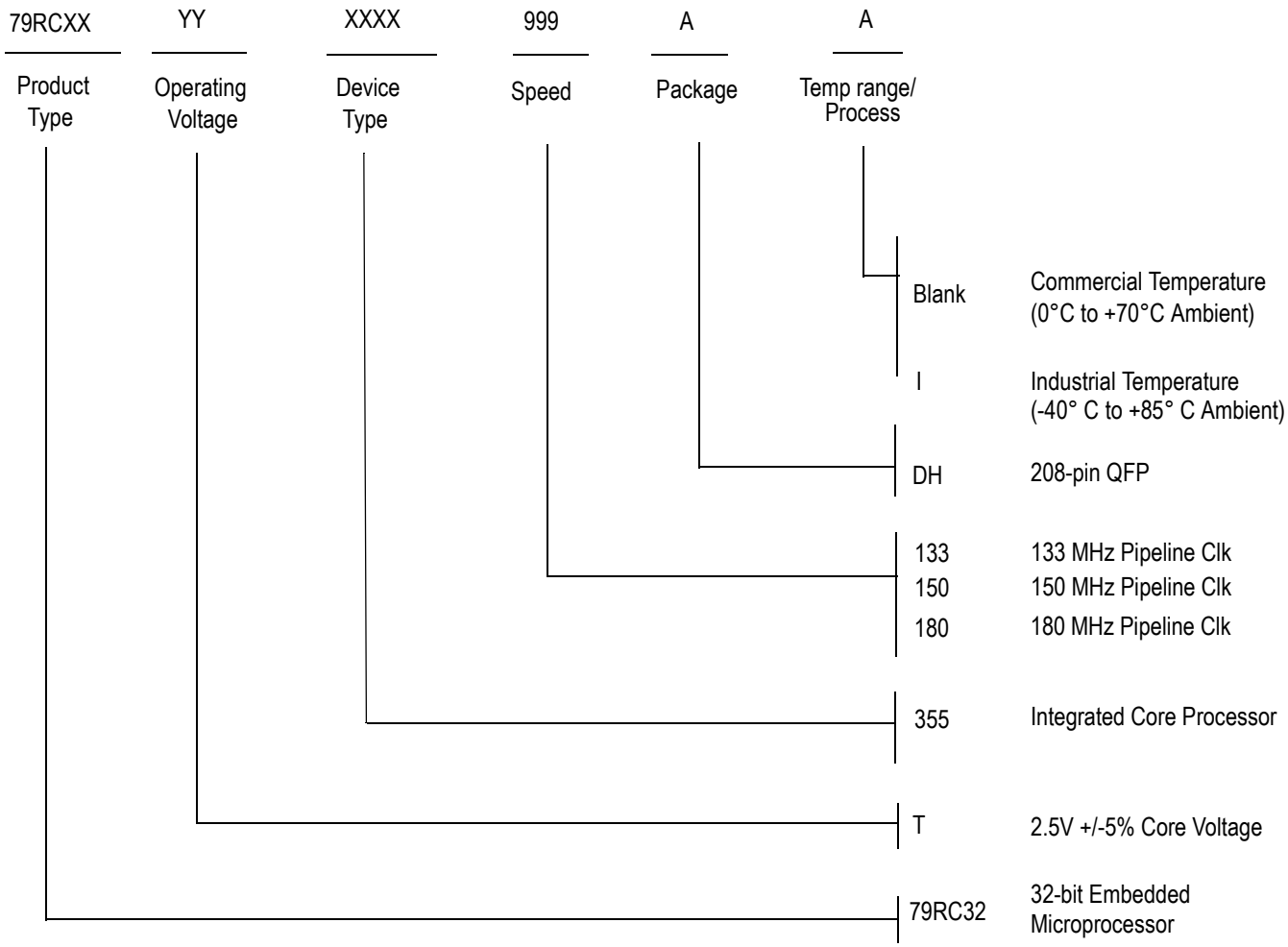
Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		51	GPIOP[32]	TDMDOP	
21	GPIOP[01]	U0SINP		54	GPIOP[16]	CSN[4]	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	55	GPIOP[17]	CSN[5]	
24	GPIOP[03]	U0DCRN		56	GPIOP[18]	DMAREQN	
27	GPIOP[04]	U0DTRN	CPUP	59	GPIOP[19]	DMADONEN	
28	GPIOP[05]	U0DSRN		60	GPIOP[20]	USBSOF	
33	GPIOP[06]	U0RTSN		62	GPIOP[21]	CKENP	
35	GPIOP[07]	U0CTSN		64	GPIOP[22]	TXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	65	GPIOP[23]	TXADDR[1]	DMAP[0]
39	GPIOP[09]	U1SINP	DMAP[2]	66	GPIOP[24]	RXADDR[0]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	69	GPIOP[26]	TDMTEN	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	71	GPIOP[27]	MADDR[22]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	73	GPIOP[28]	MADDR[23]	
46	GPIOP[14]	SDAP		74	GPIOP[29]	MADDR[24]	
47	GPIOP[15]	SCLP		75	GPIOP[30]	MADDR[25]	
48	GPIOP[35]	TDMCLKP		76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
49	GPIOP[34]	TDMFP					
50	GPIOP[33]	TDMDIP					

Table 23 Alternate Pin Functions

Package Drawing - 208-pin QFP



Ordering Information



Valid Combinations

79RC32T355 -133DH, 150DH, 180DH	208-pin QFP package, Commercial Temperature
79RC32T355 -133DHI, 150DHI	208-pin QFP package, Industrial Temperature

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