Renesas Electronics America Inc - IDT79RC32T355-180DH Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	180MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t355-180dh

- **USB**
  - *Revision 1.1 compliant*
  - *USB slave device controller*
  - *Supports a 6th USB endpoint*
  - *Full speed operation at 12 Mb/s*
  - *Supports control, interrupt, bulk and isochronous endpoints*
  - *Supports USB remote wakeup*
  - *Integrated USB transceiver*
- **TDM**
  - *Serial Time Division Multiplexed (TDM) voice and data interface*
  - *Provides interface to telephone CODECs and DSPs*
  - *Interface to high quality audio A/Ds and D/As with external glue logic*
  - *Support 1 to 128 8-bit time slots*
  - *Compatible with Lucent CHI, GCI, Mitel ST-bus, K2 and SLD busses*
  - *Supports data rates of up to 8.192 Mb/s*
  - *Supports internal or external frame generation*
  - *Supports multiple non-contiguous active input and output time slots*
- **EJTAG**
  - *Run-time Mode provides a standard JTAG interface*
  - *Real-Time Mode provides additional pins for real-time trace information*
- **Ethernet**
  - *Full duplex support for 10 and 100 Mb/s Ethernet*
  - *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
  - *IEEE 802.3u auto-negotiation for automatic speed selection*
  - *Flexible address filtering modes*
  - *64-entry hash table based multicast address filtering*
- **ATM SAR**
  - *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
  - *Supports 25Mb/s and faster ATM*
  - *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
  - *Supports standard 53-byte ATM cells*
  - *Performs HEC generation and checking*
  - *Cell processing discards short cells and clips long cells*
  - *16 cells worth of buffering*
  - *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
  - *Hardware support for CRC-32 generation and checking for AAL5*
  - *Hardware support for CRC-10 generation and checking*
  - *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
  - *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*
- **System Features**
  - *JTAG Interface (IEEE Std. 1149.1 compatible)*
  - *208 pin PQFP package*
  - *2.5V core supply and 3.3V I/O supply*
  - *Up to 180 MHz pipeline frequency and up to 75 MHz bus frequency*

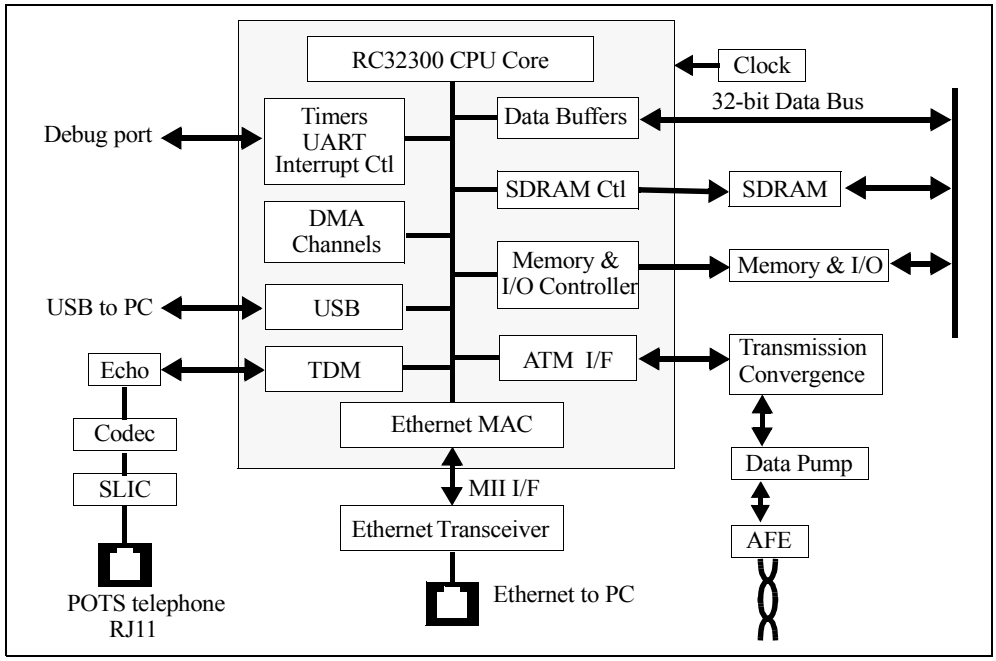


Figure 2 Example of xDSL Residential Gateway Using RC32355

Pin Description Table

The following table lists the functions of the pins provided on the RC32355. Some of the functions listed may be multiplexed onto the same pin.

To define the active polarity of a signal, a suffix will be used. Signals ending with an "N" should be interpreted as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level.

Note: The input pads of the RC32355 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as BRN) which, if left floating, could adversely affect the RC32355's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Name	Type	I/O Type	Description
System			
CLKP	I	Input	**System Clock input.** This is the system master clock input. The RISCore 32300 pipeline frequency is a multiple (x2, x3, or x4) of this clock frequency. All other logic runs at this frequency or less.
COLDRSTN	I	STI[1]	**Cold Reset.** The assertion of this signal low initiates a cold reset. This causes the RC32355 state to be initialized, boot configuration to be loaded, and the internal processor PLL to lock onto the system clock (CLKP).
RSTN	I/O	Low Drive with STI	**Reset.** This bidirectional signal is either driven low or tri-stated, an external pull-up is required to supply the high state. The RC32355 drives RSTN low during a reset (to inform the external system that a reset is taking place) and then tri-states it. The external system can drive RSTN low to initiate a warm reset, and then should tri-state it.
SYSCLKP	O	High Drive	**System clock output.** This is a buffered and delayed version of the system clock input (CLKP). All SDRAM transactions are synchronous to this clock. This pin should be externally connected to the SDRAMs and to the RC32355 SDCLKINP pin (SDRAM clock input).
Memory and Peripheral Bus			
MADDR[25:0]	O	[21:0] High Drive [25:22] Low Drive with STI	**Memory Address Bus.** 26-bit address bus for memory and peripheral accesses. MADDR[20:17] are used for the SODIMM data mask enables if SODIMM mode is selected. MADDR[22] Primary function: General Purpose I/O, GPIOP[27]. MADDR[23] Primary function: General Purpose I/O, GPIOP[28]. MADDR[24] Primary function: General Purpose I/O, GPIOP[29]. MADDR[25] Primary function: General Purpose I/O, GPIOP[30].
MDATA[31:0]	I/O	High Drive	**Memory Data Bus.** 32-bit data bus for memory and peripheral accesses.
BDIRN	O	High Drive	**External Buffer Direction.** External transceiver direction control for the memory and peripheral data bus, MDATA[31:0]. It is asserted low during any read transaction, and remains high during write transactions.
BOEN[1:0]	O	High Drive	**External Buffer Output Enable.** These signals provide two output enable controls for external data bus transceivers on the memory and peripheral data bus, MDATA. BOEN[0] is asserted low during external device read transactions. BOEN[1] is asserted low during SDRAM read transactions.
BRN	I	STI	**External Bus Request.** This signal is asserted low by an external master device to request ownership of the memory and peripheral bus.
BGN	O	Low Drive	**External Bus Grant.** This signal is asserted low by RC32355 to indicate that RC32355 has relinquished ownership of the local memory and peripheral bus to an external master.
WAITACKN	I	STI	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted low during a memory and peripheral device bus transaction to extend the bus cycle. When configured as transfer acknowledge, this signal is asserted low during a memory and peripheral device bus transaction to signal the completion of the transaction.
CSN[5:0]	O	[3:0] High Drive [5:4] Low Drive	**Device Chip Select.** These signals are used to select an external device on the memory and peripheral bus during device transactions. Each bit is asserted low during an access to the selected external device. CSN[4] Primary function: General purpose I/O, GPIOP[16]. CSN[5] Primary function: General purpose I/O, GPIOP[17].

Table 1 Pin Descriptions (Part 1 of 8)

Name	Type	I/O Type	Description
TDMTEN	O	Low Drive	**TDM External Buffer Enable.** This signal controls an external tri-state buffer output enable connected to the TDM output data, TDMDOP. It is asserted low when the RC32355 is driving data on TDMDOP. Primary function: General Purpose I/O, GPIOP[26]
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
GPIOP[5]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data set ready, U0DSRN.
GPIOP[6]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 request to send, U0RTSN.
GPIOP[7]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 clear to send, U0CTSN.
GPIOP[8]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial output, U1SOUTP. 2nd Alternate function: Active DMA channel code, DMAP[3].
GPIOP[9]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial input, U1SINP. 2nd Alternate function: Active DMA channel code, DMAP[2].
GPIOP[10]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[0].
GPIOP[11]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data set ready, U1DSRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[1].
GPIOP[12]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 request to send, U1RTSN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[2].
GPIOP[13]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 clear to send, U1CTSN. 2nd Alternate function: ICE PC trace clock, EJTAG_DCLK.
GPIOP[14]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface data, SDAP.
GPIOP[15]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: I^2C interface clock, SCLP.
GPIOP[16]	I/O	High Drive	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[4].

Table 1 Pin Descriptions (Part 3 of 8)

Name	Type	I/O Type	Description
DMAP[2]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[9]. 1st Alternate function: U1SINP.
DMAP[3]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[8]. 1st Alternate function: U1SOUTP.
UART			
U0SOUTP	I	STI	**UART channel 0 serial transmit.** Primary function: General Purpose I/O, GPIOP[0]. At reset, this pin defaults to primary function GPIOP[0].
U0SINP	I	STI	**UART channel 0 serial receive.** Primary function: General Purpose I/O, GPIOP[1]. At reset, this pin defaults to primary function GPIOP[1].
U0RIN	I	STI	**UART channel 0 ring indicator.** Primary function: General Purpose I/O, GPIOP[2]. At reset, this pin defaults to primary function GPIOP[2] if JTAG reset enable is not selected during reset using the boot configuration. 2nd Alternate function: JTAG boundary scan reset, JTAG_TRST_N.
U0DCRN	I	STI	**UART channel 0 data carrier detect.** Primary function: General Purpose I/O, GPIOP[3]. At reset, this pin defaults to primary function GPIOP[3].
U0DTRN	O	Low Drive	**UART channel 0 data terminal ready.** Primary function: General Purpose I/O, GPIOP[4]. At reset, this pin defaults to primary function GPIOP[4] if CPU/DMA Status Mode enable is not selected during reset using the boot configuration. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
U0DSRN	I	STI	**UART channel 0 data set ready.** Primary function: General Purpose I/O, GPIOP[5]. At reset, this pin defaults to primary function GPIOP[5].
U0RTSN	O	Low Drive	**UART channel 0 request to send.** Primary function: General Purpose I/O, GPIOP[6]. At reset, this pin defaults to primary function GPIOP[6].
U0CTSN	I	STI	**UART channel 0 clear to send.** Primary function: General Purpose I/O, GPIOP[7]. At reset, this pin defaults to primary function GPIOP[7].
U0SOUTP	O	Low Drive	**UART channel 1 serial transmit.** Primary function: General Purpose I/O, GPIOP[8]. At reset, this pin defaults to primary function GPIOP[8] if DMA Debug enable is not selected during reset using the boot configuration. 2nd Alternate function: DMA channel, DMAP[3].
U1SINP	I	STI	**UART channel 1 serial receive.** Primary function: General Purpose I/O, GPIOP[9]. At reset, this pin defaults to primary function GPIOP[9] if DMA Debug enable is not selected during reset using the boot configuration. 2nd Alternate function: DMA channel, DMAP[2].
U1DTRN	O	Low Drive	**UART channel 1 data terminal ready.** Primary function: General Purpose I/O, GPIOP[10]. At reset, this pin defaults to primary function GPIOP[10] if ICE Interface enable is not selected during reset using the boot configuration. Alternate function: PC trace status bit 0, EJTAG_PCST[0].
U1DSRN	I	STI	**UART channel 1 data set ready.** Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace status bit 1, EJTAG_PCST[1].
U1RTSN	O	Low Drive	**UART channel 1 request to send.** Primary function: General Purpose I/O, GPIOP[12]. At reset, this pin defaults to primary function GPIOP[12] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace status bit 2, EJTAG_PCST[2].

Table 1 Pin Descriptions (Part 7 of 8)

Name	Type	I/O Type	Description
U1CTSN	I	STI	**UART channel 1 clear to send.** Primary function: General Purpose I/O, GPIOP[13]. At reset, this pin defaults to primary function GPIOP[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 8 of 8)

1. Schmitt Trigger Input.
2. 2I^2C - Bus Specification by Philips Semiconductors.

Boot Configuration Vector

The boot configuration vector is read into the RC32355 during cold reset. The vector defines parameters in the RC32355 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Signal	Name/Description
MDATA[2:0]	**Clock Multiplier**. This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	**Endian.** This bit specifies the endianness of RC32355. 0x0 - little endian 0x1 - big endian
MDATA[4]	**Reserved.** Must be set to 0.
MDATA[5]	**Debug Boot Mode**. When this bit is set, the RC32355 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	**Boot Device Width**. This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	**EJTAG/ICE Interface Enable**. When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIOP[31, 13:10] pins behaves as GPIOP 0x1 - GPIOP[31] pin behaves as EJTAG_TRST_N, GPIOP[12:10] pins behave as EJTAG_PCST[2:0], and GPIOP[13] pin behaves as EJTAG_DCLK
MDATA[9]	**Fast Reset**. When this bit is set, RC32355 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32355 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32355 drives RSTN for 64 clock cycles (test only)
MDATA[10]	**DMA Debug Enable**. When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIOP[8, 9, 25, 23] pins behave as GPIOP 0x1 - GPIOP[8, 9, 25, 23] pins behave as DMAP[3:0]

Table 2 Boot Configuration Vector Encoding (Part 1 of 2)

Signal	Name/Description
MDATA[11]	**Hold SYSCLKP Constant**. For systems that do not require a SYSCLKP output and can instead use CLKP, setting this bit to a one causes the SYSCLKP output to be held at a constant level. This may be used to reduce EMI. 0x0 - Allow SYSCLKP to toggle 0x1 - Hold SYSCLKP constant
MDATA[12]	**JTAG Boundary Scan Reset Enable**. When this bit is set, Alternate 2 pin function, JTAG_TRST_N is selected. 0x0 - GPIOP[2] pin behaves as GPIOP 0x1 - GPIOP[2] pin behaves as JTAG_TRST_N
MDATA[13]	**CPU / DMA Transaction Indicator Enable**. When this bit is set, Alternate 2 pin function, CPUP is selected. 0x0 - GPIOP[4] pin behaves as GPIOP 0x1 - GPIOP[4] pin behaves as CPUP
MDATA[15:14]	**Reserved**. These pins must be driven low during boot configuration.

Table 2 Boot Configuration Vector Encoding (Part 2 of 2)

Clock Parameters

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%, V_{cc} Core and V_{cc}P = +2.5V±5%)

Parameter	Symbol	Reference Edge	133MHz		150MHz		180MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Internal CPU pipeline clock[1]	Frequency	none	100	133	100	150	100	180	MHz	Figure 4
CLKP[2,3,4]	Frequency	none	25	67	25	75	25	90	MHz	
	Tperiod1		15	40	13.3	40	11.1	40	ns	
	Thigh1		6	—	5.4	—	5.4	—	ns	
	Tlow1		6	—	5.4	—	5.4	—	ns	
	Trise1		—	3	—	2.5	—	2.5	ns	
	Tfall1		—	3	—	2.5	—	2.5	ns	
	Tjitter		—	±250	—	±200	—	±200	ps	

[1] The CPU pipeline clock speed is selected during cold reset by the boot configuration vector (see Table 2).
[2] Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.
[3] USB clock (USBCLKP) frequency must be less than CLKP frequency.
[4] ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

Table 3 Clock Parameters

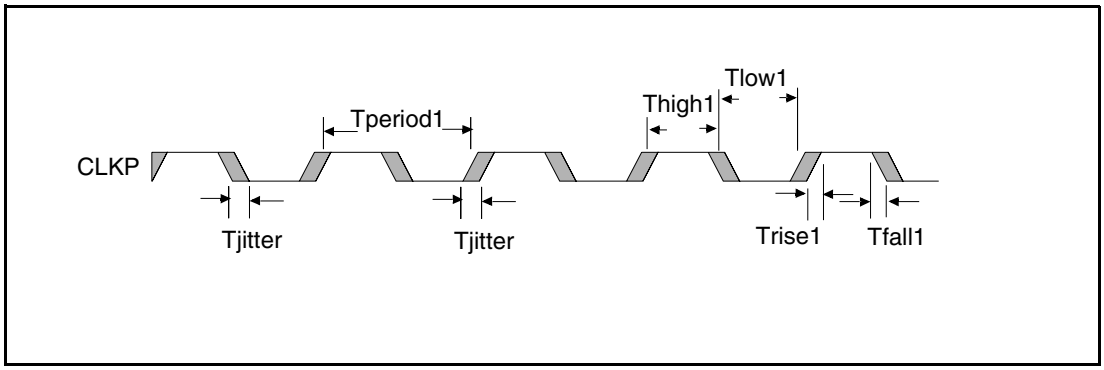


Figure 4 Clock Parameters Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus - SDRAM Access											
MDATA[31:0]	Tsu1	SDCLKINP rising	2.5	—	2.5	—	2.5	—	ns		Figure 8 Figure 9 Figure 10
	Thld1		1.5	—	1.5	—	1.5	—	ns		
	Tdo1	SYSCLKP rising	1.2	5.8	1.2	5.8	1.2	5.8	ns		
	Tdz1		—	5.0	—	5.0	—	5.0	ns		
	Tzd1		1.0	—	1.0	—	1.0	—	ns		
MADDR[20:2], BWEN[3:0]	Tdo2	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CASN, RASN, SDCSN[1:0], SDWEN	Tdo3	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
CKENP	Tdo4	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BDIRN	Tdo5	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
BOEN[1:0]	Tdo6	SYSCLKP rising	1.2	5.3	1.2	5.3	1.2	5.3	ns		
SYSCLKP rising	Tdo7	CLKP rising	0.5	5.0	0.5	5.0	0.5	5.0	ns		
SDCLKINP	Tperiod8	none	15	50	13.3	50	13.3	50	ns		
	Thigh8,Tlow8		6.0	—	5.4	—	5.4	—	ns		
	Trise8,Tfall8		—	3.0	—	2.5	—	2.5	ns		
	Tdelay8	SYSCLKP rising	0	4.8	0	4.8	0	4.8	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

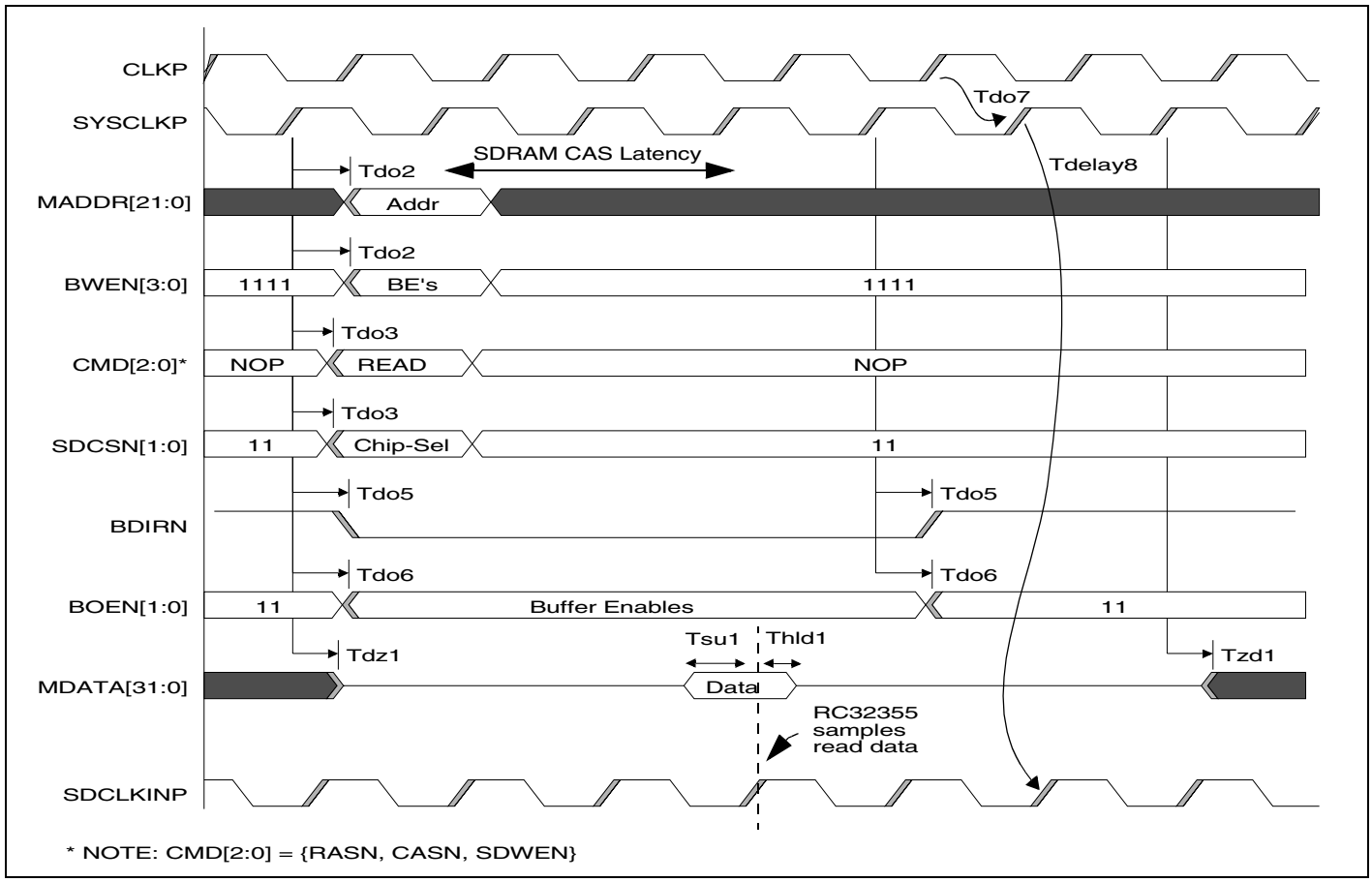


Figure 8 Memory and Peripheral Bus AC Timing Waveform - SDRAM Read Access

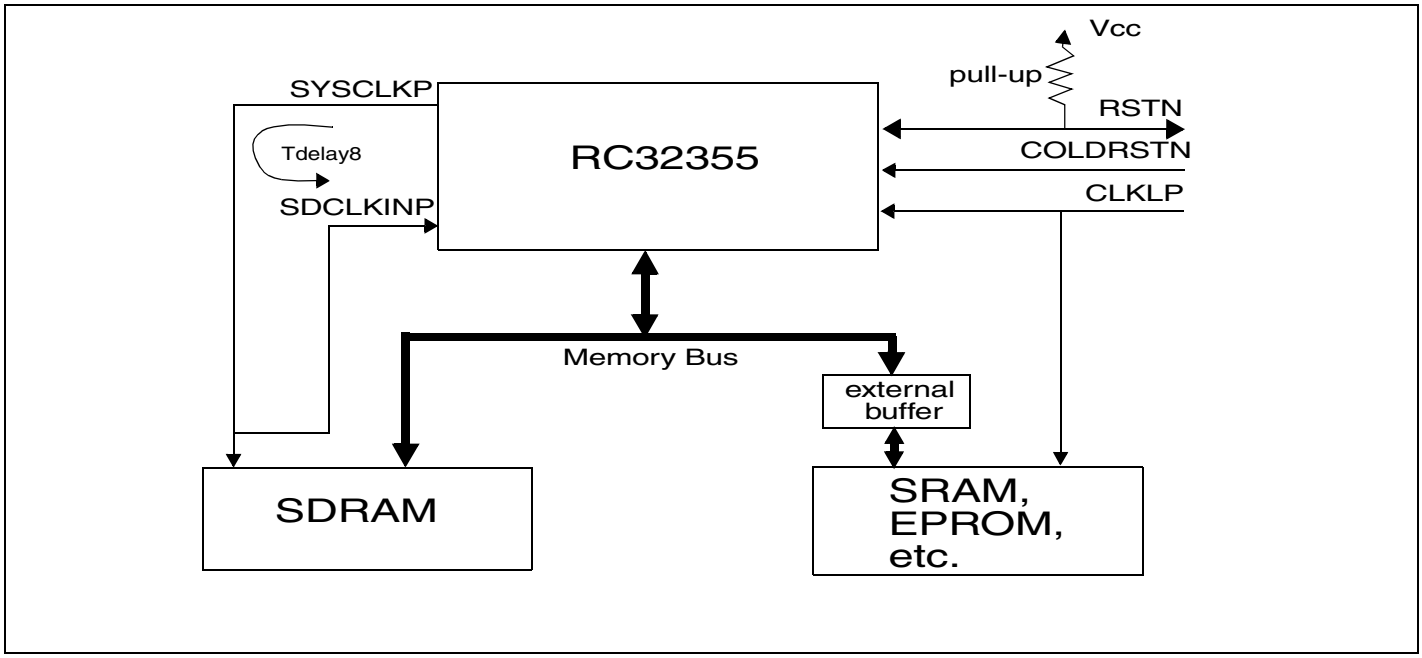


Figure 9 SYSCLKP - SDCLKINP Relationship

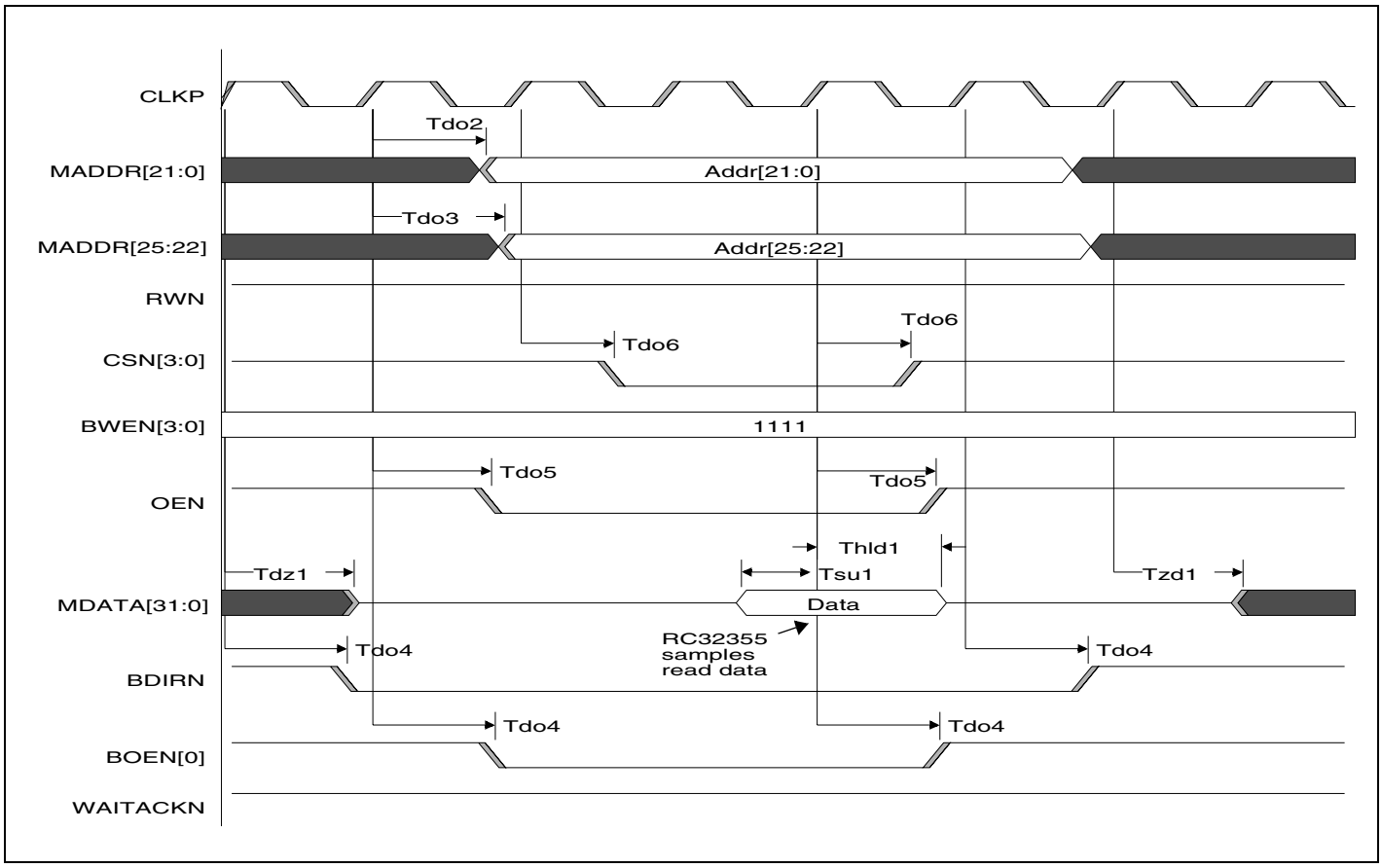


Figure 11 Memory and Peripheral Bus AC Timing Waveform - Device Read Access

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
TDM											
TDMCLKP[1]	Tperiod1	none	—	125	—	62.5	—	62.5	ns		Figure 15 Figure 16
	Thigh1		62.5	—	31.2	—	31.2	—	ns		
	Tlow1		62.5	—	31.2	—	31.2	—	ns		
	Trise1		—	3	—	3	—	3	ns		
	Tfall1		—	3	—	3	—	3	ns		
TDMFP	Tsu2	TDMCLKP rising or falling	4	—	4	—	4	—	ns		
	Thld2		1	—	1	—	1	—	ns		
	Tdo2		2	9	2	9	2	9	ns		
TDMDIP	Tsu3	TDMCLKP rising or falling	4	—	4	—	4	—	ns		
	Thld3		1	—	1	—	1	—	ns		
TDMDOP	Tdo4	TDMCLKP rising or falling	2	9	2	9	2	9	ns		
	Tdz4		—	12	—	12	—	12	ns		
	Tzd4		3	—	3	—	3	—	ns		
TDMTEN	Tdo5	TDMCLKP rising or falling	2	9	2	9	2	9	ns		

[1]The rising or falling edge of TDMCLKP is used as the reference clock edge for the timing depending on the TDM bus mode and protocol selection.

Table 10 TDM AC Timing Characteristics

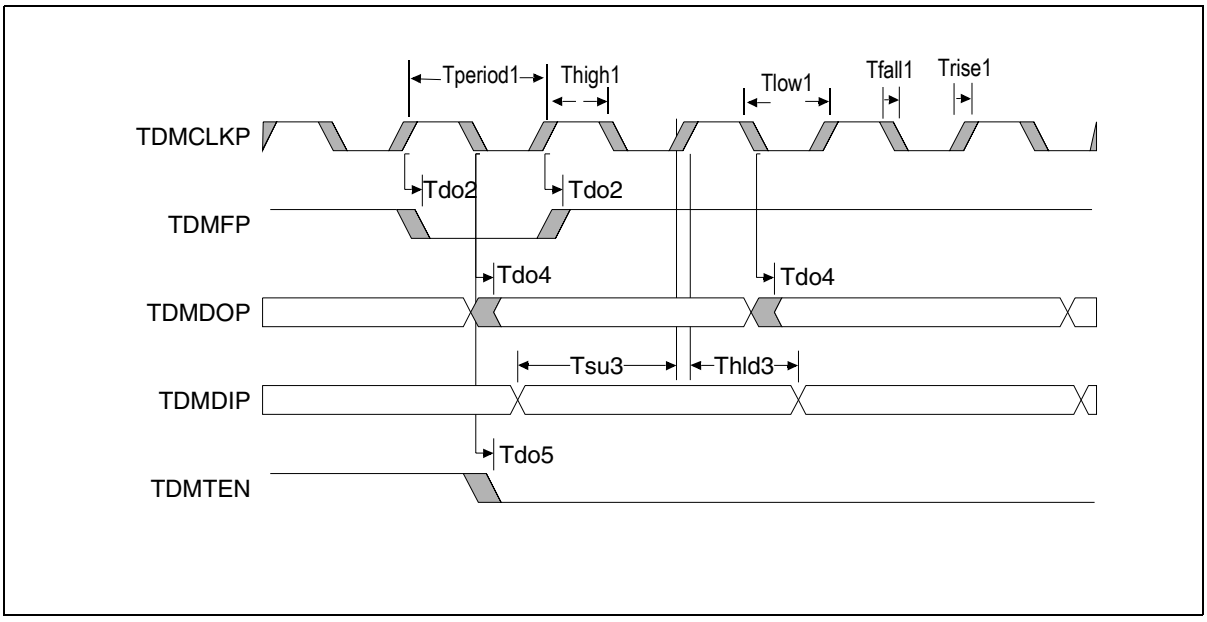


Figure 15 TDM AC Timing Waveform, Master Mode

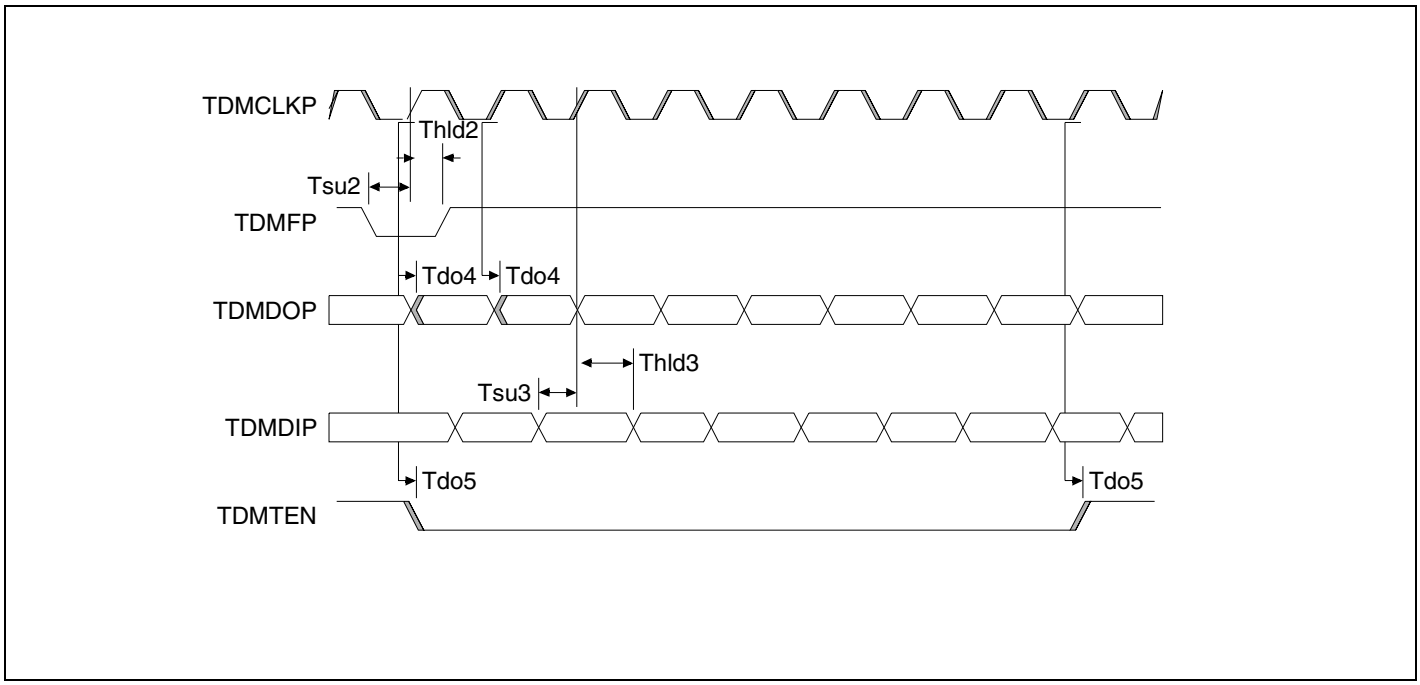


Figure 16 TDM AC Timing Waveform, Slave Mode

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
I^2C[1]											
SCLP	Frequency	none	0	100	0	100	0	100	kHz	100 KHz	Figure 18
	Thigh1		4.0	—	4.0	—	4.0	—	µs		
	Tlow1		4.7	—	4.7	—	4.7	—	µs		
	Trise1		—	1000	—	1000	—	1000	ns		
	Tfall1		—	300	—	300	—	300	ns		
SDAP	Tsu2	SCLP rising	250	—	250	—	250	—	ns		
	Thld2		0	3.45	0	3.45	0	3.45	µs		
	Trise2		—	1000	—	1000	—	1000	ns		
	Tfall2		—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu3	SDAP falling	4.7	—	4.7	—	4.7	—	µs		
	Thld3		4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu4	SDAP rising	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay5		4.7	—	4.7	—	4.7	—	µs		
SCLP	Frequency	none	0	400	0	400	0	400	kHz	400 KHz	
	Thigh1		0.6	—	0.6	—	0.6	—	µs		
	Tlow1		1.3	—	1.3	—	1.3	—	µs		
	Trise1		—	300	—	300	—	300	ns		
	Tfall1		—	300	—	300	—	300	ns		
SDAP	Tsu2	SCLP rising	100	—	100	—	100	—	ns		
	Thld2		0	0.9	0	0.9	0	0.9	µs		
	Trise2		—	300	—	300	—	300	ns		
	Tfall2		—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu3	SDAP falling	0.6	—	0.6	—	0.6	—	µs		
	Thld3		0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu4	SDAP rising	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay5		1.3	—	1.3	—	1.3	—	µs		

Table 13 I^2C AC Timing Characteristics

1. For more information see the I^2C-Bus specification by Philips Semiconductor

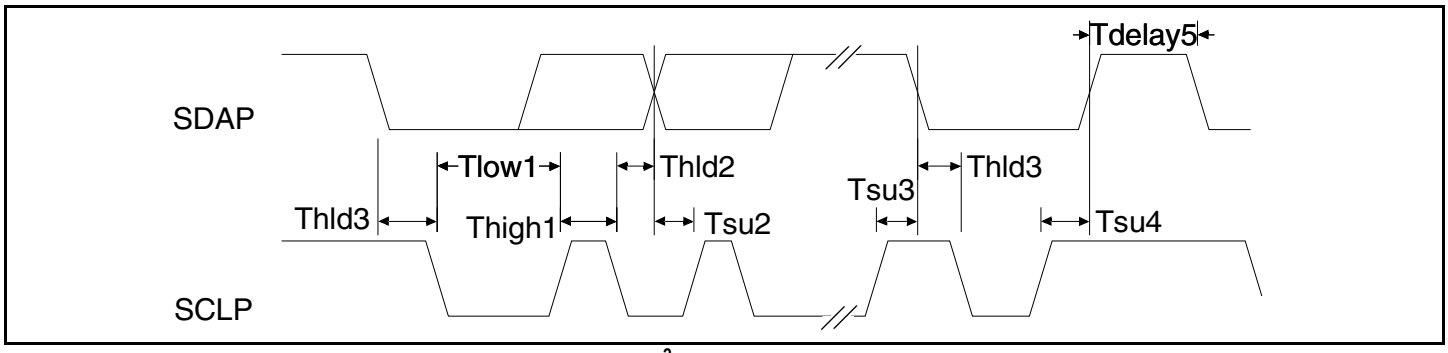


Figure 18 I^2C AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
GPIOP											
GPIOP[31:0][1]	Tsu1	CLKP rising	4	—	4	—	4	—	ns		Figure 19
	Thld1		1.4	—	1.4	—	1.4	—	ns		
	Tdo1		2	8	2	8	2	8	ns		
GPIOP[35:32][2]	Tsu1		3	—	3	—	3	—	ns		
	Thld1		1	—	1	—	1	—	ns		
	Tdo1		3	8	3	8	3	8	ns		

[1] GPIOP[31:0] are controlled through the GPIO interface. GPIO[31:0] are asynchronous signals, the values are provided for ATE (test) only.
[2] GPIOP[35:32] are controlled through the TDM interface.

Table 14 GPIOP AC Timing Characteristics

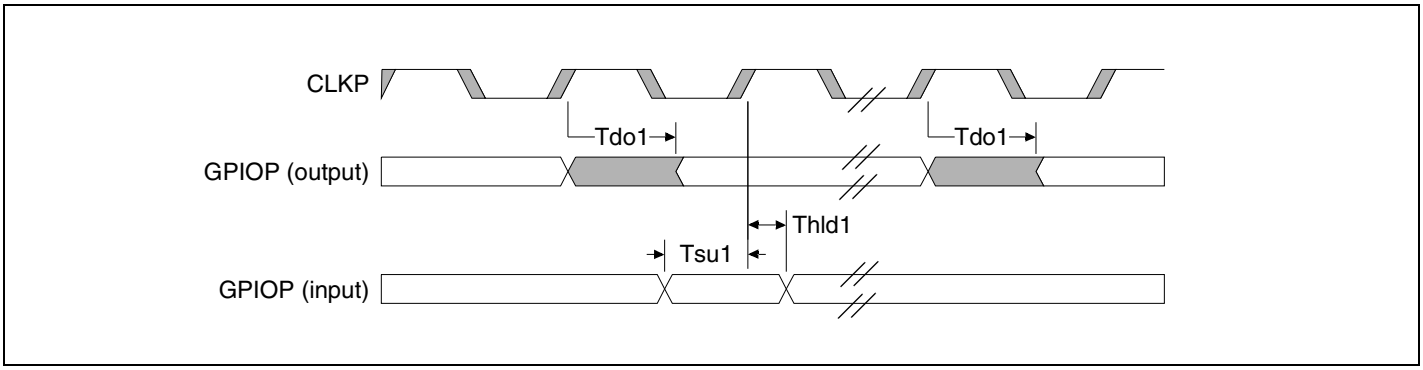


Figure 19 GPIOP AC Timing Waveform

Signal	Symbol	Reference Edge	133MHz		150MHz		180MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max			
EJTAG and JTAG											
JTAG_TCK	Tperiod1	none	100	—	100	—	100	—	ns		Figure 20
	Thigh1, Tlow1		40	—	40	—	40	—	ns		
	Trise1, Tfall1		—	5	—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	7.5	10.0	6.7	10.0	5.6	10.0	ns		
	Thigh2, Tlow2		2.5	—	2.5	—	2.5	—	ns		
	Trise2, Tfall2		—	3.5	—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2	12.0	2	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 15 JTAG AC Timing Characteristics

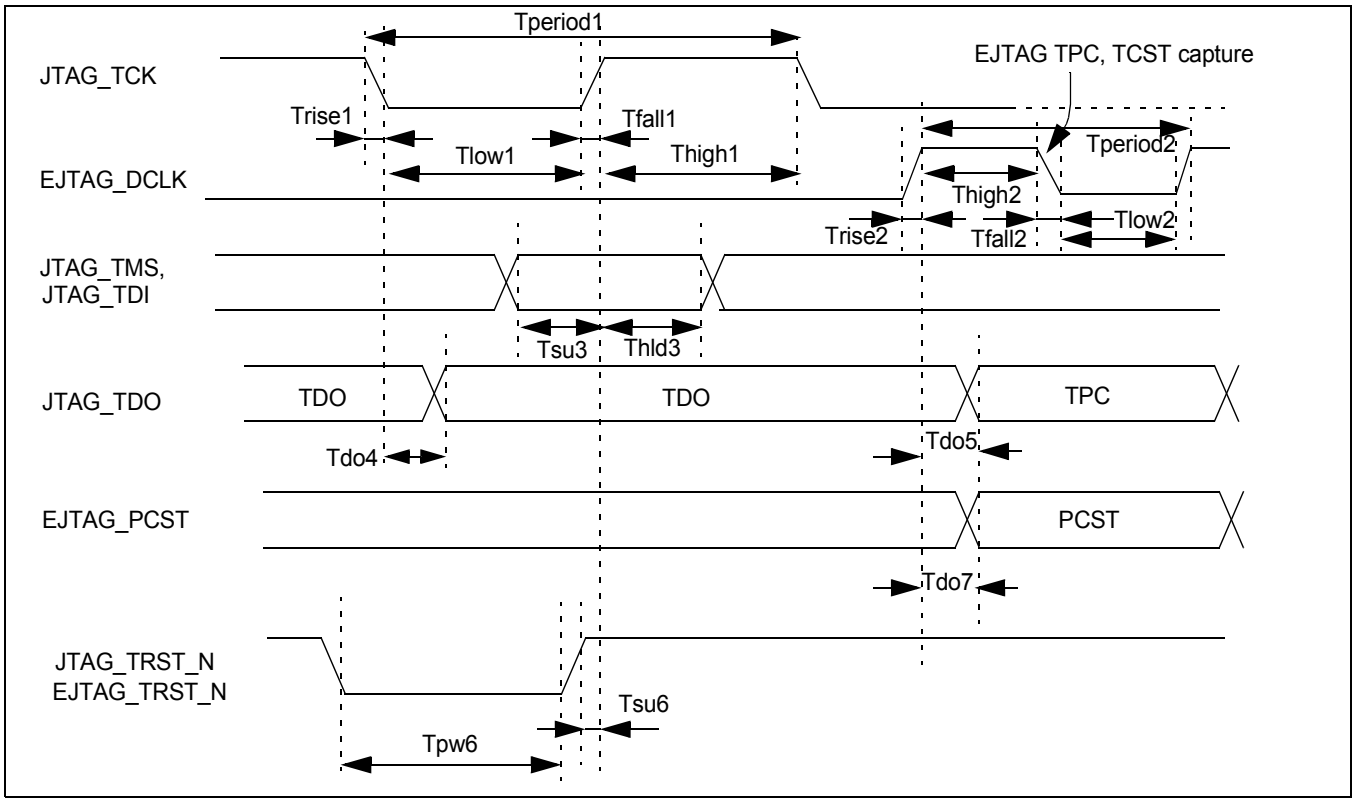


Figure 20 JTAG AC Timing Waveform

Power-on RampUp

The 2.5V core supply (and 2.5V V_{cc}PLL supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

DC Electrical Characteristics

($T_{ambient}$ = 0°C to +70°C Commercial, $T_{ambient}$ = -40°C to +85°C Industrial, Vcc I/O = +3.3V±5%, V_{cc} Core and V_{cc} P = +2.5V±5%)

	Para-meter	Min	Max	Unit	Pin Numbers	Conditions
LOW Drive Output with Schmitt Trigger Input (STI)	I_{OL}	7.3	—	mA	1-4,6-8,10-16,18,20-25,27-29,32,33,35-37, 39-42,44,46-48,50,52,53,56,58-60,62-69, 71-77,82-85,87-94,96-99,101-105,167, 205-208	V_{OL} = 0.4V
	I_{OH}	-8.0	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
HIGH Drive Output with Standard Input	I_{OL}	9.4	—	mA	49,51,54,55,106-108,110,112-117,119, 121,123-128,130,132-137,139,141,143, 150,152,154-159,161,163-166,168-170, 172,174-179,181,185-190,192,194-200, 202,204	V_{OL} = 0.4V
	I_{OH}	-15	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
Clock Drive Output	I_{OL}	39	—	mA	183	V_{OL} = 0.4V
	I_{OH}	-24	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
Capacitance	C_{IN}	—	10	pF	All pins	—
Leakage	I/O_{LEAK}	—	20	µA	All pins	—

Table 18 DC Electrical Characteristics

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
35	GPIOP[07]	1	87	MIITXDP[2]		139	MDATA[06]		191	Vcc I/O	
36	ATMINP [11]		88	MIITXDP[3]		140	Vcc I/O		192	MADDR[19]	
37	GPIOP[08]	2	89	MIITXENP		141	MDATA[22]		193	Vss	
38	Vcc Core		90	MIITXCLKP		142	Vss		194	MADDR[09]	
39	GPIOP[09]	2	91	MIITXERP		143	MDATA[07]		195	MADDR[20]	
40	GPIOP[10]	2	92	MIIRXERP		144	MDATA[23]		196	MADDR[10]	
41	GPIOP[11]	2	93	MIIRXCLKP		145	SDCLKINP		197	MADDR[21]	
42	GPIOP[12]	2	94	MIIRXDVP		146	MDATA[08]		198	CASN	
43	Vcc I/O		95	Vcc I/O		147	MDATA[24]		199	RASN	
44	GPIOP[13]	2	96	MIIRXDP[0]		148	MDATA[09]		200	SDWEN	
45	Vss		97	MIIRXDP[1]		149	MDATA[25]		201	Vcc I/O	
46	GPIOP[14]	1	98	MIIRXDP[2]		150	MDATA[10]		202	SDCSN[0]	
47	GPIOP[15]	1	99	MIIRXDP[3]		151	Vcc I/O		203	Vss	
48	GPIOP[35]	1	100	Vss		152	MDATA[26]		204	SDCSN[1]	
49	GPIOP[34]	1	101	MIIDCP		153	Vss		205	ATMINP[00]	
50	GPIOP[33]	1	102	MIIDIOP		154	MDATA[11]		206	ATMIOP[0]	
51	GPIOP[32]	1	103	RSTN		155	MDATA[27]		207	ATMIOP[1]	
52	INSTP		104	BRN		156	MDATA[12]		208	ATMINP[01]	

[1] VccP and VssP are the Phase Lock Loop (PLL) power and ground. PLL power and ground should be supplied through a special filter circuit.

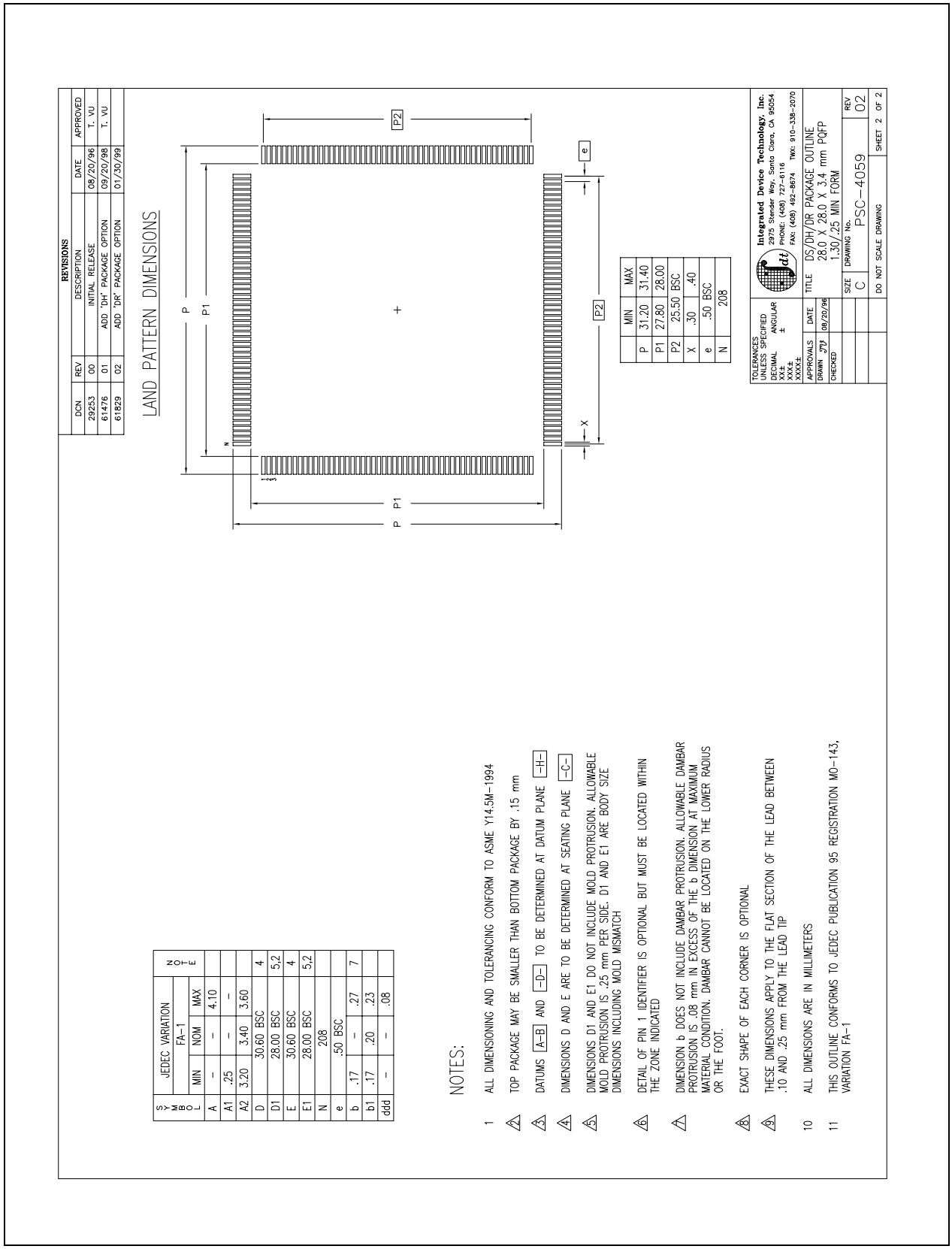
Table 22: 208-pin QFP Package Pin-Out (Part 2 of 2)

Alternate Pin Functions

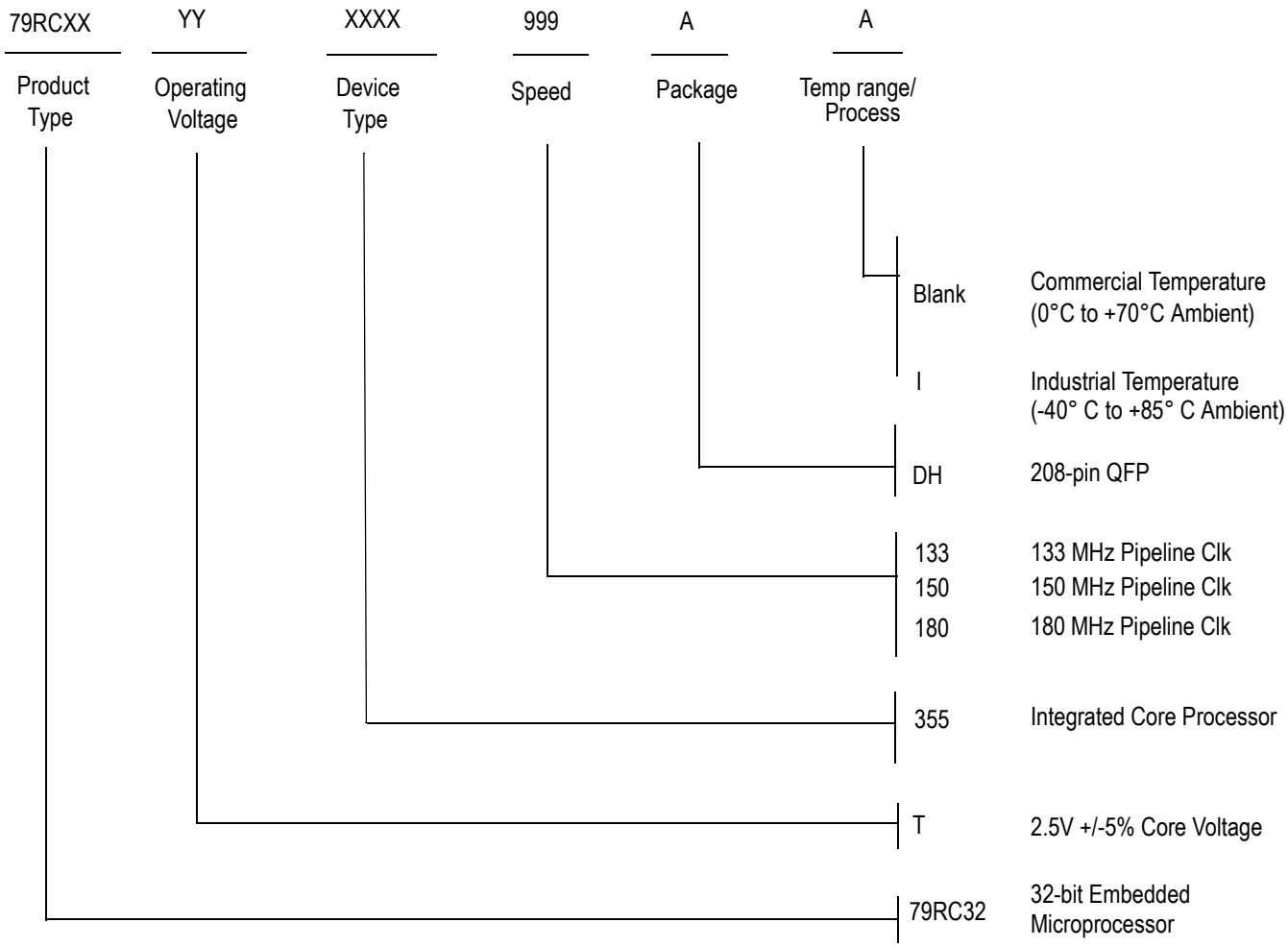
Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		51	GPIOP[32]	TDMDOP	
21	GPIOP[01]	U0SINP		54	GPIOP[16]	CSN[4]	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	55	GPIOP[17]	CSN[5]	
24	GPIOP[03]	U0DCRN		56	GPIOP[18]	DMAREQN	
27	GPIOP[04]	U0DTRN	CPUP	59	GPIOP[19]	DMADONEN	
28	GPIOP[05]	U0DSRN		60	GPIOP[20]	USBSOF	
33	GPIOP[06]	U0RTSN		62	GPIOP[21]	CKENP	
35	GPIOP[07]	U0CTSN		64	GPIOP[22]	TXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	65	GPIOP[23]	TXADDR[1]	DMAP[0]
39	GPIOP[09]	U1SINP	DMAP[2]	66	GPIOP[24]	RXADDR[0]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	69	GPIOP[26]	TDMTEN	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	71	GPIOP[27]	MADDR[22]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	73	GPIOP[28]	MADDR[23]	
46	GPIOP[14]	SDAP		74	GPIOP[29]	MADDR[24]	
47	GPIOP[15]	SCLP		75	GPIOP[30]	MADDR[25]	
48	GPIOP[35]	TDMCLKP		76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
49	GPIOP[34]	TDMFP					
50	GPIOP[33]	TDMDIP					

Table 23 Alternate Pin Functions

Package Drawing - page two



Ordering Information



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