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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	79
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 135°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5744pfk1aklq8

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[49]	0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I		
	IMCR[98]	0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I		
A[4]	MSCR[4]	0000 (Default)	GPIO[4]	SIUL2-GPIO[4]	General Purpose IO A[4]	I/O	108	D16
		0001	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0010	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0011	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0100	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[112]	0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I		
	IMCR[177]	0001	REQ4	SIUL2	SIUL2 External Interrupt Source 4	I		
	IMCR[172]	0000 (Default)	FAB	MC_RGM	RGM Force Alternate Boot Mode	I		
	IMCR[65]	0001	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I		
	IMCR[63]	0011	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
A[5]	MSCR[5]	0000 (Default)	GPIO[5]	SIUL2-GPIO[5]	General Purpose IO A[5]	I/O	14	H4
		0001	CS0	DSPI1	DSPI 1 Peripheral Chip Select 0	I/O		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[70]	0001	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[178]	0001	REQ5	SIUL2	SIUL2 External Interrupt Source 5	I		
A[6]	MSCR[6]	0000 (Default)	GPIO[6]	SIUL2-GPIO[6]	General Purpose IO A[6]	I/O	2	D1
		0001	SCK	DSPI1	DSPI 1 Input/Output Serial Clock	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[191]	0001	REQ18	SIUL2	SIUL2 External Interrupt Source 18	I		
B[7]	MSCR[23]	0000 (Default)	GPI[23][4] ADC0_AN[0]	SIUL2-GPI[23]	General Purpose Input B[7]	I	43	R5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[165]	0010	RXD	LIN0	LIN 0 Receive Pin	I		
B[8]	MSCR[24]	0	GPI[24][4] ADC0_AN[1]	SIUL2-GPI[24]	General Purpose Input B[8]	I	47	P7
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[64]	0001	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I		
B[9]	MSCR[25]	0000 (Default)	GPI[25][4] ADC0_ADC1_AN[11]	SIUL2-GPI[25]	General Purpose Input B[9]	I	52	U7
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[10]	MSCR[26]	0000 (Default)	GPI[26][4] ADC0_ADC1_AN[12]	SIUL2-GPI[26]	General Purpose Input B[10]	I	53	R8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[11]	MSCR[27]	0000 (Default)	GPI[27][4] ADC0_ADC1_AN[13]	SIUL2-GPI[27]	General Purpose Input B[11]	I	54	T8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[12]	MSCR[28]	0000 (Default)	GPI[28][4] ADC0_ADC1_AN[14]	SIUL2-GPI[28]	General Purpose Input B[12]	I	55	U8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
B[13]	MSCR[29]	0000 (Default)	GPI[29][4] ADC1_AN[0]	SIUL2-GPI[29]	General Purpose Input B[13]	I	60	R10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[166]	0001	RXD	LIN1	LIN 1 Receive Pin	I		
B[14]	MSCR[30]	0000 (Default)	GPI[30][4] ADC1_AN[1]	SIUL2-GPI[30]	General Purpose Input B[14]	I	64	P11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0001	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0011	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[62]	0001	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I		
	IMCR[92]	0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I		
E[0]	MSCR[64]	0000 (Default)	GPI[64][4] ADC1_AN[5]/ ADC3_AN[4]	SIUL2-GPI[64]	General Purpose Input E[0]	I	68	T13
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[2]	MSCR[66]	0000 (Default)	GPI[66][4] ADC0_AN[5]	SIUL2-GPI[66]	General Purpose Input E[2]	I	49	U6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[4]	MSCR[68]	0000 (Default)	GPI[68][4] ADC0_AN[7]	SIUL2-GPI[68]	General Purpose Input E[4]	I	42	U4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[5]	MSCR[69]	0000 (Default)	GPI[69][4] ADC0_AN[8]	SIUL2-GPI[69]	General Purpose Input E[5]	I	44	T5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[6]	MSCR[70]	0000 (Default)	GPI[70][4] ADC0_ADC2_AN[4]	SIUL2-GPI[70]	General Purpose Input E[6]	I	46	R6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[7]	MSCR[71]	0000 (Default)	GPI[71][4] ADC0_AN[6]	SIUL2-GPI[71]	General Purpose Input E[7]	I	48	T6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[9]	MSCR[73]	0000	GPI[73][4] ADC1_AN[7]/ ADC3_AN[6]	SIUL2-GPI[73]	General Purpose Input E[9]	I	61	U10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[113]	0010	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I		
H[13]	MSCR[125]	0000 (Default)	GPIO[125]	SIUL2-GPIO[125]	General Purpose IO H[13]	I/O		A14
		0001	X3	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 3	I/O		
		0010	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[74]	0010	ETC3	eTimer_2	eTimer_2 Input Data Channel 3	I		
H[14]	MSCR[126]	0000 (Default)	GPIO[126]	SIUL2-GPIO[126]	General Purpose IO H[14]	I/O		P13
		0001	A3	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 3	I/O		
		0010	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[75]	0010	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I		
H[15]	MSCR[127]	0000 (Default)	GPIO[127]	SIUL2-GPIO[127]	General Purpose IO H[15]	I/O		C17
		0001	B3	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 3	I/O		
		0010	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[76]	0010	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I		
I[0]	MSCR[128]	0000 (Default)	GPIO[128]	SIUL2-GPIO[128]	General Purpose IO I[0]	I/O		C6
		0001	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O		
		0010	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0011-1111	—	Reserved	—	—		
	IMCR[71]	0010	ETC0	eTimer_2	eTimer_2 Input Data Channel 0	I		
	IMCR[100]	0001	FAULT0	FlexPWM_1	FlexPWM_1 Fault Input 0	I		
I[1]	MSCR[129]	0000 (Default)	GPIO[129]	SIUL2-GPIO[129]	General Purpose IO I[1]	I/O		T3
		0001	ETC1	eTimer_2	eTimer_2 Input/Output Data Channel 1	I/O		

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0001	I/O-Pad	C[5]
			0010	I/O-Pad	D[8]
			0011	I/O-Pad	G[11]
			0100-1111	—	Reserved
FlexPWM_0	EXT_SYNC	IMCR[87]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved
FlexPWM_0	A0	IMCR[88]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010	I/O-Pad	D[10]
			0011-1111	—	Reserved
FlexPWM_0	B0	IMCR[89]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010	I/O-Pad	D[11]
			0011-1111	—	Reserved
FlexPWM_0	A1	IMCR[91]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[7]
			0010	I/O-Pad	C[15]
			0011	I/O-Pad	F[0]
			0100-1111	—	Reserved
FlexPWM_0	B1	IMCR[92]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[6]
			0010	I/O-Pad	D[0]
			0011	I/O-Pad	D[14]
			0100-1111	—	Reserved
FlexPWM_0	X1	IMCR[93]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[4]
			0010	I/O-Pad	D[12]
			0011-1111	—	Reserved
FlexPWM_0	A2	IMCR[94]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010	I/O-Pad	A[12]
			0011	I/O-Pad	G[3]
			0100-1111	—	Reserved
FlexPWM_0	B2	IMCR[95]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[12]
			0010	I/O-Pad	A[13]
			0011	I/O-Pad	G[4]

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0100-1111	—	Reserved
FlexPWM_0	X2	IMCR[96]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010	I/O-Pad	G[2]
			0011-1111	—	Reserved
FlexPWM_0	A3	IMCR[97]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[2]
			0010	I/O-Pad	C[10]
			0011	I/O-Pad	D[3]
			0100	I/O-Pad	G[6]
			0101-1111	—	Reserved
FlexPWM_0	B3	IMCR[98]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010	I/O-Pad	A[9]
			0011	I/O-Pad	D[4]
			0100	I/O-Pad	G[7]
			0101-1111	—	Reserved
FlexPWM_0	X3	IMCR[99]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[2]
			0010	I/O-Pad	D[6]
			0011	I/O-Pad	G[5]
			0100-1111	—	Reserved
FlexPWM_1	FAULT0	IMCR[100]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[0]
			0010-1111	—	Reserved
FlexPWM_1	FAULT1	IMCR[101]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[1]
			0010-1111	—	Reserved
FlexPWM_1	FAULT2	IMCR[102]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[2]
			0010-1111	—	Reserved
FlexPWM_1	FAULT3	IMCR[103]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[3]
			0010-1111	—	Reserved
FlexPWM_1	A0	IMCR[105]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	H[5]
			0011-1111	—	Reserved
FlexPWM_1	B0	IMCR[106]	0000 (Default)	—	Disable

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0001	I/O-Pad	C[14]
			0010	I/O-Pad	H[6]
			0011-1111	—	Reserved
FlexPWM_1	A1	IMCR[109]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[12]
			0010	I/O-Pad	H[8]
			0011-1111	—	Reserved
FlexPWM_1	B1	IMCR[110]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[13]
			0010	I/O-Pad	H[9]
			0011-1111	—	Reserved
FlexPWM_1	A2	IMCR[112]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[4]
			0010	I/O-Pad	H[11]
			0011-1111	—	Reserved
FlexPWM_1	B2	IMCR[113]	0000	—	Disable
			0001	I/O-Pad	E[14]
			0010	I/O-Pad	H[12]
			0011-1111	—	Reserved
FlexRay	FR_A_RX	IMCR[136]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[1]
			0010-1111	—	Reserved
FlexRay	FR_B_RX	IMCR[137]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[2]
			0010-1111	—	Reserved
LIN_0	RXD	IMCR[165]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[3]
			0010	I/O-Pad	B[7]
			0011-1111	—	Reserved
LIN_1	RXD	IMCR[166]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[13]
			0010	I/O-Pad	D[12]
			0011	I/O-Pad	F[15]
			0100-1111	—	Reserved
MC_RGM	ABS0	IMCR[169]	0000 (Default)	I/O-Pad	A[2]
			0001	—	Disable
			0010-1111	—	Reserved
MC_RGM	ABS2	IMCR[171]	0000 (Default)	I/O-Pad	A[3]
			0001	—	Disable

Table continues on the next page...

Table 11. Peripheral muxing example

SSS field value in IMCR[214]	Result
0001	I/O-Pad I[12] is connected to SENT_1 Receive input SENT_RX[1]
0010	I/O-Pad J[6] is connected to SENT_1 Receive input SENT_RX[1]

See Table 9 concerning the availability of port pins on the packages.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 200 MHz.

3.2 165°C junction temperature option

For orderable parts whose device marking shows they support this extended temperature option:

- Operation at 150°C < T_J < 165°C is allowed for a maximum cumulative time of 200 hours over the device lifetime.
- Production parameters at 165°C reflect testing over an ambient temperature range of –40°C to 150°C with appropriate guardbanding to guarantee operation at 165°C.

3.3 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	90	230	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	120	310	
$I_{DD\_LV\_HALT}$	Operating current in V_{DD} HALT mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	25	40	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	110	300	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	140	400	
$I_{DD\_LV\_LFAST}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.6	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.8	
$I_{DD\_LV\_NEXUS}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.1	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.5	
$I_{DD\_HV\_ADV}$[3]	Operating current	T_J = 150 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.4	4.2	mA
		T_J = 165 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.5	4.5	
$I_{DD\_HV\_ADRE}$'[4]	Operating current	T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.20	0.28	mA
		T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.32	0.50	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.24	0.40	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.40	0.70	
$I_{DD\_HV\_OSC}$	Operating current	T_J = 150 °C 3.3 V supplies	—	—	1.6	mA

Table continues on the next page...

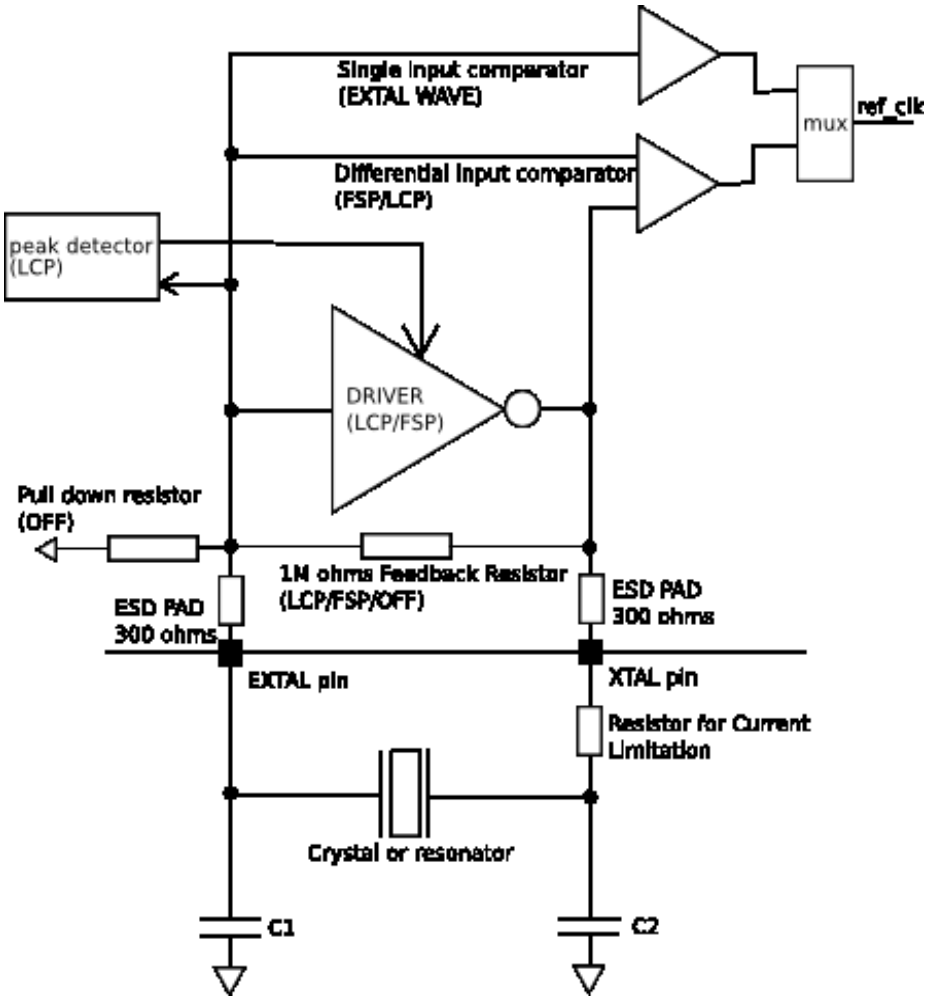


Figure 5. Oscillator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions[1]	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP	—	4[2]	—	40	MHz
$g_{mXOSCHS}$	Driver transconductance	LCP	$V_{DD\_HV\_OSC}$ = 3.3V	—	20	—	mA/V
		FSP	–5%, +10%	—	30	—	
V_{XOSCHS}	Oscillation amplitude	LCP	f_{OSC} = 4, 8, 16 MHz	1.1	1.3	2.6	V
			f_{OSC} = 40 MHz	1.2	1.5	1.7	V
$T_{XOSCHSSU}$	Oscillator startup time	FSP/LCP[3]	f_{OSC} = 4 MHz	1.75	2.5	2.9	ms
			f_{OSC} = 8, 16, 40 MHz	0.25	0.5	1.1	ms

Table continues on the next page...

Table 35. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UTO-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UTO-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.16.3 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

NOTE

If the user does not follow these recommended settings, the user must run the flash memory's array integrity (AI) check with breakpoints disabled: Set the Array Integrity Break Point Enable bit in the C55FMC's UTest 0 register (C55FMC_UT0[AIBPE]) to 0.

Table 36. Flash memory read wait-state and address-pipeline control combinations

Operating frequency (f_{CPU} = SYS_CLK)		RWSC	APC	Flash read latency on mini-cache miss (# of f_{CPU} clock periods)	Flash read latency on mini-cache hit (# of f_{CPU} clock periods)
–40°C to 150°C	Max 165°C option				
0 MHz < f_{CPU} ≤ 33 MHz	0 MHz < f_{CPU} ≤ 30 MHz	0	0	3	1
33 MHz < f_{CPU} ≤ 100 MHz	30 MHz < f_{CPU} ≤ 90 MHz	2	1	5	1
100 MHz < f_{CPU} ≤ 133 MHz	90 MHz < f_{CPU} ≤ 120 MHz	3	1	6	1

Table continues on the next page...

3.18 RESET sequence duration

This following table shows the duration of different reset sequences. See the chip's Reference Manual for details about the reset sequences.

Table 38. RESET sequences

Symbol	Parameter	Conditions	T_{Reset}			Unit
			Min	Typ	Max[1]	
T_{DRB}	'Destructive' reset sequence, BIST enabled	Self test clock in STCU is the PLL generated clock. Self test configuration as per DCF record programming. For four LBIST partitions in design, two LBIST partitions are run in parallel.	—	—	18.0	ms
T_{DR}	'Destructive' reset sequence, BIST disabled	—	—	440	480	µs
T_{ERLB}	External reset sequence—long, BIST enabled	Self test clock in STCU is the PLL generated clock. Self test configuration as per DCF record programming. For four LBIST partitions in design, two LBIST partitions are run in parallel.	—	—	17.5	ms
T_{ERL}	External reset sequence—long, BIST disabled	—	—	120	150	µs
T_{FRL}	Functional reset sequence—long	—	—	165	180	µs
T_{FRS}	Functional reset sequence—short	—	—	10.0	12.0	µs

1. The maximum value applies only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

3.19 AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +165°C and for the full operating range of the V_{DD_IO} supply defined in DC electrical characteristics.

Table 39. Functional Pad AC Specifications

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn's SRC[1:0] field
	Min	Max	Min	Max		MSB,LSB
I/O (output)	2.5/2.5	7.5/7.5	0.9/0.9	3/3	50	11
	—	—	—	12/12	200	

Table continues on the next page...

Table 39. Functional Pad AC Specifications (continued)

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn's SRC[1:0] field
	Min	Max	Min	Max		MSB,LSB
	—	8/8	—	3.5/3.5	25	10
	—	11.5/11.5	—	6.5/6.5	50	
	—	—	—	30/30	200	
	—	45/45	—	25/25	50	01
	—	65/65	—	30/30	200	
	—	75/75	—	40/40	50	00[2]
	—	110/110	—	50/50	200	
I/O (input)	—	1.5/1.5	—	0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

3.19.1 Reset pad (EXT_POR, RESET) electrical characteristics

The device implements a dedicated bidirectional RESET pin.

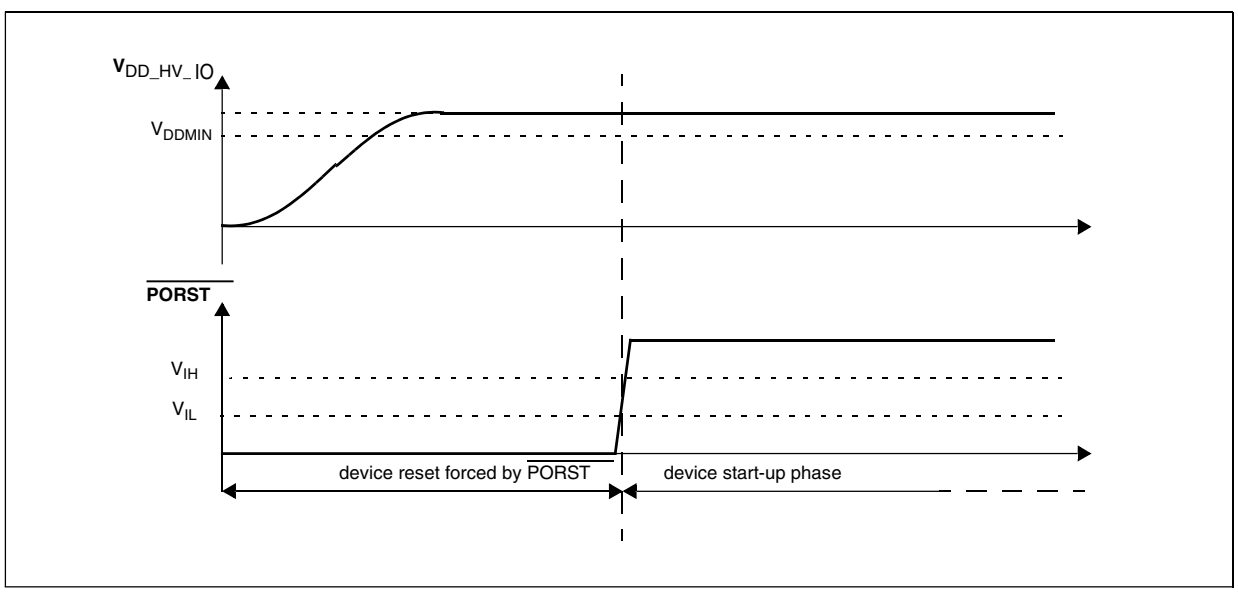


Figure 9. Start-up reset requirements

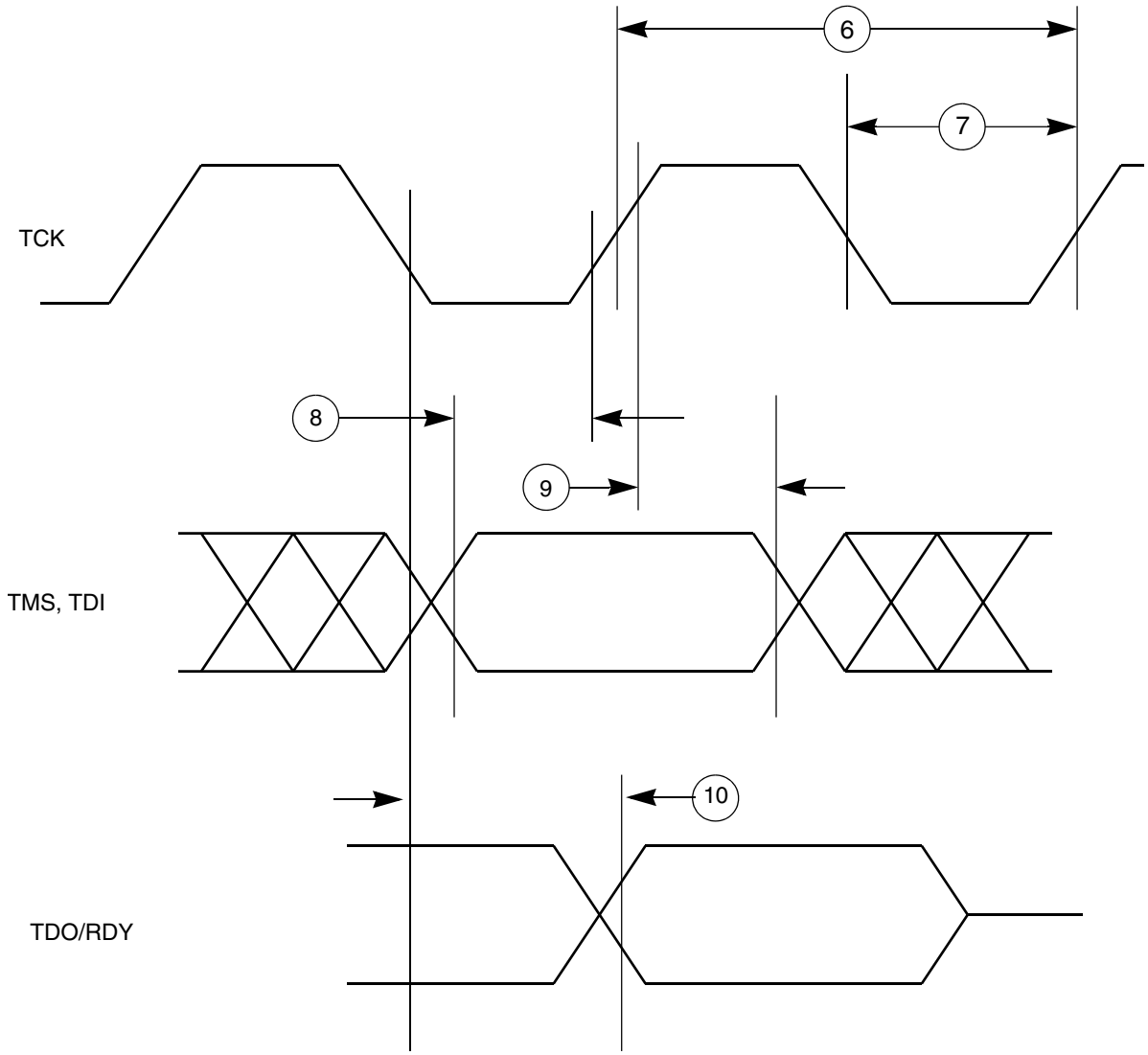


Figure 17. Nexus TDI, TMS, TDO timing

3.19.3.3 Aurora LVDS driver electrical characteristics

Table 45. Aurora LVDS driver electrical characteristics

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
Data Rate					
DATARATE	Data rate	—	1250	Typ+0.1%	Mbps
STARTUP					
T_{STRT_BIAS}	Bias startup time[2]	—	—	5	µs
T_{STRT_TX}	Transmitter startup time[3]	—	—	5	µs
T_{STRT_RX}	Receiver startup time[4]	—	—	4	µs

1. Conditions for these values are $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.

3. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.19.3.4 Nexus Aurora debug port timing

Table 46. Nexus Aurora debug port timing

#	Symbol	Characteristic	Min	Max	Unit
1	t_{REFCLK}	Reference clock frequency	625	1250	MHz
2	t_{RCDC}	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	Reference Clock Stability	50	—	PPM
5	BER	Bit Error Rate	—	10^{-12}	—
6	J_D	Transmit lane Deterministic Jitter	—	0.17	OUI
7	J_T	Transmit lane Total Jitter	—	0.35	OUI
8	S_O	Differential output skew	—	20	ps
9	S_{MO}	Lane to lane output skew	—	1000	ps
10	UI	Aurora lane Unit Interval	800	1600	ps

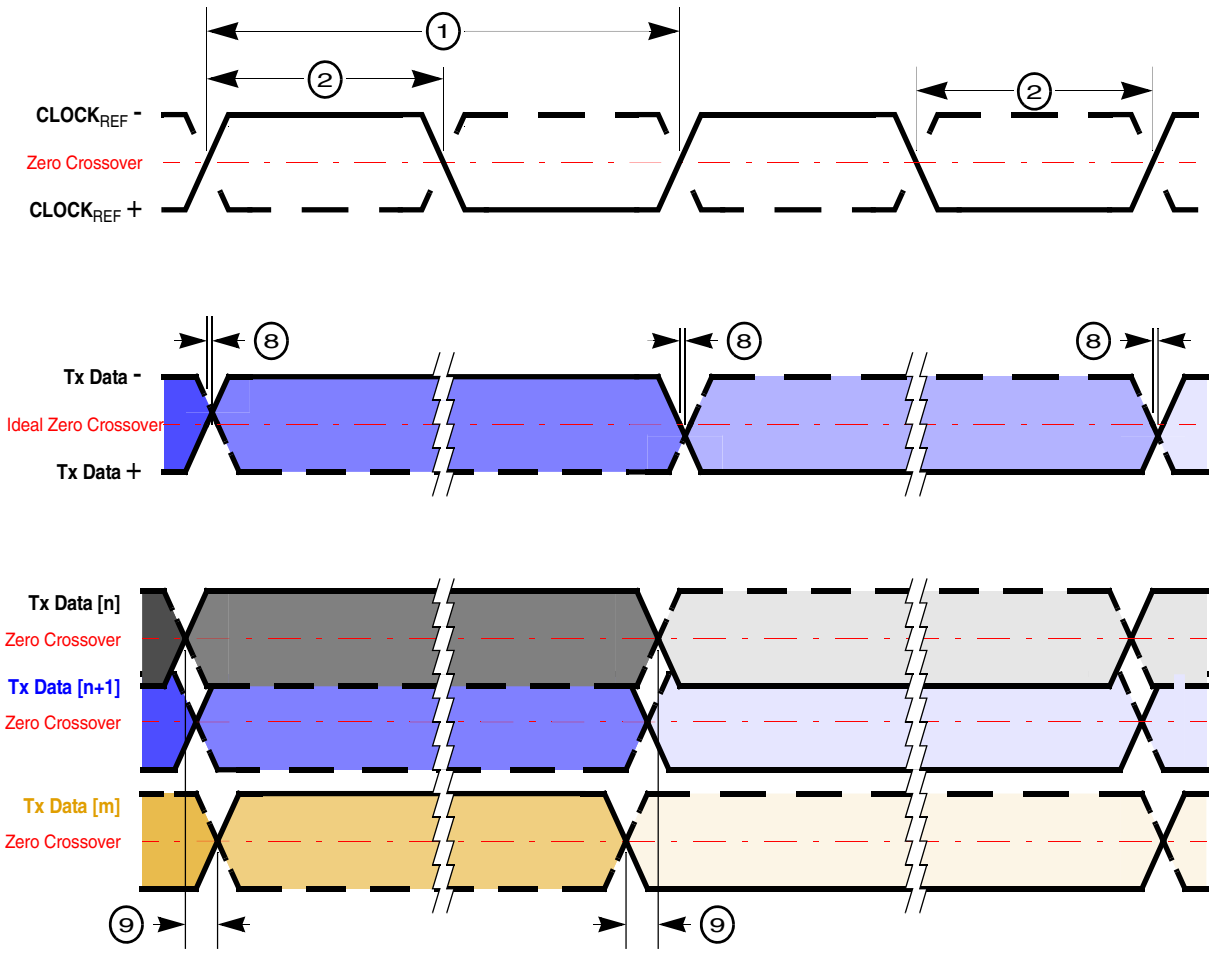


Figure 18. Nexus Aurora timings

Rise/fall timing for the Nexus Aurora debug port reference clock must conform to the area between the minimum and maximum value ranges shown in the following receiver "eye" diagram.

Table 50. LFAST electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
F_{VCO}	PLL VCO Frequency	—	—	320	—	MHz
T_{LOCK}	PLL Phase Lock	—	—	—	40	µs
ΔPER	PLL Long Term Jitter (peak to peak)	—	—	—	600	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.

3.19.7 FlexRay

3.19.7.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

3.19.7.2 TxEN

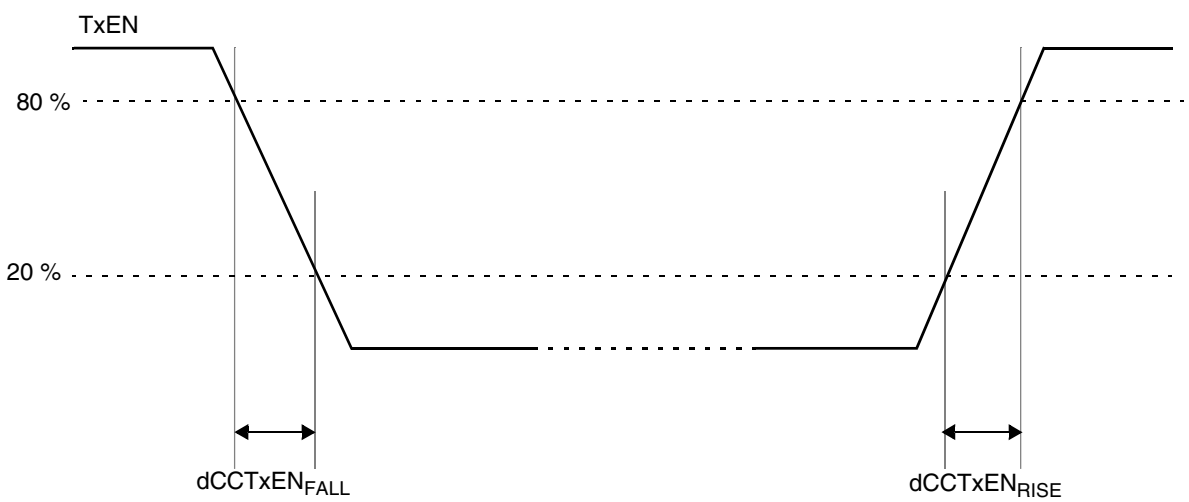
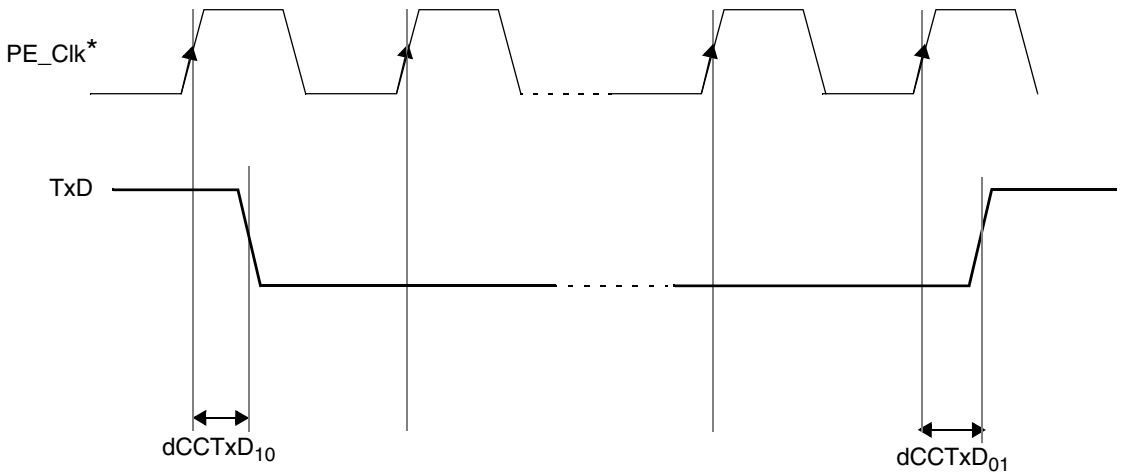


Figure 33. FlexRay TxEN signal



*FlexRay Protocol Engine Clock

Figure 36. FlexRay TxD signal propagation delays

3.19.7.4 RxD

Table 53. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 / 165 °C

3.19.7.5 Receiver asymmetry

Table 54. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	–31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	–30.5	+43.0	ns

1. All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. Not all configurations are available in the PPC parts.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 58. Revision history

Revision	Date	Description of changes

6	05/2017	Changed Freescale to NXP throughout the document.
		
		Extensively updated Generic pins/balls.
		
		Absolute maximum ratings
		• In Table 12
		  • for row set I_{INJ} changed "Maximum DC injection current per pin, 5 V pads" to "Maximum DC injection current per pin, 5V ADC pads".
		  • For row set I_{INJ} updated the footnote.
		
		Voltage regulator electrical characteristics
		• In Table 17
		  • Added the note, "The device has to.....which drives the EXT_POR".
		  • In existing row C_{ld} added Maximum value 18.8.
		  • In existing row C_{pd} added Maximum value 300.
		  • Renamed parameter from "Load Current transient" to "Load current transient time" and updated the Min and Max value.
		  • Renamed the following parameters:
		  • Supply ramp rate VDD12_CORE to Supply ramp rate VDD_LV_COR
		  • Supply ramp rate VDD33_REG to Supply ramp rate VDD_HV_PMU
		  • POR VDD12_CORE to POR_COR
		  • POR VDD33_REG to POR_PMU
		• In Figure 4 changed VDD33_REG to VDD_HV_PMU.
		
		16 MHz Internal RC Oscillator (IRCOSC) electrical specifications
		• In Table 26
		  • Changed the Min and Max values for IRCOSC frequency (untrimmed) parameter.
		  • Added IRC frequency variation with temperature and voltage compensation parameter row.
		
		ADC electrical characteristics
		• Changed the Note from "Unless noted otherwise, the specifications in Table 27 assume the use of 13-bit resolution: In ADC_CALBISTREG, set OPMODE to 110b" to "Unless noted otherwise, the specifications in Table 27 assume the use of 12-bit resolution (high accuracy, recommended): In ADC_CALBISTREG, set OPMODE to 110b".
		• In Table 27 for existing rows t_{sample} and t_{conv} changed the "13 bit resolution" to "12-bit resolution (high accuracy, recommended)".
		
		• In Flash memory program and erase specifications changed symbols for specifications:
		  • Quad-page (1024 bits) program time: Changed symbol from t_{qppgn} to t_{qppgm}
		  • 16 KB Block program time: Changed symbol from t_{16kpgn} to t_{16kpgm}
		• In Flash memory Array Integrity and Margin Read specifications incorporated minor editorial changes
		• In Flash memory AC timing specifications for t_{psus}:

Table continues on the next page...

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