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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	79
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pfk1amlq8

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Table 2. Flash memory and SRAM sizes of MPC5744P, MPC5743P, MPC5742P, and MPC5741P

Part number	Flash memory	SRAM
MPC5744P	2.5 MB	384 KB
MPC5743P	2.0 MB	256 KB
MPC5742P	1.5 MB	192 KB
MPC5741P	1.0 MB	128 KB

1.2 Block Diagram

The following figure is a top-level diagram that shows the functional organization of the system.

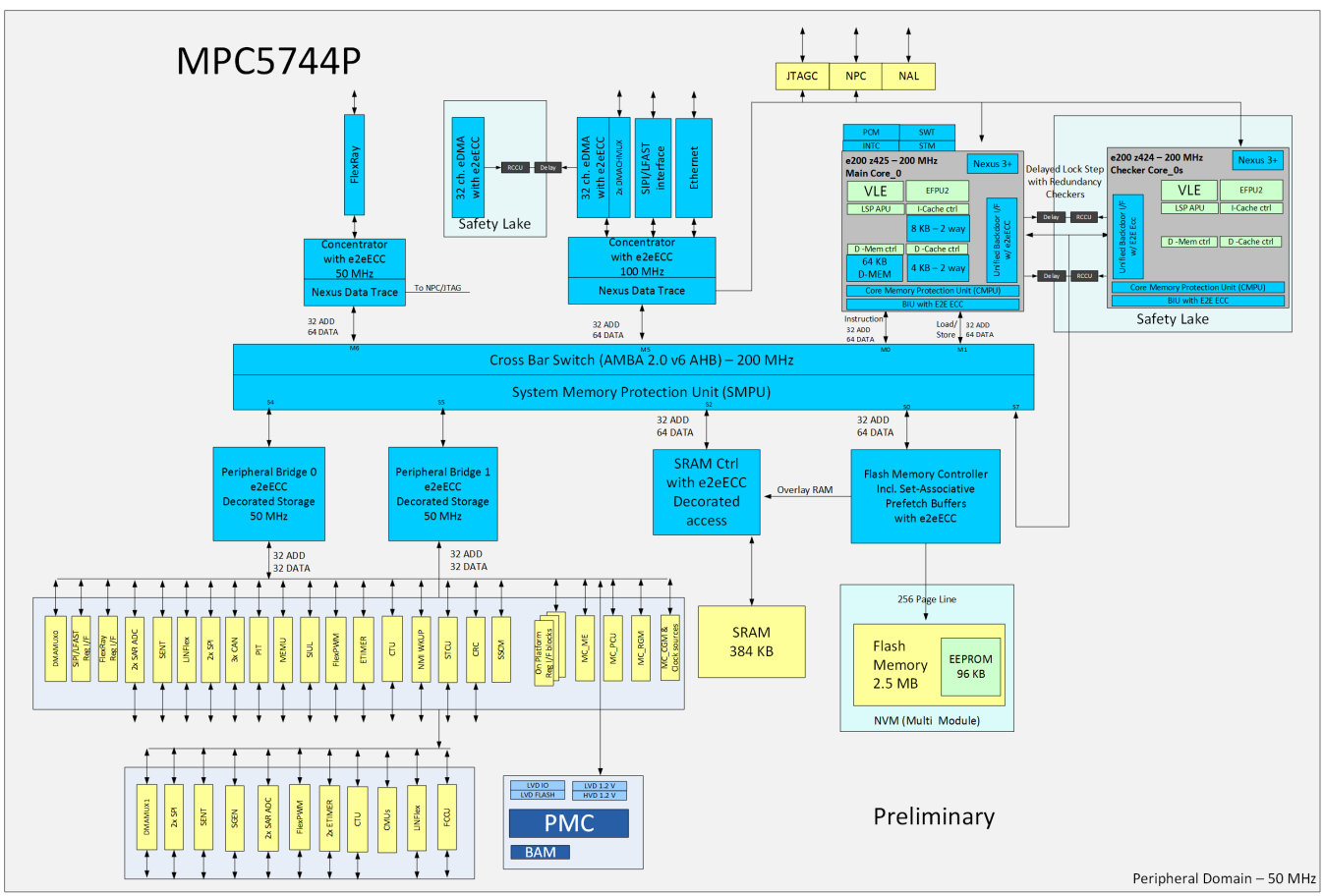

Figure 1. System Block Diagram

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	Type	Description	144LQFP	257MAPBGA
				L6
				L12
				M6
				M7
				M8
				M9
				M10
				M11
				M12
$V_{SS\_LV\_COR}$	Ground	Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144LQFP (pin 35).	17	B1
			35	G7
			40	G8
			71	G9
			94	G10
			96	G11
			132	H7
			137	H8
				H9
				H10
				H11
				J7
				J8
				J9
				J10
				J11
				K7
				K8
				K9
				K10
				K11
				L7
				L8
				L9
				L10
				L11
$V_{DD\_LV\_PLL}$	Power	PLL low voltage Supply	36	P4
$V_{SS\_LV\_PLL}$	Ground	PLL low voltage Ground	35	N4

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	**Type**	**Description**	**144LQFP**	**257MAPBGA**
$V_{DD\_HV\_IO}$	Power	High voltage Power Supply for I/O	6	A9
			21	B2
			72	B16
			91	D8
			126	D14
				G2
				M2
				T2
				T16
				U14
$V_{SS\_HV\_IO}$	Ground	High voltage Ground Supply for I/O	7	A1
			22	A2
			90	A16
			127	A17
				B1
				B9
				B17
				C3
				C15
				D9
				H2
				N2
				R3
				R15
				T1
				T17
				U1
				U2
				U16
				U17
$V_{DD\_HV\_PMU}$ $V_{DD\_HV\_PMU\_AUX}$	Power	PMU high voltage Supply	72	U14
$V_{DD\_HV\_OSC}$	Power	Power Supply for the oscillator	27	M1
$V_{SS\_HV\_OSC}$	Ground	Ground Supply for the oscillator	28	P1
$V_{DD\_HV\_FLA}$	Power	Power Supply and decoupling pin for flash memory	97	H16
$V_{DD\_HV\_ADV}$	Power	High voltage Supply for ADC, TSENS, SGEN (3.3 V)	58	T10
$V_{SS\_HV\_ADV}$	Ground	High voltage Ground for ADC	59	U9

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0011	DEBUG1	SSCM	SSCM Debug Output 1	O		
		0100-1111	—	Reserved	—	—		
	IMCR[32]	0010	RXD	CAN0	CAN 0 Receive Pin	I		
	IMCR[33]	0010	RXD	CAN1	CAN 1 Receive Pin	I		
	IMCR[68]	0001	ETC3	eTimer_1	eTimer_1 Input Data Channel 3	I		
	IMCR[189]	0001	REQ16	SIUL2	SIUL2 External Interrupt Source 16	I		
B[2]	MSCR[18]	0000 (Default)	GPIO[18]	SIUL2-GPIO[18]	General Purpose IO B[2]	I/O	114	C12
		0001	TXD	LIN0	LINFlexD 0 Transmit Pin	O		
		0010	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0011	DEBUG2	SSCM	SSCM Debug Output 2	O		
		0100-1111	—	Reserved	—	—		
	IMCR[190]	0001	REQ17	SIUL2	SIUL2 External Interrupt Source 17	I		
B[3]	MSCR[19]	0000 (Default)	GPIO[19]	SIUL2-GPIO[19]	General Purpose IO B[3]	I/O	116	B12
		0001	—	Reserved	—	—		
		0010	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0011	DEBUG3	SSCM	SSCM Debug Output 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[165]	0001	RXD	LIN0	LIN 0 Receive Pin	I		
B[4]	MSCR[20]	0	GPIO[20]	SIUL2-GPIO[20]	General Purpose IO B[4]	I/O	89	G14
		0001 (Default)	TDO	NPC_HNDSHK	NPC_HNDSHK Test Data Out (TDO)	O		
		0010-1111	—	Reserved	—	—		
B[5]	MSCR[21]	0000 (Default)	GPIO[21]	SIUL2-GPIO[21]	JTAGC Test Data In (TDI)[3] General Purpose IO B[5]	I/O	86	J17
		0001	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0010-1111	—	Reserved	—	—		
B[6]	MSCR[22]	0000 (Default)	GPIO[22]	SIUL2-GPIO[22]	General Purpose IO B[6]	I/O	138	B5
		0001	CLK_OUT	MC_CGM	CGM Clock out for off-chip use and observation	O		
		0010	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O		
		0011-1111	—	Reserved	—	—		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[63]	0001	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
	IMCR[192]	0001	REQ19	SIUL2	SIUL2 External Interrupt Source 19	I		
B[15]	MSCR[31]	0000 (Default)	GPI[31][4] ADC1_AN[2]	SIUL2-GPI[31]	General Purpose Input B[15]	I	62	R11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[193]	0001	REQ20	SIUL2	SIUL2 External Interrupt Source 20	I		
C[0]	MSCR[32]	0000 (Default)	GPI[32][4] ADC1_AN[3]	SIUL2-GPI[32]	General Purpose Input C[0]	I	66	R12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[1]	MSCR[33]	0000 (Default)	GPI[33][4] ADC0_AN[2]	SIUL2-GPI[33]	General Purpose Input C[1]	I	41	T4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[2]	MSCR[34]	0000 (Default)	GPI[34][4] ADC0_AN[3]	SIUL2-GPI[34]	General Purpose Input C[2]	I	45	U5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[4]	MSCR[36]	0000 (Default)	GPIO[36]	SIUL2-GPIO[36]	General Purpose IO C[4]	I/O	11	H3
		0001	CS0	DSPI0	DSPI 0 Peripheral Chip Select 0	I/O		
		0010	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0011	DEBUG4	SSCM	SSCM Debug Output 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[93]	0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input 1	I		
	IMCR[195]	0001	REQ22	SIUL2	SIUL2 External Interrupt Source 22	I		
C[5]	MSCR[37]	0000 (Default)	GPIO[37]	SIUL2-GPIO[37]	General Purpose IO C[5]	I/O	13	G3
		0001	SCK	DSPI0	DSPI 0 Input/Output Serial Clock	I/O		
		0010	—	Reserved	—	—		
		0011	DEBUG5	SSCM	SSCM Debug Output 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0001	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
C[15]	MSCR[47]	0000 (Default)	GPIO[47]	SIUL2-GPIO[47]	General Purpose IO C[15]	I/O	124	A8
		0001	FR_A_TXEN	FLEXRAY	FlexRay Transmit Enable Channel A	O		
		0010	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[38]	0010	EXT_IN	CTU_0	CTU 0 External Trigger Input	I		
	IMCR[65]	0010	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I		
	IMCR[87]	0010	EXT_SYNC	FlexPWM_0	FlexPWM_0 External Sync Input	I		
	IMCR[91]	0010	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I		
D[0]	MSCR[48]	0000 (Default)	GPIO[48]	SIUL2-GPIO[48]	General Purpose IO D[0]	I/O	125	B8
		0001	FR_A_TX	FLEXRAY	FlexRay Transmit Data Channel A	O		
		0010	ETC1	eTimer_1	eTimer_1 Input/Output Data Channel 1	I/O		
		0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[66]	0010	ETC1	eTimer_1	eTimer_1 Input Data Channel 1	I		
	IMCR[92]	0010	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I		
D[1]	MSCR[49]	0000 (Default)	GPIO[49]	SIUL2-GPIO[49]	General Purpose IO D[1]	I/O	3	E3
		0001	—	Reserved	—	—		
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O		
		0011	EXT_TGR	CTU_0	CTU 0 External Trigger Output	O		
		0100-1111	—	Reserved	—	—		
	IMCR[67]	0011	ETC2	eTimer_1	eTimer_1 Input Data Channel 2	I		
	IMCR[136]	0001	FR_A_RX	FLEXRAY	FlexRay Channel A Receive Pin	I		
D[2]	MSCR[50]	0000 (Default)	GPIO[50]	SIUL2-GPIO[50]	General Purpose IO D[2]	I/O	140	B4
		0001	—	Reserved	—	—		
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0011-1111	—	Reserved	—	—		
D[10]	MSCR[58]	0000 (Default)	GPIO[58]	SIUL2-GPIO[58]	General Purpose IO D[10]	I/O	76	R16
		0001	A0	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	TX_D2	ENET_0	Ethernet MII transmit data	O		
		0100	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0110-1111	—	Reserved	—	—		
	IMCR[52]	0010	CS0	DSPI3	DSPI 3 Peripheral chip Select 0	I		
	IMCR[59]	0001	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I		
	IMCR[88]	0010	A0	FlexPWM_0	FlexPWM_0 Channel A Input 0	I		
D[11]	MSCR[59]	0000 (Default)	GPIO[59]	SIUL2-GPIO[59]	General Purpose IO D[11]	I/O	78	P17
		0001	B0	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		
		0100	SCK	DSPI3	DSPI 3 Input/Output Serial Clock	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0010	SCK	DSPI3	DSPI 3 Input Serial Clock	I		
	IMCR[60]	0001	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I		
	IMCR[89]	0010	B0	FlexPWM_0	FlexPWM_0 Channel B Input 0	I		
D[12]	MSCR[60]	0000 (Default)	GPIO[60]	SIUL2-GPIO[60]	General Purpose IO D[12]	I/O	99	F15
		0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0010	CS6	DSPI1	DSPI 1 Peripheral Chip Select 6	O		
		0011	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0100	SOUT	DSPI3	DSPI 3 Serial Data Output	O		
		0101-1111	—	Reserved	—	—		
	IMCR[93]	0010	X1	FlexPWM_0	FlexPWM_0 Channel X Input 1	I		
	IMCR[166]	0010	RXD	LIN1	LIN 1 Receive Pin	I		
D[14]	MSCR[62]	0000 (Default)	GPIO[62]	SIUL2-GPIO[62]	General Purpose IO D[14]	I/O	105	E17

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
E[10]	MSCR[74]	0000 (Default)	GPI[74][4] ADC1_AN[8]/ ADC3_AN[7]	SIUL2-GPI[74]	General Purpose Input E[10]	I	63	T11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[11]	MSCR[75]	0000 (Default)	GPI[75][4] ADC1_AN[4]/ ADC3_AN[3]	SIUL2-GPI[75]	General Purpose Input E[11]	I	65	U11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[12]	MSCR[76]	0000 (Default)	GPI[76][4] ADC1_AN[6]/ ADC3_AN[5]	SIUL2-GPI[76]	General Purpose Input E[12]	I	67	T12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[13]	MSCR[77]	0000 (Default)	GPIO[77]	SIUL2-GPIO[77]	General Purpose IO E[13]	I/O	117	A11
		0001	ETC5	eTimer_0	eTimer_0 Input/Output Data Channel 5	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	CS4	DSPI1	DSPI 1 Peripheral Chip Select 4	O		
		0100	SCK	DSPI3	DSPI 3 Input/Output Serial Clock	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0011	SCK	DSPI3	DSPI 3 Input Serial Clock	I		
	IMCR[198]	0001	REQ25	SIUL2	SIUL2 External Interrupt Source 25	I		
	IMCR[64]	0100	ETC5	eTimer_0	eTimer_0 Input Data Channel	I		
E[14]	MSCR[78]	0000 (Default)	GPIO[78]	SIUL2-GPIO[78]	General Purpose IO E[14]	I/O	119	B10
		0001	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0010	SOUT	DSPI3	DSPI 3 Serial Data Out	O		
		0011	CS5	DSPI1	DSPI 1 Peripheral Chip Select 5	O		
		0100	B2	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[70]	0100	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[113]	0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
F[11]	MSCR[91]	0000 (Default)	GPIO[91]	SIUL2-GPIO[91]	General Purpose IO F[11]	I/O	25	L2
		0001	—	Reserved	—	—		
		0010	EVTI_IN	NPC_WRAPPER	Nexus Event In Pin	I		
		0011-1111	—	Reserved	—	—		
F[12]	MSCR[92]	0000 (Default)	GPIO[92]	SIUL2-GPIO[92]	General Purpose IO F[12]	I/O	106	D17
		0001	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0010-0011	—	Reserved	—	—		
		0100	A1	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 1	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[68]	0011	ETC3	eTimer_1	eTimer_1 Input Data Channel 3	I		
	IMCR[109]	0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I		
	IMCR[203]	0001	REQ30	SIUL2	SIUL2 External Interrupt Source 30	I		
F[13]	MSCR[93]	0000 (Default)	GPIO[93]	SIUL2-GPIO[93]	General Purpose IO F[13]	I/O	112	A15
		0001	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0010-0011	—	Reserved	—	—		
		0100	B1	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 1	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[69]	0100	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I		
	IMCR[110]	0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I		
	IMCR[204]	0001	REQ31	SIUL2	SIUL2 External Interrupt Source 31	I		
F[14]	MSCR[94]	0000 (Default)	GPIO[94]	SIUL2-GPIO[94]	General Purpose IO F[14]	I/O	115	D12
		0001	TXD	LIN1	LINFlexD 1 Transmit Pin	O		
		0010	TXD	CAN2	CAN 2 Transmit Pin	O		
		0011-1111	—	Reserved	—	—		
F[15]	MSCR[95]	0000 (Default)	GPIO[95]	SIUL2-GPIO[95]	General Purpose IO F[15]	I/O	113	A13
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[166]	0011	RXD	LIN1	LIN1 RXD	I		
	IMCR[34]	0001	RXD	CAN2	CAN2 RXD	I		

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0101-1111	—	Reserved
DSPI_3	SCK	IMCR[51]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010	I/O-Pad	D[11]
			0011	I/O-Pad	E[13]
			0100	I/O-Pad	I[15]
			0101-1111	—	Reserved
DSPI_3	CS0	IMCR[52]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[11]
			0010	I/O-Pad	D[10]
			0011	I/O-Pad	F[5]
			0100	I/O-Pad	I[14]
			0101-1111	—	Reserved
eTimer_0	ETC0	IMCR[59]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[10]
			0010	I/O-Pad	A[0]
			0011-1111	—	Reserved
eTimer_0	ETC1	IMCR[60]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[11]
			0010	I/O-Pad	A[1]
			0011-1111	—	Reserved
eTimer_0	ETC2	IMCR[61]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
eTimer_0	ETC3	IMCR[62]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[14]
			0010	I/O-Pad	A[3]
			0011-1111	—	Reserved
eTimer_0	ETC4	IMCR[63]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[14]
			0010	I/O-Pad	G[3]
			0011	I/O-Pad	A[4]
			0100	I/O-Pad	C[11]
			0101-1111	—	Reserved
eTimer_0	ETC5	IMCR[64]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[8]
			0010	I/O-Pad	G[4]
			0011	I/O-Pad	C[12]

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
SENT_1	SENT_RX[1]	IMCR[214]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[12]
			0010	I/O-Pad	J[6]
			0011	I/O-Pad	A[10]
			0100	I/O-Pad	G[11]
			0101-1111	—	Reserved
ENET_0	RX_CLK	IMCR[224]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[8]
			0010-1111	—	Reserved
ENET_0	RX_DV	IMCR[225]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[7]
			0010-1111	—	Reserved
ENET_0	RX_D0	IMCR[226]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010-1111	—	Reserved
ENET_0	RX_D1	IMCR[227]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010-1111	—	Reserved
ENET_0	RX_D2	IMCR[228]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[8]
			0010-1111	—	Reserved
ENET_0	RX_D3	IMCR[229]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[9]
			0010-1111	—	Reserved
ENET_0	COL	IMCR[230]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[5]
			0010-1111	—	Reserved
ENET_0	CRS	IMCR[231]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[4]
			0010-1111	—	Reserved
ENET_0	RX_ER	IMCR[232]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[1]
			0010-1111	—	Reserved
ENET_0	TX_CLK	IMCR[233]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[8]
			0010-1111	—	Reserved

1. (Default) = configuration after reset
2. Selecting an alternate function with a 'Reserved' source function causes the pin to enter a null state (Input buffer and Output buffer enables both at 0).

3.16.1.2 Flash memory Array Integrity and Margin Read specifications

Table 29. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.1.3 Flash memory module life specifications

Table 30. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

Table 31. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

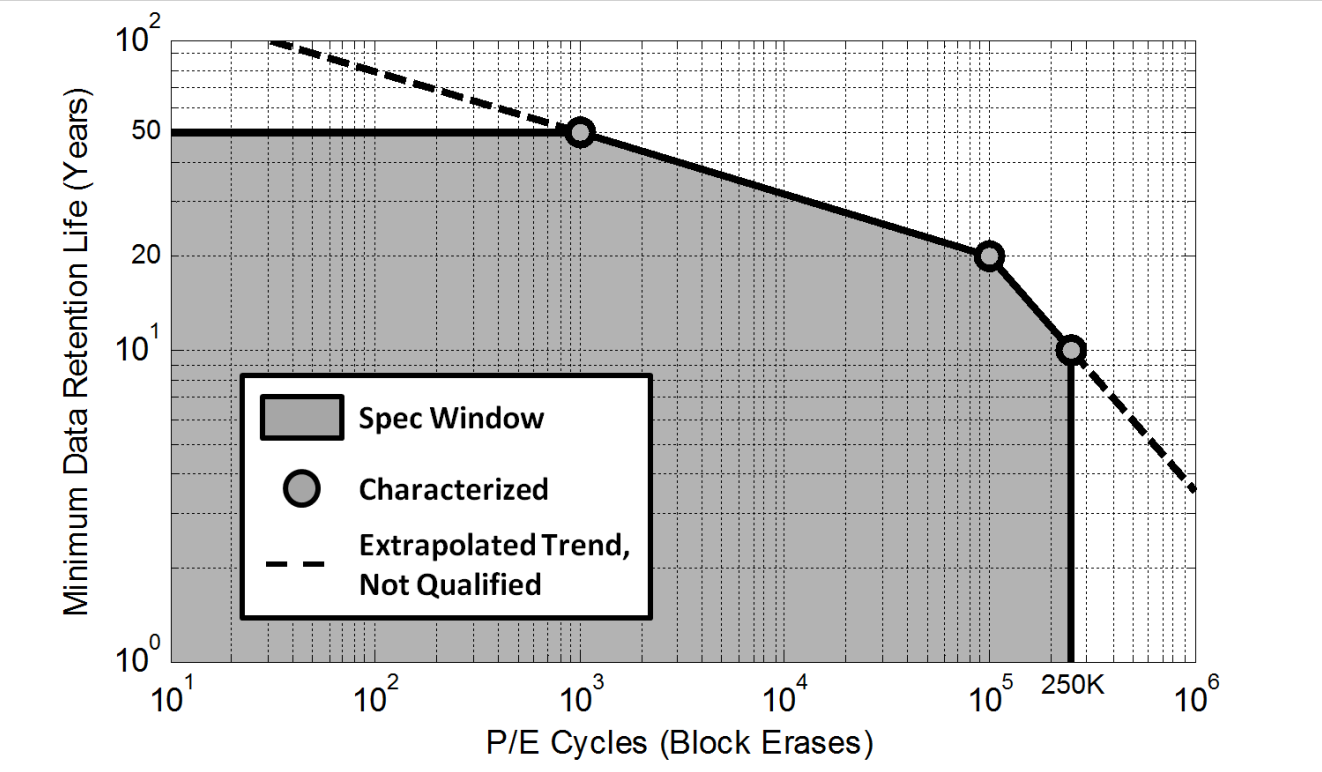
3.16.2 Maximum junction temperature 165°C

3.16.2.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 32 shows the estimated Program/Erase times.



3.16.2.5 Flash memory AC timing specifications

Table 35. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

Maximum junction temperature 165°C

1. These specifications apply to JTAG boundary scan only.

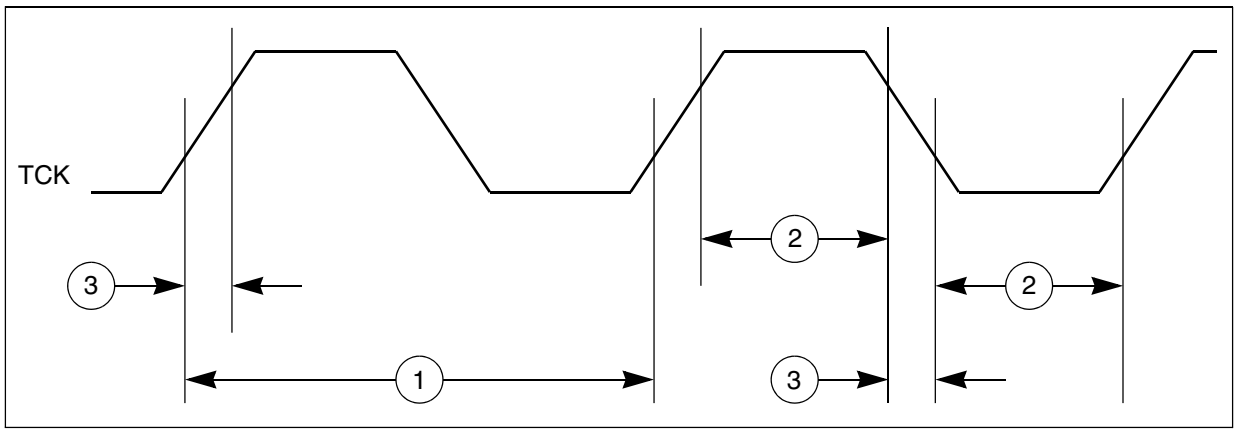


Figure 11. JTAG test clock input timing

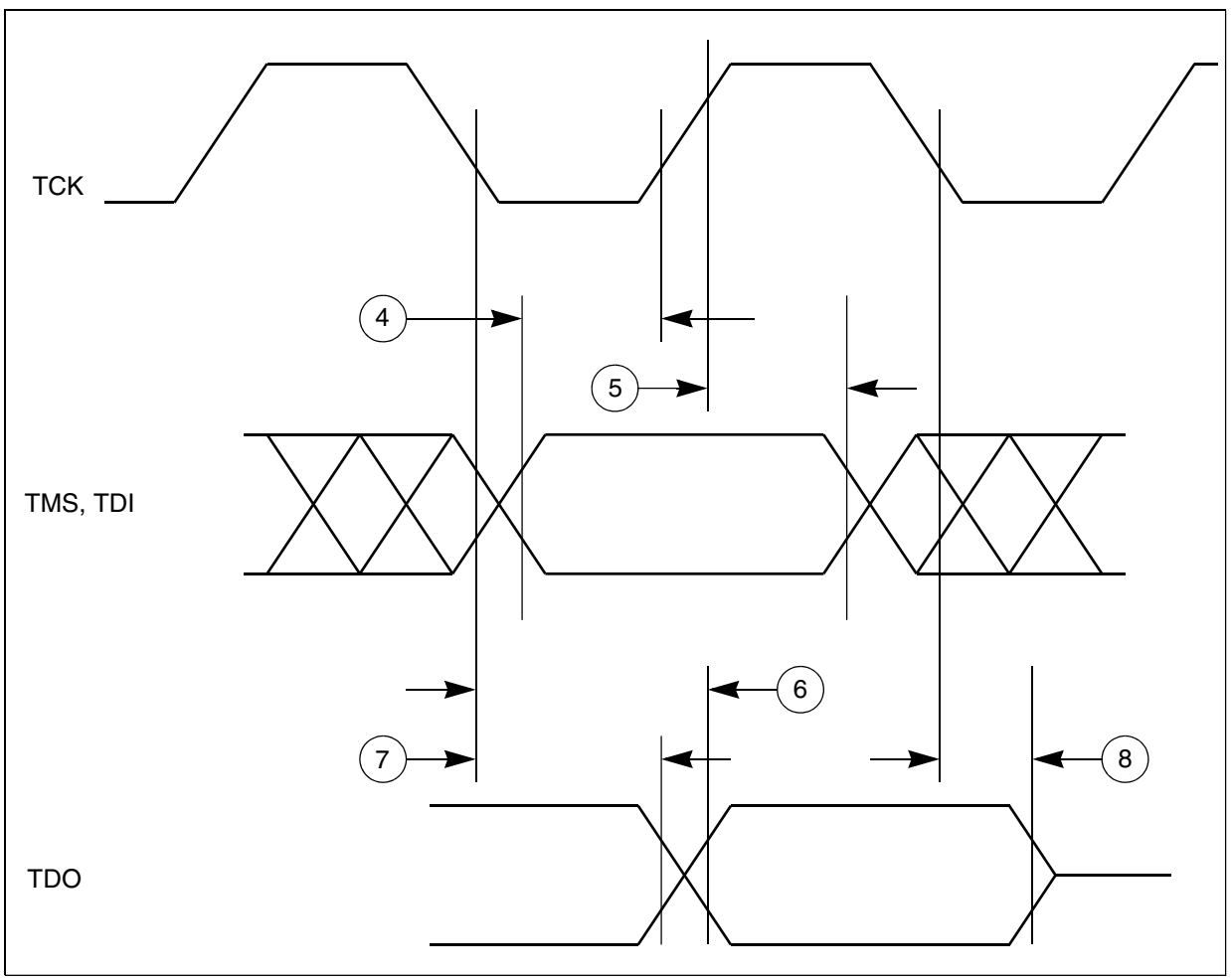


Figure 12. JTAG test access port timing

3. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.19.3.4 Nexus Aurora debug port timing

Table 46. Nexus Aurora debug port timing

#	Symbol	Characteristic	Min	Max	Unit
1	t_{REFCLK}	Reference clock frequency	625	1250	MHz
2	t_{RCDC}	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	Reference Clock Stability	50	—	PPM
5	BER	Bit Error Rate	—	10^{-12}	—
6	J_D	Transmit lane Deterministic Jitter	—	0.17	OUI
7	J_T	Transmit lane Total Jitter	—	0.35	OUI
8	S_O	Differential output skew	—	20	ps
9	S_{MO}	Lane to lane output skew	—	1000	ps
10	UI	Aurora lane Unit Interval	800	1600	ps

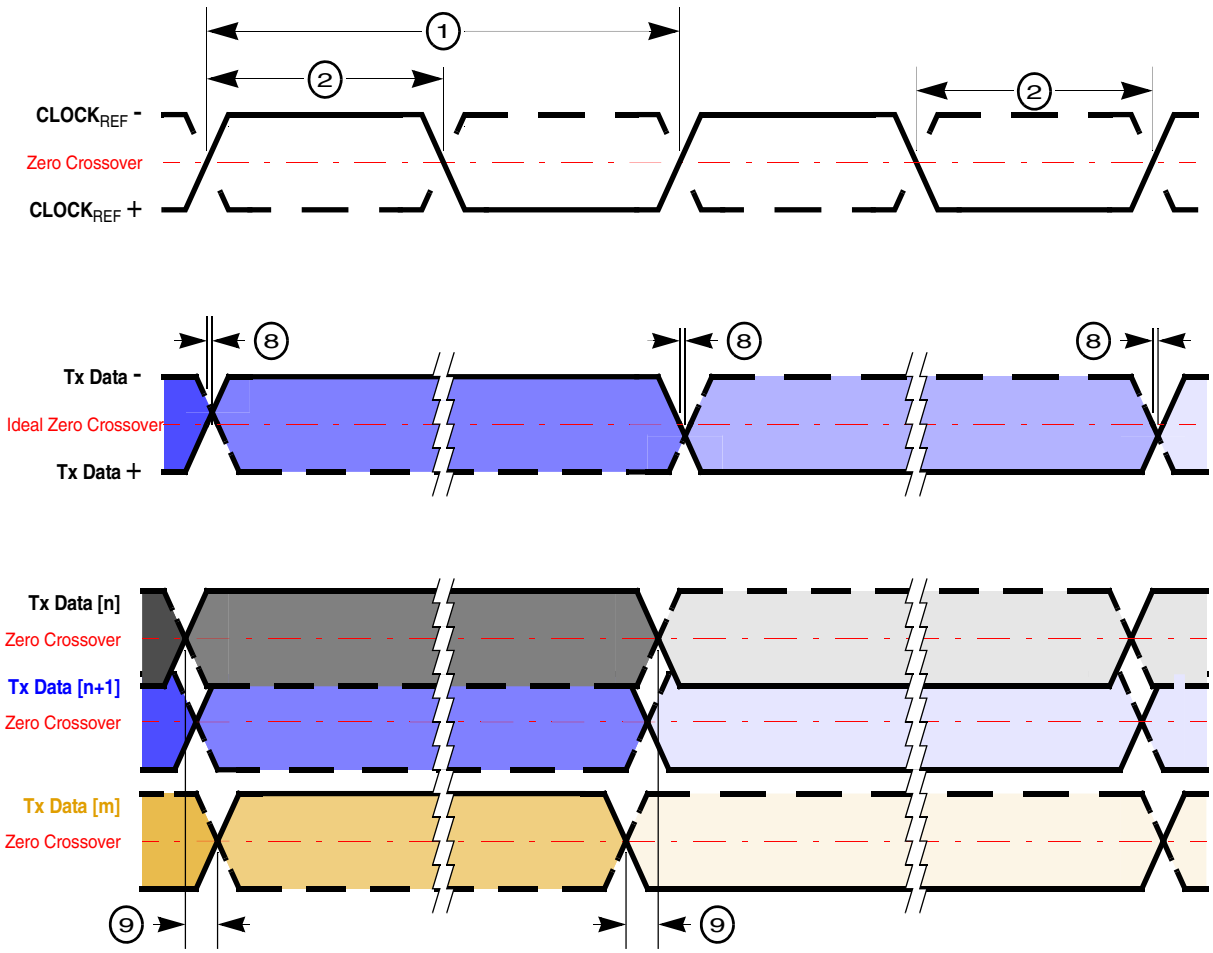


Figure 18. Nexus Aurora timings

Rise/fall timing for the Nexus Aurora debug port reference clock must conform to the area between the minimum and maximum value ranges shown in the following receiver "eye" diagram.

3.19.6.1 LFAST interface timing diagrams

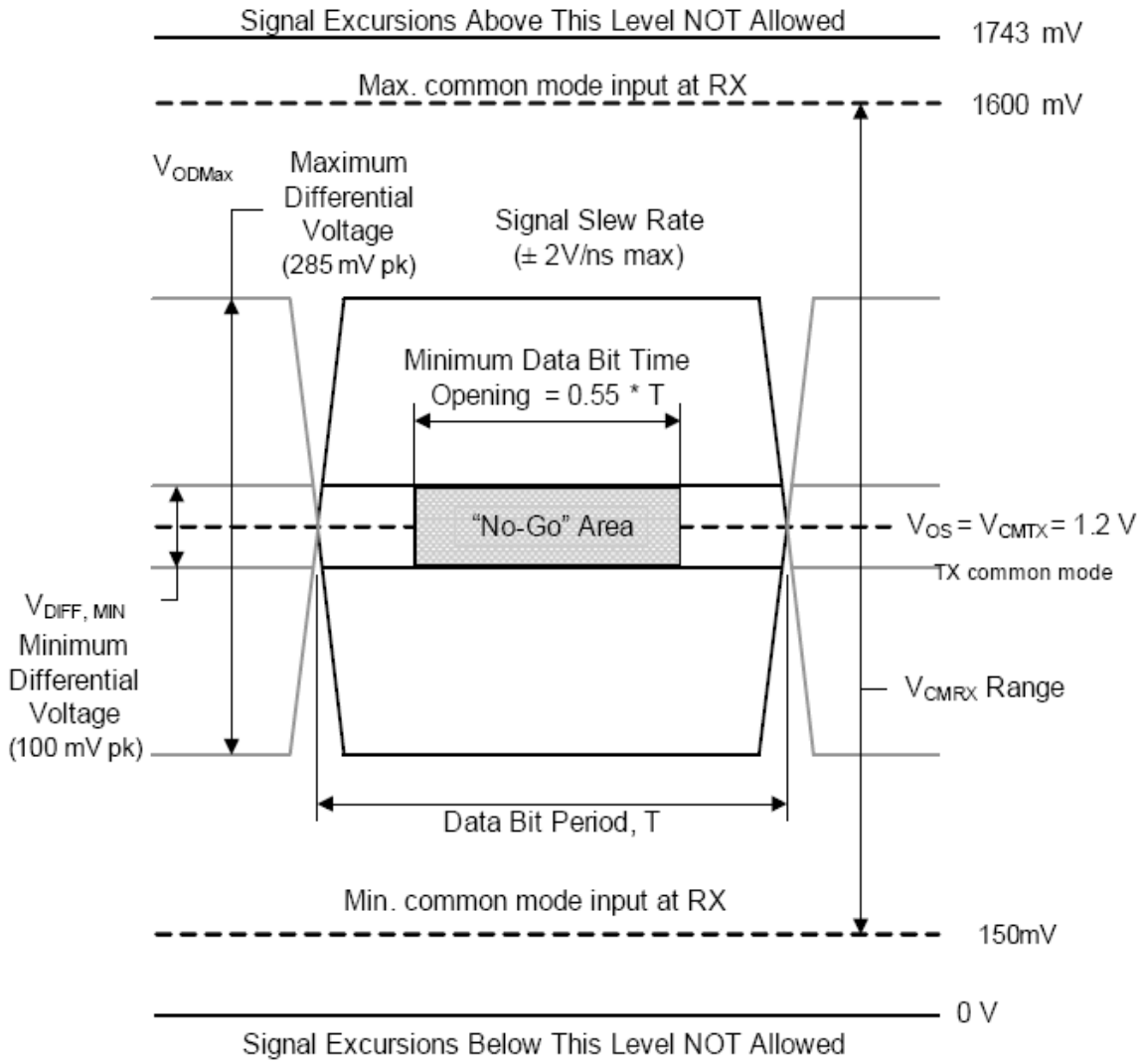


Figure 30. LFAST timing definition

Table 49. LFAST electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
TRANSMITTER						
V_{OS_DRF}	Common mode voltage	—	1.18	—	1.32	V
$\lvert\Delta V_{OD\_DRF}\rvert$	Differential output voltage swing (terminated)	—	100	200	285	mV
T_{TR_DRF}	Rise/Fall time (10% - 90% of swing)	—	0.26	—	1.5	ns
R_{OUT_DRF}	Terminating resistance	—	67	—	198	Ω
C_{OUT_DRF}	Capacitance[6]	—	—	—	5	pF
RECEIVER						
V_{ICOM_DRF}	Common mode voltage	—	0.15[7]	—	1.6[8]	V
$\lvert D_{VI\_DRF}\rvert$	Differential input voltage	—	100	—	—	mV
R_{IN_DRF}	Terminating resistance	—	80	115	150	Ω
C_{IN_DRF}	Capacitance[9]	—	—	3.5	6	pF
L_{IN_DRF}	Parasitic Inductance[10]	—	—	5	10	nH

1. $V_{DD\_VH\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to 165 °C, unless otherwise specified
2. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
5. Startup time is defined as the time taken by LFAST receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
6. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation is needed to verify LFAST template compliancy.
7. Absolute min = 0.15 V – (285 mV / 2) = 0 V
8. Absolute max = 1.6 V + (285 mV / 2) = 1.743 V
9. Total capacitance including silicon, package pin and bond wire
10. Total inductance including silicon, package pin and bond wire

Table 50. LFAST electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
F_{RF_REF}	SysClk Frequency	—	10	—	26	MHz
ERR_{REF}	SysClk Frequency Error	—	-1	—	1	%
DC_{REF}	SysClk Duty Cycle	—	45	—	55	%
C_{LOAD}	Output Buffer Load Capacitance	—	—	—	10	pF
R_{LOAD}	Output Buffer Load Resistance	—	10	—	—	kΩ
PN	Integrated Phase Noise (single side band)	20 MHz	—	—	-58	dBc
		10 MHz	—	—	-64	dBc

Table continues on the next page...