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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	79
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pfk1amlq9

1 Introduction

1.1 Features

The following table summarizes the features of the MPC5744P.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution speed	0 MHz to 200 MHz (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory—see Table 2 for additional details	
Code/data flash memory	**2.5 MB**, ECC, RWW
Data flash memory	Supported with RWW
SRAM	**384 KB**, ECC
Overlay access to SRAM from Flash Memory Controller	Yes
Modules	
Interrupt controller	32 interrupt priority levels, 16 SW programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	Type	Description	144LQFP	257MAPBGA
				L6
				L12
				M6
				M7
				M8
				M9
				M10
				M11
				M12
$V_{SS\_LV\_COR}$	Ground	Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144LQFP (pin 35).	17	B1
			35	G7
			40	G8
			71	G9
			94	G10
			96	G11
			132	H7
			137	H8
				H9
				H10
				H11
				J7
				J8
				J9
				J10
				J11
				K7
				K8
				K9
				K10
				K11
				L7
				L8
				L9
				L10
				L11
$V_{DD\_LV\_PLL}$	Power	PLL low voltage Supply	36	P4
$V_{SS\_LV\_PLL}$	Ground	PLL low voltage Ground	35	N4

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[49]	0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I		
	IMCR[98]	0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I		
A[4]	MSCR[4]	0000 (Default)	GPIO[4]	SIUL2-GPIO[4]	General Purpose IO A[4]	I/O	108	D16
		0001	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0010	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0011	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0100	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[112]	0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I		
	IMCR[177]	0001	REQ4	SIUL2	SIUL2 External Interrupt Source 4	I		
	IMCR[172]	0000 (Default)	FAB	MC_RGM	RGM Force Alternate Boot Mode	I		
	IMCR[65]	0001	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I		
	IMCR[63]	0011	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
A[5]	MSCR[5]	0000 (Default)	GPIO[5]	SIUL2-GPIO[5]	General Purpose IO A[5]	I/O	14	H4
		0001	CS0	DSPI1	DSPI 1 Peripheral Chip Select 0	I/O		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[70]	0001	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[178]	0001	REQ5	SIUL2	SIUL2 External Interrupt Source 5	I		
A[6]	MSCR[6]	0000 (Default)	GPIO[6]	SIUL2-GPIO[6]	General Purpose IO A[6]	I/O	2	D1
		0001	SCK	DSPI1	DSPI 1 Input/Output Serial Clock	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0011-1111	—	Reserved	—	—		
	IMCR[83]	0010	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[95]	0010	B2	FlexPWM_0	FlexPWM_0 Channel B Input 2	I		
	IMCR[47]	0001	SIN	DSPI2	DSPI 2 Serial Data Input	I		
	IMCR[185]	0001	REQ12	SIUL2	SIUL2 External Interrupt Source 12	I		
A[14]	MSCR[14]	0000 (Default)	GPIO[14]	SIUL2-GPIO[14]	General Purpose IO A[14]	I/O	143	A3
		0001	TXD	CAN1	CAN 1 Transmit Pin	O		
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[69]	0001	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I		
	IMCR[186]	0001	REQ13	SIUL2	SIUL2 External Interrupt Source 13	I		
A[15]	MSCR[15]	0000 (Default)	GPIO[15]	SIUL2-GPIO[15]	General Purpose IO A[15]	I/O	144	D3
		0001	—	Reserved	—	—		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[32]	0001	RXD	CAN0	CAN 0 Receive Pin	I		
	IMCR[33]	0001	RXD	CAN1	CAN 1 Receive Pin	I		
	IMCR[70]	0010	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[187]	0001	REQ14	SIUL2	SIUL2 External Interrupt Source 14	I		
B[0]	MSCR[16]	0000 (Default)	GPIO[16]	SIUL2-GPIO[16]	General Purpose IO B[0]	I/O	109	C16
		0001	TXD	CAN0	CAN 0 Transmit Pin	O		
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O		
		0011	DEBUG0	SSCM	SSCM Debug Output 0	O		
		0100-1111	—	Reserved	—	—		
	IMCR[67]	0001	ETC2	eTimer_1	eTimer_1 Input Data Channel 2	I		
	IMCR[188]	0001	REQ15	SIUL2	SIUL2 External Interrupt Source 15	I		
B[1]	MSCR[17]	0000 (Default)	GPIO[17]	SIUL2-GPIO[17]	General Purpose IO B[1]	I/O	110	C14
		0001	—	Reserved	—	—		
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0001	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0011	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[62]	0001	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I		
	IMCR[92]	0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I		
E[0]	MSCR[64]	0000 (Default)	GPI[64][4] ADC1_AN[5]/ ADC3_AN[4]	SIUL2-GPI[64]	General Purpose Input E[0]	I	68	T13
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[2]	MSCR[66]	0000 (Default)	GPI[66][4] ADC0_AN[5]	SIUL2-GPI[66]	General Purpose Input E[2]	I	49	U6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[4]	MSCR[68]	0000 (Default)	GPI[68][4] ADC0_AN[7]	SIUL2-GPI[68]	General Purpose Input E[4]	I	42	U4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[5]	MSCR[69]	0000 (Default)	GPI[69][4] ADC0_AN[8]	SIUL2-GPI[69]	General Purpose Input E[5]	I	44	T5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[6]	MSCR[70]	0000 (Default)	GPI[70][4] ADC0_ADC2_AN[4]	SIUL2-GPI[70]	General Purpose Input E[6]	I	46	R6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[7]	MSCR[71]	0000 (Default)	GPI[71][4] ADC0_AN[6]	SIUL2-GPI[71]	General Purpose Input E[7]	I	48	T6
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[9]	MSCR[73]	0000	GPI[73][4] ADC1_AN[7]/ ADC3_AN[6]	SIUL2-GPI[73]	General Purpose Input E[9]	I	61	U10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
I[6][5]	MSCR[134]	0000 (Default)	GPIO[134]	SIUL2-GPIO[134]	General Purpose IO I[6][11]	I/O		M15
		0001	—	Reserved	—	—		
		0010	—	Reserved	—	—		
		0011	LFAST_RXN	LFAST	SIPI/LFAST LVDS receive negative terminal	I		
		0100-1111	—	Reserved	—	—		
	IMCR[34]	0010	RXD	CAN2	CAN 2 Receive Pin	I		
I[7]	MSCR[135]	0000 (Default)	GPIO[135]	SIUL2-GPIO[135]	General Purpose IO I[7]	I/O		D2
		0001	LFAST_REF_CLK	MC_CGM	SIPI/LFAST Input/Output reference clock	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[205]	0010	SENT_RX[0]	SENT0	SENT 0 Receiver channel 0	I		
I[8]	MSCR[136]	0000 (Default)	GPIO[136]	SIUL2-GPIO[136]	General Purpose IO I[8]	I/O		K4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[213]	0010	SENT_RX[0]	SENT1	SENT 1 Receiver channel 0	I		
I[9]	MSCR[137]	0000 (Default)	GPIO[137]	SIUL2-GPIO[137]	General Purpose IO I[9]	I/O		L3
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[75]	0011	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I		
I[10]	MSCR[138]	0000 (Default)	GPIO[138]	SIUL2-GPIO[138]	General Purpose IO I[10]	I/O		M3
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[76]	0011	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I		
I[11]	MSCR[139]	0000 (Default)	GPIO[139]	SIUL2-GPIO[139]	General Purpose IO I[11]	I/O		U3
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[206]	0001	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I		
I[12]	MSCR[140]	0000 (Default)	GPIO[140]	SIUL2-GPIO[140]	General Purpose IO I[12]	I/O		P5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[214]	0001	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I		

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0010-1111	—	Reserved
SIUL	REQ25	IMCR[198]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[13]
			0010-1111	—	Reserved
SIUL	REQ26	IMCR[199]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[14]
			0010-1111	—	Reserved
SIUL	REQ27	IMCR[200]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[15]
			0010-1111	—	Reserved
SIUL	REQ28	IMCR[201]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010-1111	—	Reserved
SIUL	REQ29	IMCR[202]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[9]
			0010-1111	—	Reserved
SIUL	REQ30	IMCR[203]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[12]
			0010-1111	—	Reserved
SIUL	REQ31	IMCR[204]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[13]
			0010-1111	—	Reserved
SENT_0	SENT_RX[0]	IMCR[205]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010	I/O-Pad	I[7]
			0011	I/O-Pad	G[8]
			0100-1111	—	Reserved
SENT_0	SENT_RX[1]	IMCR[206]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[11]
			0010	I/O-Pad	J[5]
			0011	I/O-Pad	A[9]
			0100	I/O-Pad	G[10]
			0101-1111	—	Reserved
SENT_1	SENT_RX[0]	IMCR[213]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[7]
			0010	I/O-Pad	I[8]
			0011	I/O-Pad	G[9]
			0100	I/O-Pad	C[12]
			0101-1111	—	Reserved

Table continues on the next page...

Table 18. FlexRay (SYM) configuration output buffer electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
F_{max_Y}	Output frequency SYM configuration	C_L = 20 pF, $V_{DD\_HV\_IO}$=3.3 V –5%, +10%	—	—	50	MHz
T_{tr_Y}	Transition time output pin SYM configuration	C_L = 20 pF, $V_{DD\_HV\_IO}$=3.3 V –5%, +10%	1	—	6	ns
$\lvert T_{skew\_Y} \rvert$	Difference between rise and fall time	—	0	—	1	ns

1. $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 165 °C, unless otherwise specified.

NOTE

See the LFAST section for parameters dedicated to this interface.

Table 19. LFAST output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$\lvert \Delta_{VO\_L} \rvert$	Absolute value for differential output voltage swing (terminated)	—	100	200	285	mV
V_{ICOM_L}	Common mode voltage	—	1.08	1.2	1.32	V
T_{tr_L}	Transition time output pin LVDS configuration	—	0.2	—	1.5	ns

1. $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 165 °C, unless otherwise specified.

NOTE

Fast IOs must be specified only as fast (and not as high current). See Table 20.

Table 20. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DD_LV}	LV (core) Supply Voltage	—	1.19	—	1.32	V
$V_{DD\_HV\_IO}$[1]	I/O Supply Voltage	—	3.15	—	3.6	V
V_{IH}	CMOS Input Buffer High Voltage (with hysteresis disabled)	—	0.55 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	—	Vss - 0.3	—	0.40 * $V_{DD\_HV\_IO}$	V
V_{HYS}	CMOS Input Buffer Hysteresis	—	0.1 * $V_{DD\_HV\_IO}$	—	—	V
Pull_I_{OH}	Weak Pullup Current[2]	—	10	—	80	µA
Pull_I_{OL}	Weak Pulldown Current[3]	—	10	—	80	µA

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Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		Frequency: 200MHz				
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	1.8	
$I_{DD\_HV\_FLA}$	Operating current	T_J = 150 °C 3.3 V supplies Frequency: 200MHz	—	—	5.5	mA
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	7.0	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Enabled modules: ADC0/1, FlexPWM0, eTimer0, two SPIs, two FlexCANs, FlexRay, one LINFlexD, DMA. At maximum frequency. I/O supply current excluded.
3. Internal structures hold the input voltage less than $V_{DD\_HV\_ADV}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
4. This value is the total current for two ADCs.

3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 22. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range	—	–40	—	165	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy for linear temperature sensor	T_J = –40 to 150 °C	–3	—	+3	°C
		T_J = 150 to 165 °C	–5	—	+5	
—	Accuracy for temperature-threshold digital flags	T_J = –40 to 150 °C	–5	—	+5	°C
—	Temperature variation for each customer-adjustable trim step	T_J = –40 to 150 °C	0.4	0.7	1.0	°C
—	Operating current	T_J = –40 to 165 °C	—	—	675	µA

3.12 Main oscillator electrical characteristics

This device provides a driver for the oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing EMI and power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between the crystal and the MCU.

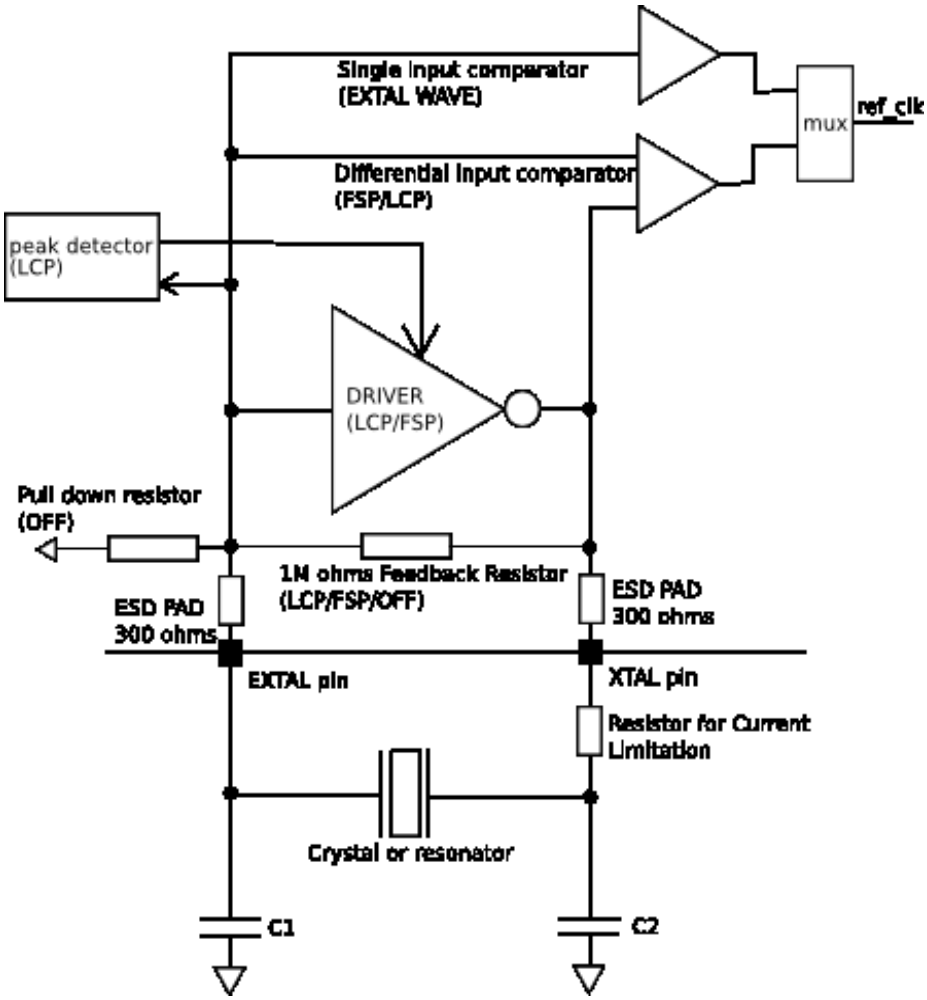


Figure 5. Oscillator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions[1]	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP	—	4[2]	—	40	MHz
$g_{mXOSCHS}$	Driver transconductance	LCP	$V_{DD\_HV\_OSC}$ = 3.3V	—	20	—	mA/V
		FSP	–5%, +10%	—	30	—	
V_{XOSCHS}	Oscillation amplitude	LCP	f_{OSC} = 4, 8, 16 MHz	1.1	1.3	2.6	V
			f_{OSC} = 40 MHz	1.2	1.5	1.7	V
$T_{XOSCHSSU}$	Oscillator startup time	FSP/LCP[3]	f_{OSC} = 4 MHz	1.75	2.5	2.9	ms
			f_{OSC} = 8, 16, 40 MHz	0.25	0.5	1.1	ms

Table continues on the next page...

3.16.1.2 Flash memory Array Integrity and Margin Read specifications

Table 29. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.1.3 Flash memory module life specifications

Table 30. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

Table 32. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Units
			Initial Max	Initial Max Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C≤ T_A ≤ 30°C[4]	–40°C≤ T_J ≤ 150°C[4]	–40°C≤ T_J ≤ 165 °C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	65	650		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	145	650		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	540	2,700		µs
t_{16kers}	16 KB Block erase time	168	290	320	500	9,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	70	1,400		ms
t_{32kers}	32 KB Block erase time	217	360	390	610	9,000		ms
t_{32kpgm}	32 KB Block program time	69	100	110	140	2,800		ms
t_{64kers}	64 KB Block erase time	315	490	590	820	9,000		ms
t_{64kpgm}	64 KB Block program time	138	180	210	280	5,500		ms
$t_{256kers}$	256 KB Code erase time[7]	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Code program time[7]	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: –40°C ≤ T_J ≤ 165°C; full spec voltage. 16 KB, 32 KB and 64 KB blocks are allowed to be programmed or erased up to T_J = 165°C with restrictions.
7. 256 KB blocks may be programmed or erased at T_J = 150°C maximum. Times listed on this row are T_J = 150°C times.

3.16.2.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 x Tperiod x Nread	—

Table continues on the next page...

Table 35. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UTO-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UTO-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.16.3 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

NOTE

If the user does not follow these recommended settings, the user must run the flash memory's array integrity (AI) check with breakpoints disabled: Set the Array Integrity Break Point Enable bit in the C55FMC's UTest 0 register (C55FMC_UT0[AIBPE]) to 0.

Table 36. Flash memory read wait-state and address-pipeline control combinations

Operating frequency (f_{CPU} = SYS_CLK)		RWSC	APC	Flash read latency on mini-cache miss (# of f_{CPU} clock periods)	Flash read latency on mini-cache hit (# of f_{CPU} clock periods)
–40°C to 150°C	Max 165°C option				
0 MHz < f_{CPU} ≤ 33 MHz	0 MHz < f_{CPU} ≤ 30 MHz	0	0	3	1
33 MHz < f_{CPU} ≤ 100 MHz	30 MHz < f_{CPU} ≤ 90 MHz	2	1	5	1
100 MHz < f_{CPU} ≤ 133 MHz	90 MHz < f_{CPU} ≤ 120 MHz	3	1	6	1

Table continues on the next page...

3.18 RESET sequence duration

This following table shows the duration of different reset sequences. See the chip's Reference Manual for details about the reset sequences.

Table 38. RESET sequences

Symbol	Parameter	Conditions	T_{Reset}			Unit
			Min	Typ	Max[1]	
T_{DRB}	'Destructive' reset sequence, BIST enabled	Self test clock in STCU is the PLL generated clock. Self test configuration as per DCF record programming. For four LBIST partitions in design, two LBIST partitions are run in parallel.	—	—	18.0	ms
T_{DR}	'Destructive' reset sequence, BIST disabled	—	—	440	480	µs
T_{ERLB}	External reset sequence—long, BIST enabled	Self test clock in STCU is the PLL generated clock. Self test configuration as per DCF record programming. For four LBIST partitions in design, two LBIST partitions are run in parallel.	—	—	17.5	ms
T_{ERL}	External reset sequence—long, BIST disabled	—	—	120	150	µs
T_{FRL}	Functional reset sequence—long	—	—	165	180	µs
T_{FRS}	Functional reset sequence—short	—	—	10.0	12.0	µs

1. The maximum value applies only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

3.19 AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +165°C and for the full operating range of the V_{DD_IO} supply defined in DC electrical characteristics.

Table 39. Functional Pad AC Specifications

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn's SRC[1:0] field
	Min	Max	Min	Max		MSB,LSB
I/O (output)	2.5/2.5	7.5/7.5	0.9/0.9	3/3	50	11
	—	—	—	12/12	200	

Table continues on the next page...

Table 39. Functional Pad AC Specifications (continued)

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn's SRC[1:0] field
	Min	Max	Min	Max		MSB,LSB
	—	8/8	—	3.5/3.5	25	10
	—	11.5/11.5	—	6.5/6.5	50	
	—	—	—	30/30	200	
	—	45/45	—	25/25	50	01
	—	65/65	—	30/30	200	
	—	75/75	—	40/40	50	00[2]
	—	110/110	—	50/50	200	
I/O (input)	—	1.5/1.5	—	0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

3.19.1 Reset pad (EXT_POR, RESET) electrical characteristics

The device implements a dedicated bidirectional RESET pin.

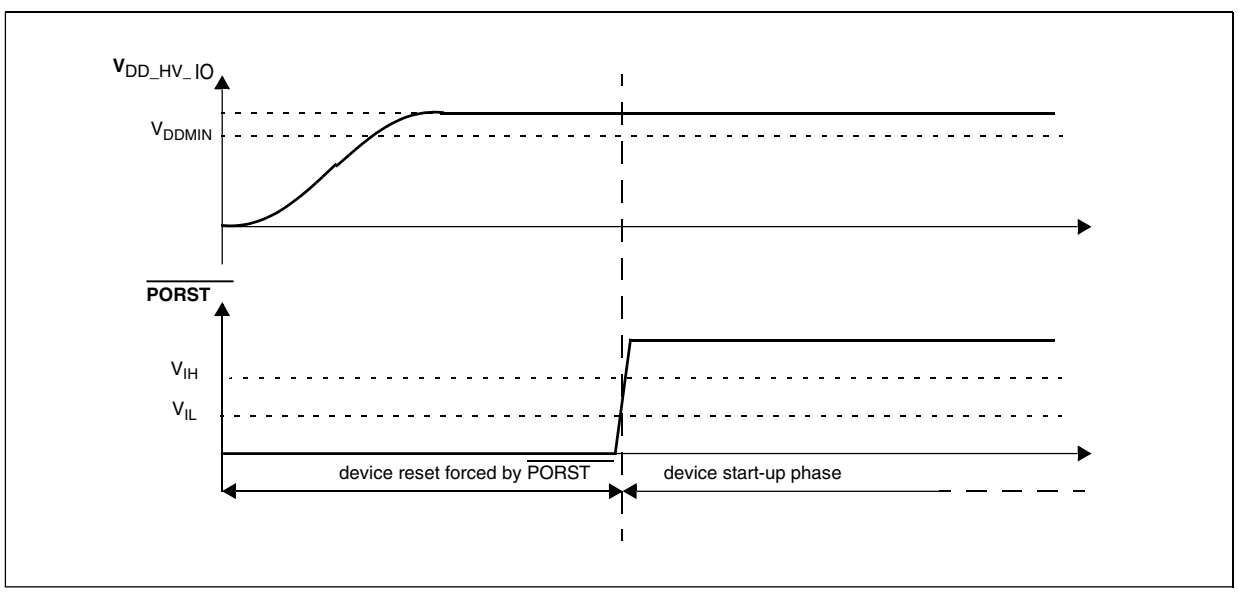


Figure 9. Start-up reset requirements

Maximum junction temperature 165°C

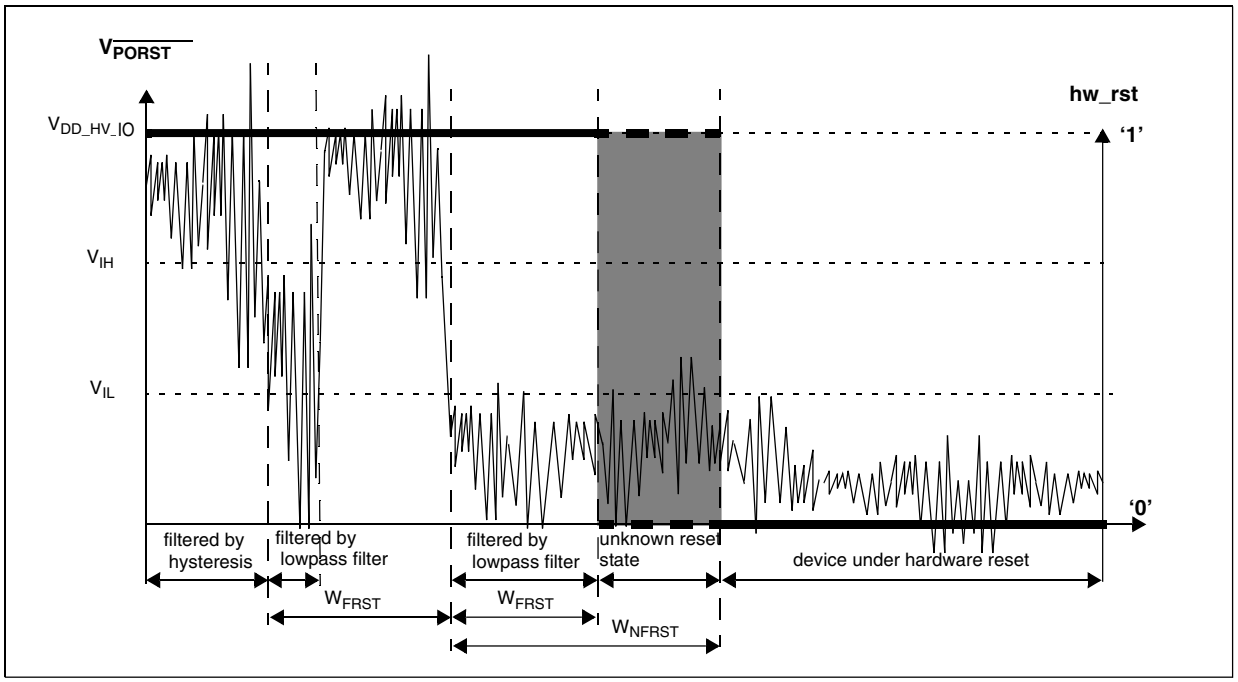


Figure 10. Noise filtering on reset signal

Table 40. Reset ($\overline{RESET}$) electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_IO}$ + 0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DD\_HV\_A}$=1.0 V V_{OL} = 0.35*$V_{DD\_HV\_IO}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_IO}$=3.0 V V_{OL} = 0.35*$V_{DD\_HV\_IO}$	15	—	—	mA
W_{FRST}	($\overline{RESET}$)-input filtered pulse	—	—	—	500	ns
W_{NFRST}	($\overline{RESET}$)-input not filtered pulse	—	2	—	—	µs
$\lvert I_{WPD} \rvert$	Weak pull-down current absolute value	RESET pin V_{IN} = V_{DD}	30	—	80	µA

Maximum junction temperature 165°C

1. These specifications apply to JTAG boundary scan only.

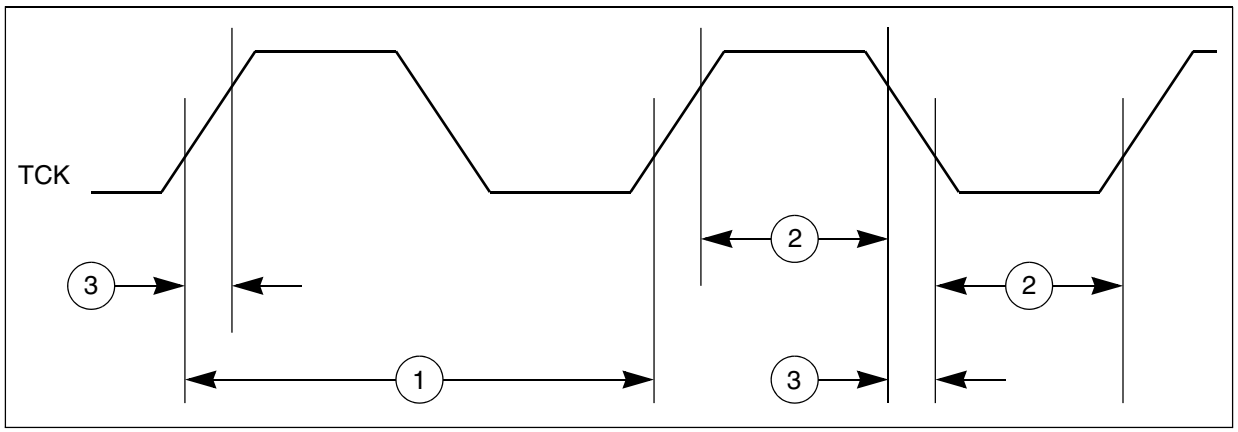


Figure 11. JTAG test clock input timing

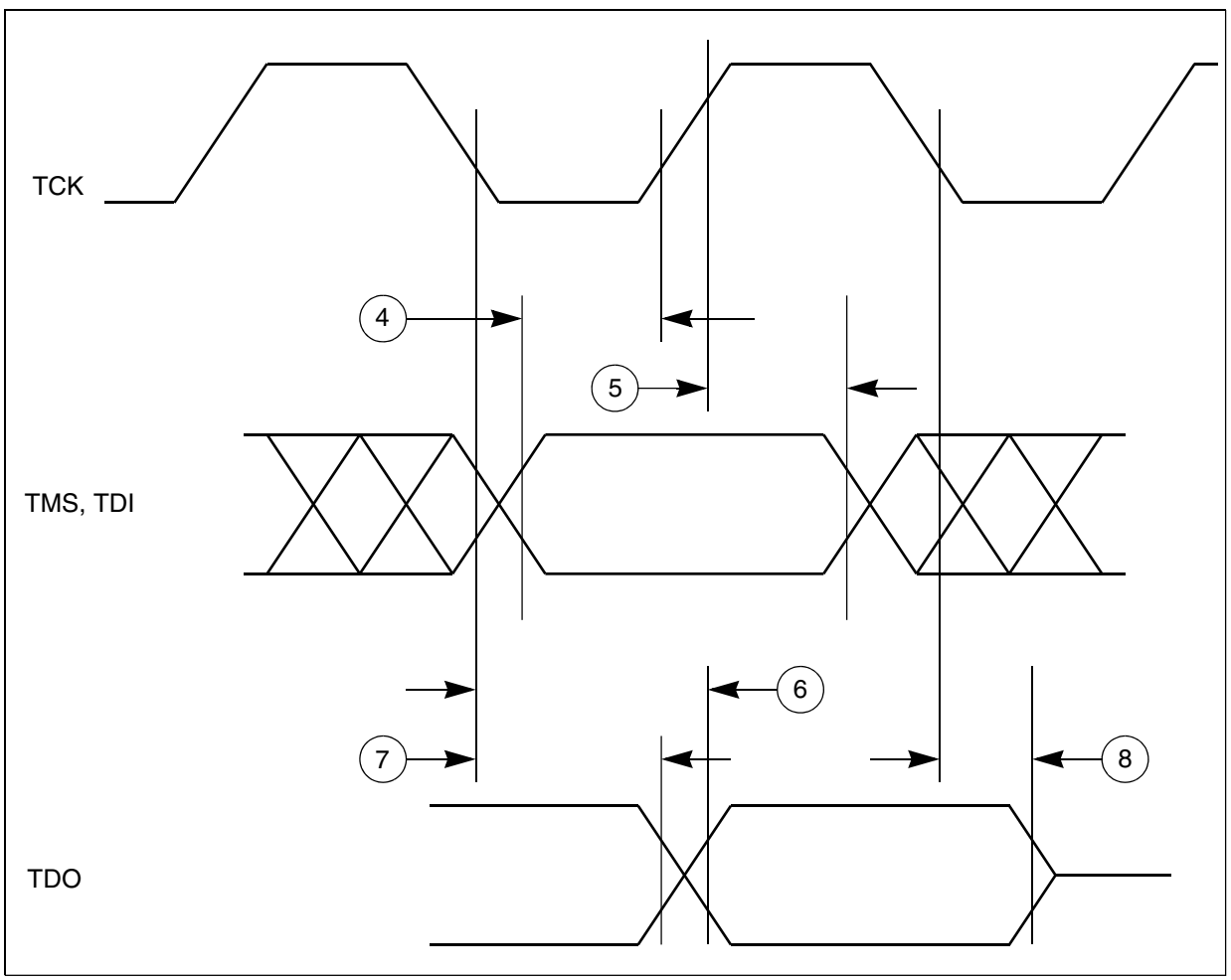


Figure 12. JTAG test access port timing

3.19.6.1 LFAST interface timing diagrams

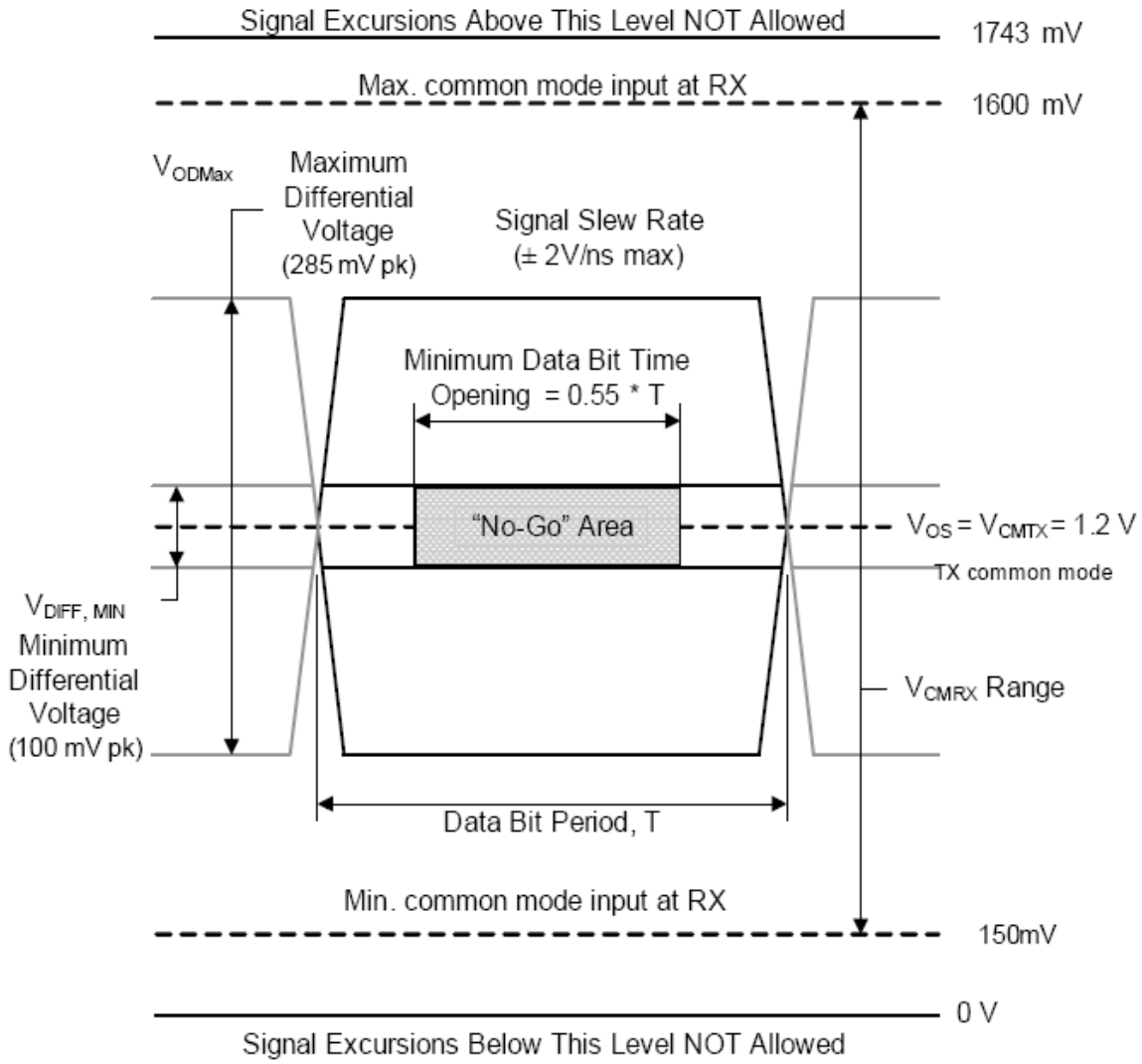


Figure 30. LFAST timing definition

Table 51. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C, TxEN pin load maximum 25 pF

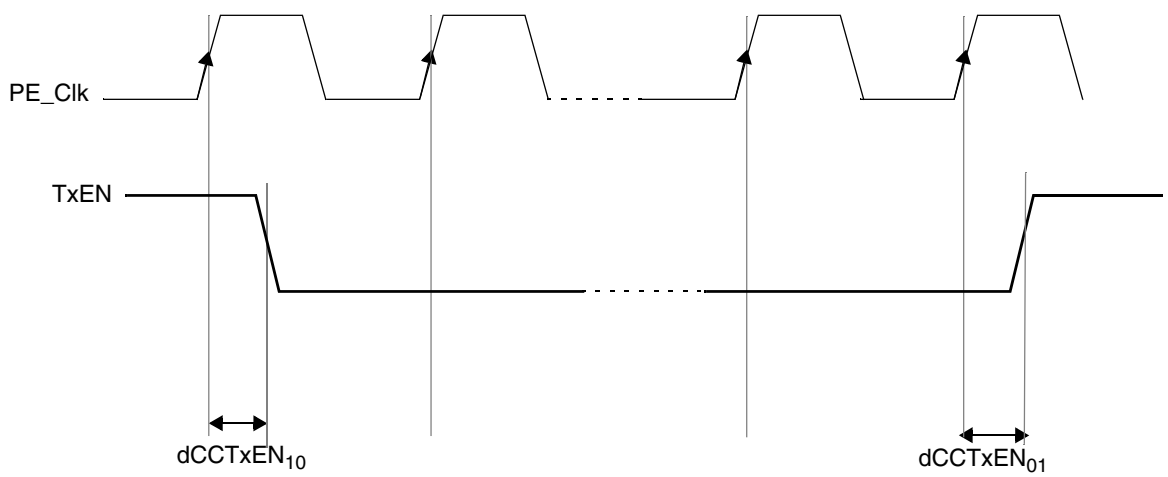
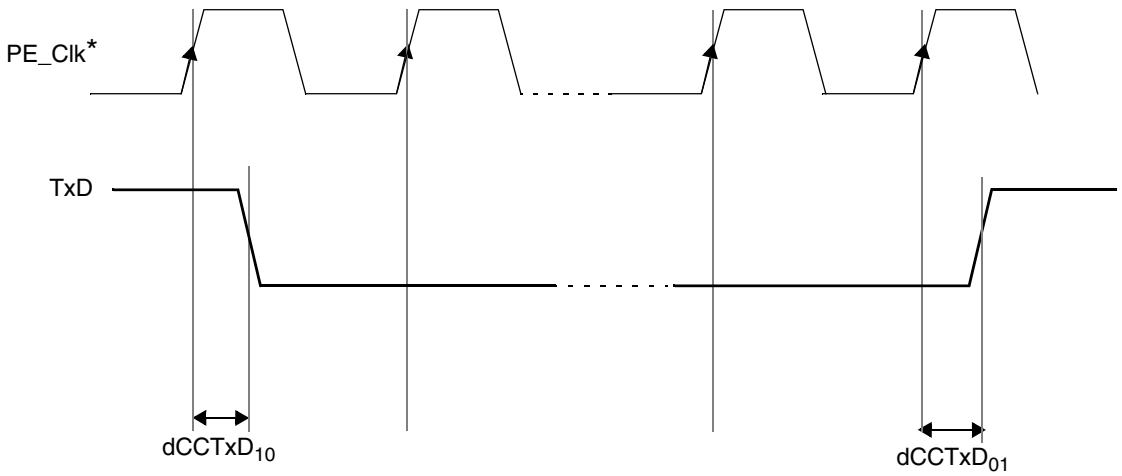


Figure 34. FlexRay TxEN signal propagation delays



*FlexRay Protocol Engine Clock

Figure 36. FlexRay TxD signal propagation delays

3.19.7.4 RxD

Table 53. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 / 165 °C

3.19.7.5 Receiver asymmetry

Table 54. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	–31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	–30.5	+43.0	ns