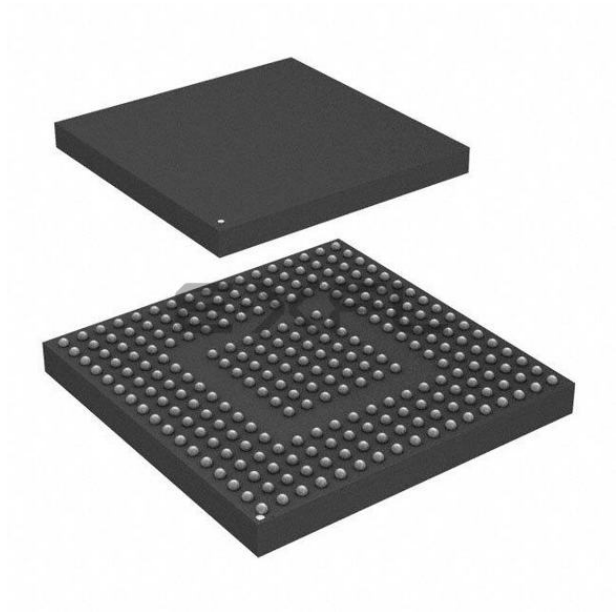

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	-
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pfk1ammm8

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[49]	0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I		
	IMCR[98]	0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I		
A[4]	MSCR[4]	0000 (Default)	GPIO[4]	SIUL2-GPIO[4]	General Purpose IO A[4]	I/O	108	D16
		0001	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0010	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0011	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0100	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[112]	0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I		
	IMCR[177]	0001	REQ4	SIUL2	SIUL2 External Interrupt Source 4	I		
	IMCR[172]	0000 (Default)	FAB	MC_RGM	RGM Force Alternate Boot Mode	I		
	IMCR[65]	0001	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I		
	IMCR[63]	0011	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
A[5]	MSCR[5]	0000 (Default)	GPIO[5]	SIUL2-GPIO[5]	General Purpose IO A[5]	I/O	14	H4
		0001	CS0	DSPI1	DSPI 1 Peripheral Chip Select 0	I/O		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[70]	0001	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[178]	0001	REQ5	SIUL2	SIUL2 External Interrupt Source 5	I		
A[6]	MSCR[6]	0000 (Default)	GPIO[6]	SIUL2-GPIO[6]	General Purpose IO A[6]	I/O	2	D1
		0001	SCK	DSPI1	DSPI 1 Input/Output Serial Clock	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[73]	0001	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I		
	IMCR[179]	0001	REQ6	SIUL2	SIUL2 External Interrupt Source 6	I		
A[7]	MSCR[7]	0000 (Default)	GPIO[7]	SIUL2-GPIO[7]	General Purpose IO A[7]	I/O	10	G4
		0001	SOUT	DSPI1	DSPI 1 Serial Data Out	O		
		0010	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[74]	0001	ETC3	eTimer_2	eTimer_2 Input Data Channel 3	I		
	IMCR[180]	0001	REQ7	SIUL2	SIUL2 External Interrupt Source 7	I		
A[8]	MSCR[8]	0000 (Default)	GPIO[8]	SIUL2-GPIO[8]	General Purpose IO A[8]	I/O	12	H1
		0001	—	Reserved	—	—		
		0010	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[44]	0001	SIN	DSPI1	DSPI 1 Serial Data Input	I		
	IMCR[75]	0001	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I		
	IMCR[181]	0001	REQ8	SIUL2	SIUL2 External Interrupt Source 8	I		
A[9]	MSCR[9]	0000 (Default)	GPIO[9]	SIUL2-GPIO[9]	General Purpose IO A[9]	I/O	134	A4
		0001	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0010	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[76]	0001	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I		
	IMCR[98]	0010	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
	IMCR[83]	0001	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[206]	0011	SENT_RX[1]	SENT_0	SENT 0 Receiver channel 1	I		
A[10]	MSCR[10]	0000 (Default)	GPIO[10]	SIUL2-GPIO[10]	General Purpose IO A[10]	I/O	118	B11
		0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	O		
		0010	B0	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 0	I/O		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[63]	0001	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
	IMCR[192]	0001	REQ19	SIUL2	SIUL2 External Interrupt Source 19	I		
B[15]	MSCR[31]	0000 (Default)	GPI[31][4] ADC1_AN[2]	SIUL2-GPI[31]	General Purpose Input B[15]	I	62	R11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[193]	0001	REQ20	SIUL2	SIUL2 External Interrupt Source 20	I		
C[0]	MSCR[32]	0000 (Default)	GPI[32][4] ADC1_AN[3]	SIUL2-GPI[32]	General Purpose Input C[0]	I	66	R12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[1]	MSCR[33]	0000 (Default)	GPI[33][4] ADC0_AN[2]	SIUL2-GPI[33]	General Purpose Input C[1]	I	41	T4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[2]	MSCR[34]	0000 (Default)	GPI[34][4] ADC0_AN[3]	SIUL2-GPI[34]	General Purpose Input C[2]	I	45	U5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[4]	MSCR[36]	0000 (Default)	GPIO[36]	SIUL2-GPIO[36]	General Purpose IO C[4]	I/O	11	H3
		0001	CS0	DSPI0	DSPI 0 Peripheral Chip Select 0	I/O		
		0010	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0011	DEBUG4	SSCM	SSCM Debug Output 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[93]	0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input 1	I		
	IMCR[195]	0001	REQ22	SIUL2	SIUL2 External Interrupt Source 22	I		
C[5]	MSCR[37]	0000 (Default)	GPIO[37]	SIUL2-GPIO[37]	General Purpose IO C[5]	I/O	13	G3
		0001	SCK	DSPI0	DSPI 0 Input/Output Serial Clock	I/O		
		0010	—	Reserved	—	—		
		0011	DEBUG5	SSCM	SSCM Debug Output 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0001	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[196]	0001	REQ23	SIUL2	SIUL2 External Interrupt Source 23	I		
C[6]	MSCR[38]	0000 (Default)	GPIO[38]	SIUL2-GPIO[38]	General Purpose IO C[6]	I/O	142	D4
		0001	SOUT	DSPI0	DSPI 0 Serial Data Out	O		
		0010	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0011	DEBUG6	SSCM	SSCM Debug Output 6	O		
		0100-1111	—	Reserved	—	—		
	IMCR[92]	0001	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I		
	IMCR[197]	0001	REQ24	SIUL2	SIUL2 External Interrupt Source 24	I		
C[7]	MSCR[39]	0000 (Default)	GPIO[39]	SIUL2-GPIO[39]	General Purpose IO C[7]	I/O	15	J1
		0001	—	Reserved	—	—		
		0010	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0011	DEBUG7	SSCM	SSCM Debug Output 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[41]	0001	SIN	DSPI0	DSPI 0 Serial Data Input	I		
	IMCR[91]	0001	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I		
C[10]	MSCR[42]	0000 (Default)	GPIO[42]	SIUL2-GPIO[42]	General Purpose IO C[10]	I/O	111	B14
		0001	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O		
		0010	—	Reserved	—	—		
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[84]	0001	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I		
	IMCR[97]	0010	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I		
C[11]	MSCR[43]	0000 (Default)	GPIO[43]	SIUL2-GPIO[43]	General Purpose IO C[11]	I/O	80	P16
		0001	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0010	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O		
		0011	TX_ER	ENET_0	Ethernet transmit Data Error	O		
		0100	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0101-1111	—	Reserved	—	—		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[199]	0001	REQ26	SIUL2	SIUL2 External Interrupt Source 26	I		
E[15]	MSCR[79]	0000 (Default)	GPIO[79]	SIUL2-GPIO[79]	General Purpose IO E[15]	I/O	121	C8
		0001	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O		
		0010	—	Reserved	—	—		
		0011	TIMER1	ENET_0	Ethernet TIMER Outputs (Output Compare Events)	O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0100	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[200]	0001	REQ27	SIUL2	SIUL2 External Interrupt Source 27	I		
F[0]	MSCR[80]	0000 (Default)	GPIO[80]	SIUL2-GPIO[80]	General Purpose IO F[0]	I/O	133	B6
		0001	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0010	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	O		
		0011	MDC	ENET_0	Ethernet MDIO clock output	O		
		0100-1111	—	Reserved	—	—		
	IMCR[61]	0001	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I		
	IMCR[91]	0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I		
	IMCR[201]	0001	REQ28	SIUL2	SIUL2 External Interrupt Source 28	I		
F[3]	MSCR[83]	0000 (Default)	GPIO[83]	SIUL2-GPIO[83]	General Purpose IO F[3]	I/O	139	B3
		0001	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O		
		0010	—	Reserved	—	—		
		0011	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0100	TIMER2	ENET_0	Ethernet TIMER Outputs 2 (Output Compare Events)	O		
		0101-1111	—	Reserved	—	—		
F[4]	MSCR[84]	0000 (Default)	GPIO[84]	SIUL2-GPIO[84]	General Purpose IO F[4]	I/O	4	E1
		0001	—	Reserved	—	O		
		0010	MDO[3]	NPC_WRAPPER	Nexus - Message Data Out Pin 3	O		
		0011	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[2]	MSCR[98]	0000 (Default)	GPIO[98]	SIUL2-GPIO[98]	General Purpose IO G[2]	I/O	102	F17
		0001	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 2	I/O		
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O		
		0011-1111	—	Reserved	—	—		
	IMCR[96]	0010	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input 2	I		
G[3]	MSCR[99]	0000 (Default)	GPIO[99]	SIUL2-GPIO[99]	General Purpose IO G[3]	I/O	104	E16
		0001	A2	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[63]	0010	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
	IMCR[94]	0011	A2	FlexPWM_0	FlexPWM_0 Channel A Input 2	I		
G[4]	MSCR[100]	0000 (Default)	GPIO[100]	SIUL2-GPIO[100]	General Purpose IO G[4]	I/O	100	F16
		0001	B2	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[64]	0010	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I		
	IMCR[95]	0011	B2	FlexPWM_0	FlexPWM_0 Channel B Input 2	I		
G[5]	MSCR[101]	0000 (Default)	GPIO[101]	SIUL2-GPIO[101]	General Purpose IO G[5]	I/O	85	M17
		0001	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	TX_EN	ENET_0	Ethernet Transmit Data Valid	O		
		0100-1111	—	Reserved	—	—		
	IMCR[99]	0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input 3	I		
G[6]	MSCR[102]	0000 (Default)	GPIO[102]	SIUL2-GPIO[102]	General Purpose IO G[6]	I/O	98	G17
		0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[97]	0100	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I		
G[7][5]	MSCR[103]	0000 (Default)	GPIO[103]	SIUL2-GPIO[103]	General Purpose IO G[7][9]	I/O	83	M16
		0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
I[6][5]	MSCR[134]	0000 (Default)	GPIO[134]	SIUL2-GPIO[134]	General Purpose IO I[6][11]	I/O		M15
		0001	—	Reserved	—	—		
		0010	—	Reserved	—	—		
		0011	LFAST_RXN	LFAST	SIPI/LFAST LVDS receive negative terminal	I		
		0100-1111	—	Reserved	—	—		
	IMCR[34]	0010	RXD	CAN2	CAN 2 Receive Pin	I		
I[7]	MSCR[135]	0000 (Default)	GPIO[135]	SIUL2-GPIO[135]	General Purpose IO I[7]	I/O		D2
		0001	LFAST_REF_CLK	MC_CGM	SIPI/LFAST Input/Output reference clock	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[205]	0010	SENT_RX[0]	SENT0	SENT 0 Receiver channel 0	I		
I[8]	MSCR[136]	0000 (Default)	GPIO[136]	SIUL2-GPIO[136]	General Purpose IO I[8]	I/O		K4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[213]	0010	SENT_RX[0]	SENT1	SENT 1 Receiver channel 0	I		
I[9]	MSCR[137]	0000 (Default)	GPIO[137]	SIUL2-GPIO[137]	General Purpose IO I[9]	I/O		L3
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[75]	0011	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I		
I[10]	MSCR[138]	0000 (Default)	GPIO[138]	SIUL2-GPIO[138]	General Purpose IO I[10]	I/O		M3
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[76]	0011	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I		
I[11]	MSCR[139]	0000 (Default)	GPIO[139]	SIUL2-GPIO[139]	General Purpose IO I[11]	I/O		U3
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[206]	0001	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I		
I[12]	MSCR[140]	0000 (Default)	GPIO[140]	SIUL2-GPIO[140]	General Purpose IO I[12]	I/O		P5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[214]	0001	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[39]	0001	EXT_IN	CTU_1	CTU 1 External Trigger Input	I		
J[5]	MSCR[149]	0000 (Default)	GPI[149][4] ADC2_ADC3_AN[0]	SIUL2-GPI[149]	General Purpose Input J[5]	I		P8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[206]	0010	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I		
J[6]	MSCR[150]	0000 (Default)	GPI[150][4] ADC2_ADC3_AN[1]	SIUL2-GPI[150]	General Purpose Input J[6]	I		P9
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[214]	0010	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I		
J[7]	MSCR[151]	0000 (Default)	GPI[151][4] ADC2_ADC3_AN[2]	SIUL2-GPI[151]	General Purpose Input J[7]	I		P10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
J[8]	MSCR[152]	0000 (Default)	GPIO[152]	SIUL2-GPIO[152]	General Purpose IO J[8]	I/O	95	G16
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[34]	0011	RXD	CAN2	CAN 2 Receive Pin	I		
	IMCR[73]	0100	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I		
	IMCR[75]	0100	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I		
J[9]	MSCR[153]	0000 (Default)	GPIO[153]	SIUL2-GPIO[153]	General Purpose IO J[9]	I/O	16	K1
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0010	NEX_RDY_B	NPC	Nexus data ready for transfer (RDY_B)	O		
		0011-1111	—	Reserved	—	—		
	IMCR[39]	0010	EXT_IN	CTU_1	CTU_1 External Trigger Input	I		
	IMCR[76]	0100	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I		
	IMCR[229]	0001	RX_D3	ENET_0	Ethernet MII Receive Data 3	I		
NMI_B	MSCR[154]	0000 (Default)	NMI_B	Core	Non-Maskable Interrupt	I	1	E4

1. Selecting an alternative function with a "Reserved" source function causes the pin to enter a null state (input buffer and output buffer enables are both 0).

2. **(Default) = ALT mode configuration after reset.**
3. Changing the B[5] configuration during debug might affect the availability of TDI.
4. ADC analog input: Program corresponding MSCR APC bit and enable ADC to switch on the analog input path.
5. When the LFAST interface is selected the other functionality of the MSCR register is not available.
6. Shared with SIPI LFAST transmit pad SIPI_TXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
7. To operate D[7] as GPIO, disable the Sine Wave Generator (SGEN) and the peripheral bus clock of the SGEN: Program the MC_ME_PCTL239 register to select an MC_ME_RUN_PCn (or MC_ME_LP_PCn) configuration where the field for the desired mode is 0.
8. SGEN output if SGEN is enabled.
9. Shared with SIPI LFAST receive pad SIPI_RXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
10. Shared with SIPI LFAST receive pad SIPI_TXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
11. Shared with SIPI LFAST receive pad SIPI_RXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.

The following table list ports that are not implemented. The corresponding control and data registers are not implemented.

Table 9. Ports - Not Implemented

Port Name	Port Index
C	3,8,9
D	13,15
E	1,3,8
F	1,2
G	0,1,[12:15]
H	[0:3]
J	[10:15]

Any attempt to access unimplemented MSCRs generates a bus error. The read value from unimplemented ports must be masked in case of parallel port accesses.

2.2.6 Peripheral input muxing

The following table describes the peripheral muxing capabilities of the device.

Table 10. Peripheral muxing

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
FlexCAN_0	RXD	IMCR[32]	0000 (Default)[1]	—	Disable
			0001	I/O-Pad	A[15]
			0010	I/O-Pad	B[1]
			0011-1111	—	Reserved[2]
FlexCAN_1	RXD	IMCR[33]	0000 (Default)	—	Disable

Table continues on the next page...

Table 11. Peripheral muxing example

SSS field value in IMCR[214]	Result
0001	I/O-Pad I[12] is connected to SENT_1 Receive input SENT_RX[1]
0010	I/O-Pad J[6] is connected to SENT_1 Receive input SENT_RX[1]

See Table 9 concerning the availability of port pins on the packages.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 200 MHz.

3.2 165°C junction temperature option

For orderable parts whose device marking shows they support this extended temperature option:

- Operation at 150°C < T_J < 165°C is allowed for a maximum cumulative time of 200 hours over the device lifetime.
- Production parameters at 165°C reflect testing over an ambient temperature range of –40°C to 150°C with appropriate guardbanding to guarantee operation at 165°C.

3.3 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

5. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
6. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
7. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

3.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

Table 15. ESD ratings

No.	Symbol	Parameter	Conditions[1]	Class	Max value	Unit
1	$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator (external NPN to support core current)
- Low voltage detector (LVD_IO) for 3.3 V supply to IO ($V_{DD\_HV\_IO}$)
- Low voltage detector (LVD_PMC) for 3.3 V supply ($V_{DD\_HV\_PMU}$)
- Low voltage detector (LVD_FLASH) for 3.3 V flash memory supply ($V_{DD\_HV\_FLA}$)
- Low voltage detector (LVD_ADC) for 3.3 V ADC supply ($V_{DD\_HV\_ADV}$)
- Low voltage detector (LVD_OSC) for 3.3 V OSC supply ($V_{DD\_HV\_OSC}$)
- Low voltage detector (LVD_CORE) for 1.25 V digital core supply (V_{DD_LV})
- Low voltage detector (LVD_CORE_BK) for the self-test of LVD_CORE
- High voltage detector (HVD_CORE) for 1.25 V digital core supply (V_{DD_LV})

- High voltage detector (HVD_CORE_BK) for the self-test of HVD_CORE
- Power on Reset (POR)

NOTE

When the external regulator mode is used either the EXT_POR_B signal needs to be driven by external circuitry until all power supplies are in recommended ranges or the internal LVDs keep the device in POR until all power supply are in recommended range. There needs to be used the external over voltage detectors for all power supplies in both regulator modes for safety operation.

The following bipolar transistor is supported:

- ON Semiconductor™ NJD2873 (requires a heat sink to operate up to 165 °C): See Table 16.

Table 16. Recommended operating characteristics: NJD2873

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Minimum peak collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_c	Minimum voltage at transistor collector	2.5	V

Table 17. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ld}	External decoupling / stability capacitor	Min value granted with respect to tolerance, voltage, temperature, and aging variations. 4 capacitors are recommended – one for each side of the chip.	4	—	18.8	µF
—	Combined ESR of external capacitor	—	0.03	—	0.15	Ω
t_{SU}	Start-up time after main supply stabilization	C_{ld} = 4 µF	—	—	2.5	ms
L_{bw}	Bonding inductance	—	—	—	13	nH
R_{bw}	Bonding wire and pad resistance	—	—	—	0.5	Ω
R_{sd}	Series resistance of on-chip power grid	—	—	—	0.1	Ω

Table continues on the next page...

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		Frequency: 200MHz				
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	1.8	
$I_{DD\_HV\_FLA}$	Operating current	T_J = 150 °C 3.3 V supplies Frequency: 200MHz	—	—	5.5	mA
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	7.0	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Enabled modules: ADC0/1, FlexPWM0, eTimer0, two SPIs, two FlexCANs, FlexRay, one LINFlexD, DMA. At maximum frequency. I/O supply current excluded.
3. Internal structures hold the input voltage less than $V_{DD\_HV\_ADV}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
4. This value is the total current for two ADCs.

3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 22. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range	—	–40	—	165	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy for linear temperature sensor	T_J = –40 to 150 °C	–3	—	+3	°C
		T_J = 150 to 165 °C	–5	—	+5	
—	Accuracy for temperature-threshold digital flags	T_J = –40 to 150 °C	–5	—	+5	°C
—	Temperature variation for each customer-adjustable trim step	T_J = –40 to 150 °C	0.4	0.7	1.0	°C
—	Operating current	T_J = –40 to 165 °C	—	—	675	µA

3.12 Main oscillator electrical characteristics

This device provides a driver for the oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing EMI and power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between the crystal and the MCU.

3.15.1 Input equivalent circuit and ADC conversion characteristics

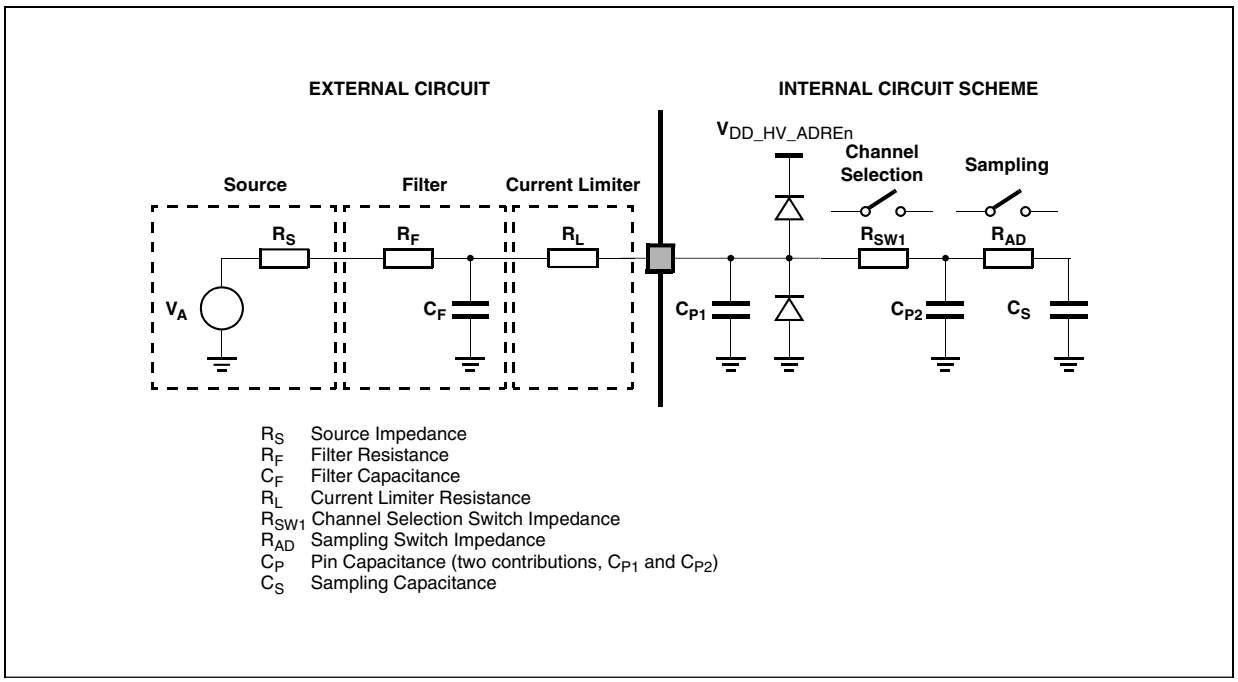


Figure 8. Input equivalent circuit

NOTE

Unless noted otherwise, the specifications in Table 27 assume the use of 12-bit resolution (high accuracy, recommended): In ADC_CALBISTREG, set OPMODE to 110b.

Table 27. ADC conversion characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	20	—	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz, 12-bit resolution	250	—	—	ns
		80 MHz, 12-bit resolution (high accuracy, recommended)	250	—	—	
t_{conv}	Conversion time[4]	80 MHz, 12-bit resolution	650	—	—	ns
		80 MHz, 12-bit resolution (high accuracy, recommended)	700	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5[6]	pF

Table continues on the next page...

Table 39. Functional Pad AC Specifications (continued)

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn's SRC[1:0] field
	Min	Max	Min	Max		MSB,LSB
	—	8/8	—	3.5/3.5	25	10
	—	11.5/11.5	—	6.5/6.5	50	
	—	—	—	30/30	200	
	—	45/45	—	25/25	50	01
	—	65/65	—	30/30	200	
	—	75/75	—	40/40	50	00[2]
	—	110/110	—	50/50	200	
I/O (input)	—	1.5/1.5	—	0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

3.19.1 Reset pad (EXT_POR, RESET) electrical characteristics

The device implements a dedicated bidirectional RESET pin.

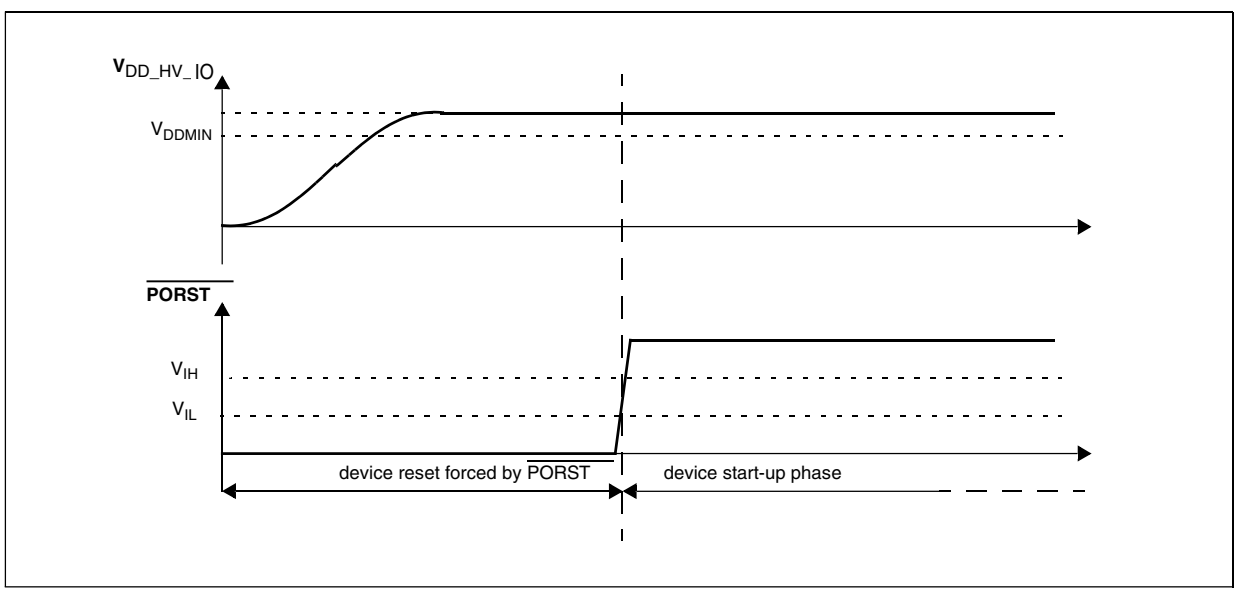


Figure 9. Start-up reset requirements

3.19.6.1 LFAST interface timing diagrams

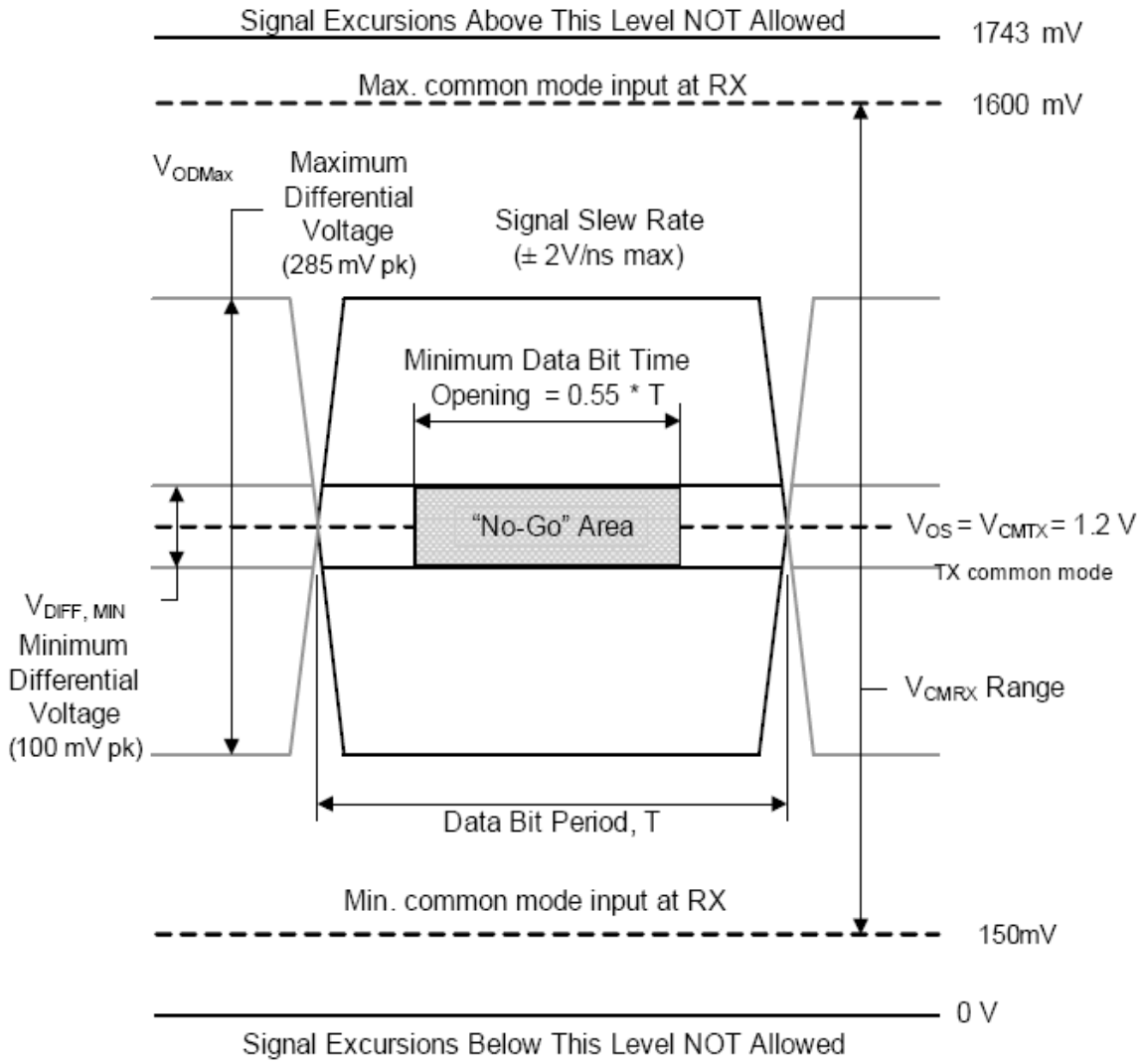


Figure 30. LFAST timing definition

Table 50. LFAST electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
F_{VCO}	PLL VCO Frequency	—	—	320	—	MHz
T_{LOCK}	PLL Phase Lock	—	—	—	40	µs
ΔPER	PLL Long Term Jitter (peak to peak)	—	—	—	600	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.

3.19.7 FlexRay

3.19.7.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

3.19.7.2 TxEN

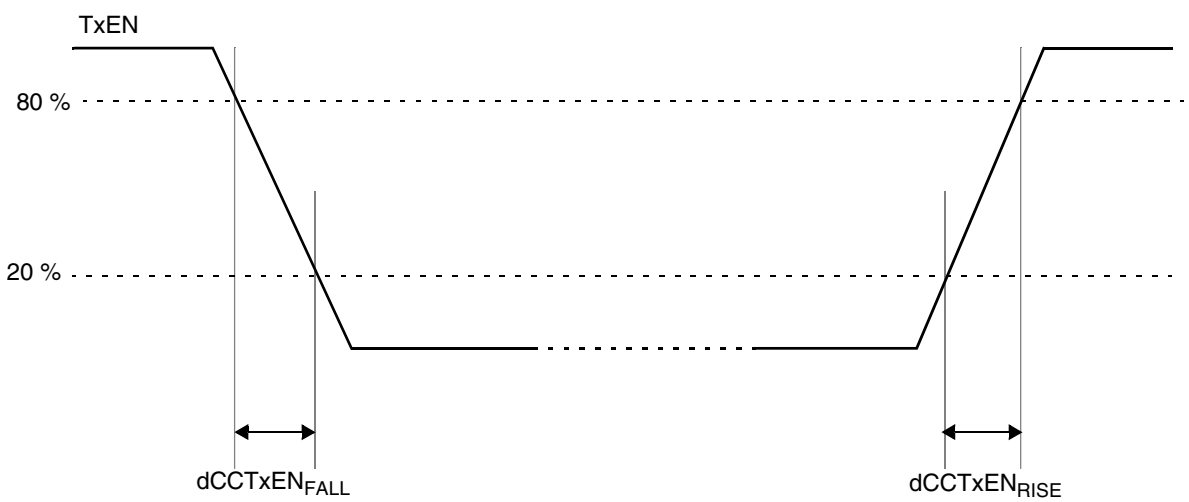


Figure 33. FlexRay TxEN signal

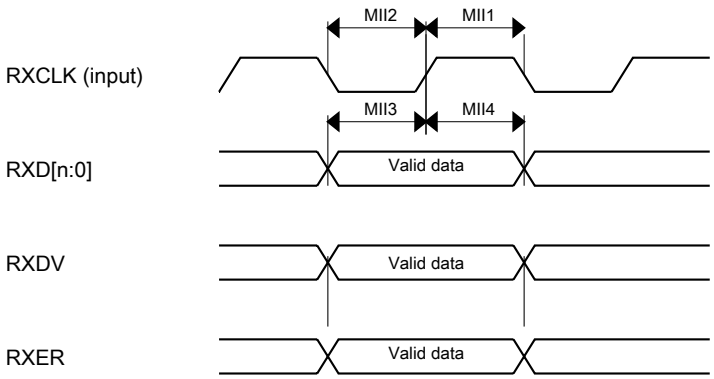


Figure 38. RMII/MII receive signal timing diagram

3.19.8.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 56. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

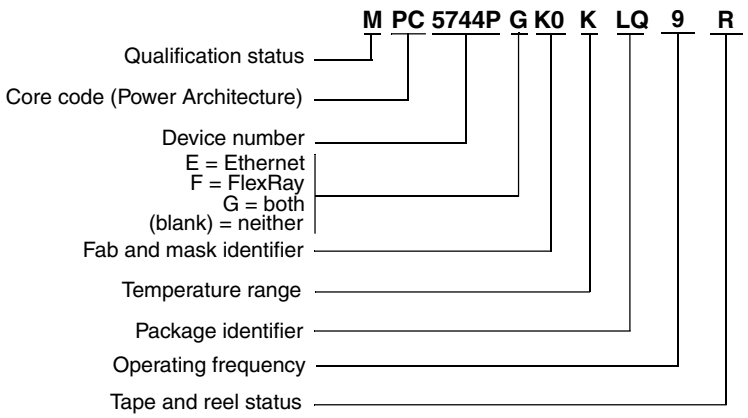
4 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
257-ball MAPBGA	98ASA00081D

5 Ordering information



Temperature range	Package identifier	Operating frequency	Qualification status	Tape and reel status
M = –40°C to +125°C K = –40°C to +135°C for extended temp (+165°C T_J)	LQ = 144 LQFP MM = 257 MAPBGA	9 = 200 MHz 8 = 180 MHz 5 = 150 MHz	P = Pre-qualification M = Fully spec. qualified, general market flow S = Fully spec. qualified, automotive flow	R = Tape and reel (blank) = Trays

Note: Not all options are available on all devices.

Table 57. Orderable part number examples

Part number[1]	Flash/SRAM	Package	Other features
SPC5744PFK1MLQ9	2.5 MB/384 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5744PGK1MMM9	2.5 MB/384 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C
SPC5743PFK1MLQ9	2 MB/256 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5743PGK1MMM9	2 MB/256 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C
SPC5742PFK1MLQ9	1.5 MB/192 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5742PGK1MMM9	1.5 MB/192 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C
SPC5741PFK1MLQ9	1 MB/128 KB	144 LQFP (Pb free)	-40 to +125 °C
SPC5741PGK1MMM9	1 MB/128 KB	257 MAPBGA (Pb free)	Ethernet interface LFAST interface Nexus Aurora -40 to +125 °C