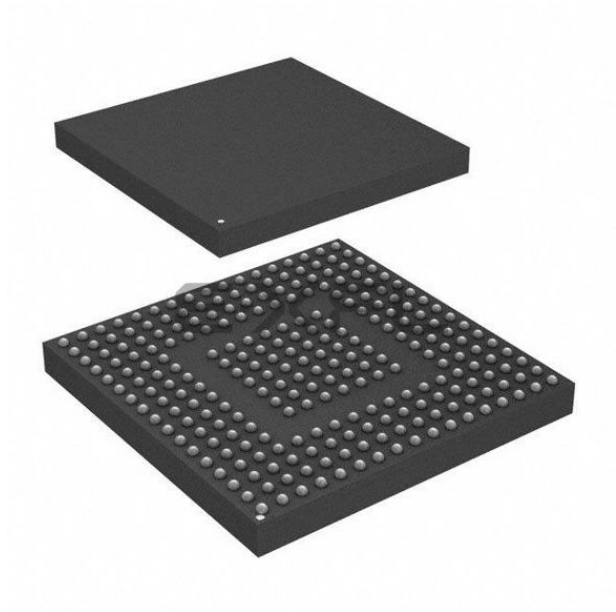

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	-
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pgk1ammm9

1 Introduction

1.1 Features

The following table summarizes the features of the MPC5744P.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution speed	0 MHz to 200 MHz (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory—see Table 2 for additional details	
Code/data flash memory	**2.5 MB**, ECC, RWW
Data flash memory	Supported with RWW
SRAM	**384 KB**, ECC
Overlay access to SRAM from Flash Memory Controller	Yes
Modules	
Interrupt controller	32 interrupt priority levels, 16 SW programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	Type	Description	144LQFP	257MAPBGA
				L6
				L12
				M6
				M7
				M8
				M9
				M10
				M11
				M12
$V_{SS\_LV\_COR}$	Ground	Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144LQFP (pin 35).	17	B1
			35	G7
			40	G8
			71	G9
			94	G10
			96	G11
			132	H7
			137	H8
				H9
				H10
				H11
				J7
				J8
				J9
				J10
				J11
				K7
				K8
				K9
				K10
				K11
				L7
				L8
				L9
				L10
				L11
$V_{DD\_LV\_PLL}$	Power	PLL low voltage Supply	36	P4
$V_{SS\_LV\_PLL}$	Ground	PLL low voltage Ground	35	N4

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0011-1111	—	Reserved	—	—		
	IMCR[48]	0001	SCK	DSPI2	DSPI 2 Input Serial Clock	I		
	IMCR[59]	0010	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I		
	IMCR[173]	0001	REQ0	SIUL2	SIUL2 External Interrupt 0	I		
A[1]	MSCR[1]	0000 (Default)	GPIO[1]	SIUL2-GPIO[1]	General Purpose IO A[1]	I/O	74	T14
		0001	ETC1	eTimer_0	eTimer_0 Input/Output Data Channel 1	I/O		
		0010	SOUT	DSPI2	DSPI 2 Serial Data Out	O		
		0011-1111	—	Reserved	—	—		
	IMCR[60]	0010	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I		
	IMCR[174]	0001	REQ1	SIUL2	SIUL2 External Interrupt Source 1	I		
A[2]	MSCR[2]	0000 (Default)	GPIO[2]	SIUL2-GPIO[2]	General Purpose IO A[2]	I/O	84	L14
		0001	ETC2	eTimer_0	eTimer_0 Input/Output Data Channel 2	I/O		
		0010	—	Reserved	—	—		
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[169]	0000 (Default)	ABS0	MC_RGM	RGM external boot mode 1	I		
	IMCR[47]	0010	SIN	DSPI2	DSPI 2 Serial Data Input	I		
	IMCR[61]	0010	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I		
	IMCR[97]	0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I		
	IMCR[175]	0001	REQ2	SIUL2	SIUL2 External Interrupt Source 2	I		
A[3]	MSCR[3]	0000 (Default)	GPIO[3]	SIUL2-GPIO[3]	General Purpose IO A[3]	I/O	92	G15
		0001	ETC3	eTimer_0	eTimer_0 Input/Output Data Channel 3	I/O		
		0010	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[171]	0000 (Default)	ABS2	MC_RGM	RGM external boot mode 2	I		
	IMCR[62]	0010	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[63]	0001	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
	IMCR[192]	0001	REQ19	SIUL2	SIUL2 External Interrupt Source 19	I		
B[15]	MSCR[31]	0000 (Default)	GPI[31][4] ADC1_AN[2]	SIUL2-GPI[31]	General Purpose Input B[15]	I	62	R11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[193]	0001	REQ20	SIUL2	SIUL2 External Interrupt Source 20	I		
C[0]	MSCR[32]	0000 (Default)	GPI[32][4] ADC1_AN[3]	SIUL2-GPI[32]	General Purpose Input C[0]	I	66	R12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[1]	MSCR[33]	0000 (Default)	GPI[33][4] ADC0_AN[2]	SIUL2-GPI[33]	General Purpose Input C[1]	I	41	T4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[2]	MSCR[34]	0000 (Default)	GPI[34][4] ADC0_AN[3]	SIUL2-GPI[34]	General Purpose Input C[2]	I	45	U5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[4]	MSCR[36]	0000 (Default)	GPIO[36]	SIUL2-GPIO[36]	General Purpose IO C[4]	I/O	11	H3
		0001	CS0	DSPI0	DSPI 0 Peripheral Chip Select 0	I/O		
		0010	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0011	DEBUG4	SSCM	SSCM Debug Output 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[93]	0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input 1	I		
	IMCR[195]	0001	REQ22	SIUL2	SIUL2 External Interrupt Source 22	I		
C[5]	MSCR[37]	0000 (Default)	GPIO[37]	SIUL2-GPIO[37]	General Purpose IO C[5]	I/O	13	G3
		0001	SCK	DSPI0	DSPI 0 Input/Output Serial Clock	I/O		
		0010	—	Reserved	—	—		
		0011	DEBUG5	SSCM	SSCM Debug Output 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0001	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
C[15]	MSCR[47]	0000 (Default)	GPIO[47]	SIUL2-GPIO[47]	General Purpose IO C[15]	I/O	124	A8
		0001	FR_A_TXEN	FLEXRAY	FlexRay Transmit Enable Channel A	O		
		0010	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[38]	0010	EXT_IN	CTU_0	CTU 0 External Trigger Input	I		
	IMCR[65]	0010	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I		
	IMCR[87]	0010	EXT_SYNC	FlexPWM_0	FlexPWM_0 External Sync Input	I		
	IMCR[91]	0010	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I		
D[0]	MSCR[48]	0000 (Default)	GPIO[48]	SIUL2-GPIO[48]	General Purpose IO D[0]	I/O	125	B8
		0001	FR_A_TX	FLEXRAY	FlexRay Transmit Data Channel A	O		
		0010	ETC1	eTimer_1	eTimer_1 Input/Output Data Channel 1	I/O		
		0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 1	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[66]	0010	ETC1	eTimer_1	eTimer_1 Input Data Channel 1	I		
	IMCR[92]	0010	B1	FlexPWM_0	FlexPWM_0 Channel B Input 1	I		
D[1]	MSCR[49]	0000 (Default)	GPIO[49]	SIUL2-GPIO[49]	General Purpose IO D[1]	I/O	3	E3
		0001	—	Reserved	—	—		
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O		
		0011	EXT_TGR	CTU_0	CTU 0 External Trigger Output	O		
		0100-1111	—	Reserved	—	—		
	IMCR[67]	0011	ETC2	eTimer_1	eTimer_1 Input Data Channel 2	I		
	IMCR[136]	0001	FR_A_RX	FLEXRAY	FlexRay Channel A Receive Pin	I		
D[2]	MSCR[50]	0000 (Default)	GPIO[50]	SIUL2-GPIO[50]	General Purpose IO D[2]	I/O	140	B4
		0001	—	Reserved	—	—		
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0010	—	Reserved	—	—		
		0011	LFAST_RXP	LFAST	SIPI/LFAST LVDS receive positive terminal	I		
		0100-1111	—	Reserved	—	—		
	IMCR[98]	0100	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
G[8]	MSCR[104]	0000 (Default)	GPIO[104]	SIUL2-GPIO[104]	General Purpose IO G[8]	I/O	81	N14
		0001	FR_DBG[0]	FLEXRAY	FlexRay Debug Strobe Signal 0	O		
		0010	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O		
		0011	RMII_CLK	ENET_0	Ethernet RMII Clock (used in MII to RMII Gaskets)	O		
		0100-1111	—	Reserved	—	—		
	IMCR[83]	0011	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[194]	0001	REQ21	SIUL2	SIUL2 External Interrupt Source 21	I		
	IMCR[205]	0011	SENT_RX[0]	SENT_0	SENT 0 Receiver channel 0	I		
	IMCR[233]	0001	TX_CLK	ENET_0	Ethernet Transmit Clock	I		
G[9]	MSCR[105]	0000 (Default)	GPIO[105]	SIUL2-GPIO[105]	General Purpose IO G[9]	I/O	79	P14
		0001	FR_DBG[1]	FLEXRAY	FlexRay Debug Strobe Signal 1	O		
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O		
		0011	TX_D0	ENET_0	Ethernet MII/RMII transmit data 0	O		
		0100-1111	—	Reserved	—	—		
	IMCR[84]	0011	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I		
	IMCR[202]	0001	REQ29	SIUL2	SIUL2 External Interrupt Source 29	I		
	IMCR[213]	0011	SENT_RX[0]	SENT_1	SENT 1 Receiver channel 0	I		
G[10]	MSCR[106]	0000 (Default)	GPIO[106]	SIUL2-GPIO[106]	General Purpose IO G[10]	I/O	77	R17
		0001	FR_DBG[2]	FLEXRAY	FlexRay Debug Strobe Signal 2	O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	TX_D1	ENET_0	Ethernet MII/RMII transmit data 1	O		
		0100-1111	—	Reserved	—	—		
	IMCR[85]	0010	FAULT2	FlexPWM_0	FlexPWM_0 Fault Input 2	I		
	IMCR[206]	0100	SENT_RX[1]	SENT_0	SENT 0 Receiver channel 1	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[11]	MSCR[107]	0000 (Default)	GPIO[107]	SIUL2-GPIO[107]	General Purpose IO G[11]	I/O	75	T15
		0001	FR_DBG[3]	FLEXRAY	FlexRay Debug Strobe Signal 3	O		
		0010	—	Reserved	—	—		
		0011	TX_D3	ENET_0	Ethernet MII/RMII transmit data 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0011	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		
	IMCR[214]	0100	SENT_RX[1]	SENT_1	SENT 1 Receiver channel 1	I		
H[4]	MSCR[116]	0000 (Default)	GPIO[116]	SIUL2-GPIO[116]	General Purpose IO H[4]	I/O		F4
		0001	X0	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 0	I/O		
		0010	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[71]	0001	ETC0	eTimer_2	eTimer_2 Input Data Channel 0	I		
	IMCR[231]	0001	CRS	ENET_0	Ethernet MII Carrier Sense	I		
H[5]	MSCR[117]	0000 (Default)	GPIO[117]	SIUL2-GPIO[117]	General Purpose IO H[5]	I/O		F3
		0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[105]	0010	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I		
	IMCR[230]	0001	COL	ENET_0	Ethernet MII Collision	I		
H[6]	MSCR[118]	0000 (Default)	GPIO[118]	SIUL2-GPIO[118]	General Purpose IO H[6]	I/O		C13
		0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[106]	0010	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I		
H[7]	MSCR[119]	0000 (Default)	GPIO[119]	SIUL2-GPIO[119]	General Purpose IO H[7]	I/O		F2
		0001	X1	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 1	I/O		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[39]	0001	EXT_IN	CTU_1	CTU 1 External Trigger Input	I		
J[5]	MSCR[149]	0000 (Default)	GPI[149][4] ADC2_ADC3_AN[0]	SIUL2-GPI[149]	General Purpose Input J[5]	I		P8
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[206]	0010	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I		
J[6]	MSCR[150]	0000 (Default)	GPI[150][4] ADC2_ADC3_AN[1]	SIUL2-GPI[150]	General Purpose Input J[6]	I		P9
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[214]	0010	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I		
J[7]	MSCR[151]	0000 (Default)	GPI[151][4] ADC2_ADC3_AN[2]	SIUL2-GPI[151]	General Purpose Input J[7]	I		P10
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
J[8]	MSCR[152]	0000 (Default)	GPIO[152]	SIUL2-GPIO[152]	General Purpose IO J[8]	I/O	95	G16
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[34]	0011	RXD	CAN2	CAN 2 Receive Pin	I		
	IMCR[73]	0100	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I		
	IMCR[75]	0100	ETC4	eTimer_2	eTimer_2 Input Data Channel 4	I		
J[9]	MSCR[153]	0000 (Default)	GPIO[153]	SIUL2-GPIO[153]	General Purpose IO J[9]	I/O	16	K1
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O		
		0010	NEX_RDY_B	NPC	Nexus data ready for transfer (RDY_B)	O		
		0011-1111	—	Reserved	—	—		
	IMCR[39]	0010	EXT_IN	CTU_1	CTU_1 External Trigger Input	I		
	IMCR[76]	0100	ETC5	eTimer_2	eTimer_2 Input Data Channel 5	I		
	IMCR[229]	0001	RX_D3	ENET_0	Ethernet MII Receive Data 3	I		
NMI_B	MSCR[154]	0000 (Default)	NMI_B	Core	Non-Maskable Interrupt	I	1	E4

1. Selecting an alternative function with a "Reserved" source function causes the pin to enter a null state (input buffer and output buffer enables are both 0).

2. **(Default) = ALT mode configuration after reset.**
3. Changing the B[5] configuration during debug might affect the availability of TDI.
4. ADC analog input: Program corresponding MSCR APC bit and enable ADC to switch on the analog input path.
5. When the LFAST interface is selected the other functionality of the MSCR register is not available.
6. Shared with SIPI LFAST transmit pad SIPI_TXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
7. To operate D[7] as GPIO, disable the Sine Wave Generator (SGEN) and the peripheral bus clock of the SGEN: Program the MC_ME_PCTL239 register to select an MC_ME_RUN_PCn (or MC_ME_LP_PCn) configuration where the field for the desired mode is 0.
8. SGEN output if SGEN is enabled.
9. Shared with SIPI LFAST receive pad SIPI_RXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
10. Shared with SIPI LFAST receive pad SIPI_TXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
11. Shared with SIPI LFAST receive pad SIPI_RXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.

The following table list ports that are not implemented. The corresponding control and data registers are not implemented.

Table 9. Ports - Not Implemented

Port Name	Port Index
C	3,8,9
D	13,15
E	1,3,8
F	1,2
G	0,1,[12:15]
H	[0:3]
J	[10:15]

Any attempt to access unimplemented MSCRs generates a bus error. The read value from unimplemented ports must be masked in case of parallel port accesses.

2.2.6 Peripheral input muxing

The following table describes the peripheral muxing capabilities of the device.

Table 10. Peripheral muxing

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
FlexCAN_0	RXD	IMCR[32]	0000 (Default)[1]	—	Disable
			0001	I/O-Pad	A[15]
			0010	I/O-Pad	B[1]
			0011-1111	—	Reserved[2]
FlexCAN_1	RXD	IMCR[33]	0000 (Default)	—	Disable

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0101-1111	—	Reserved
DSPI_3	SCK	IMCR[51]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010	I/O-Pad	D[11]
			0011	I/O-Pad	E[13]
			0100	I/O-Pad	I[15]
			0101-1111	—	Reserved
DSPI_3	CS0	IMCR[52]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[11]
			0010	I/O-Pad	D[10]
			0011	I/O-Pad	F[5]
			0100	I/O-Pad	I[14]
			0101-1111	—	Reserved
eTimer_0	ETC0	IMCR[59]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[10]
			0010	I/O-Pad	A[0]
			0011-1111	—	Reserved
eTimer_0	ETC1	IMCR[60]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[11]
			0010	I/O-Pad	A[1]
			0011-1111	—	Reserved
eTimer_0	ETC2	IMCR[61]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
eTimer_0	ETC3	IMCR[62]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[14]
			0010	I/O-Pad	A[3]
			0011-1111	—	Reserved
eTimer_0	ETC4	IMCR[63]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[14]
			0010	I/O-Pad	G[3]
			0011	I/O-Pad	A[4]
			0100	I/O-Pad	C[11]
			0101-1111	—	Reserved
eTimer_0	ETC5	IMCR[64]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[8]
			0010	I/O-Pad	G[4]
			0011	I/O-Pad	C[12]

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0010-1111	—	Reserved
SIUL	REQ25	IMCR[198]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[13]
			0010-1111	—	Reserved
SIUL	REQ26	IMCR[199]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[14]
			0010-1111	—	Reserved
SIUL	REQ27	IMCR[200]	0000 (Default)	—	Disable
			0001	I/O-Pad	E[15]
			0010-1111	—	Reserved
SIUL	REQ28	IMCR[201]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010-1111	—	Reserved
SIUL	REQ29	IMCR[202]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[9]
			0010-1111	—	Reserved
SIUL	REQ30	IMCR[203]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[12]
			0010-1111	—	Reserved
SIUL	REQ31	IMCR[204]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[13]
			0010-1111	—	Reserved
SENT_0	SENT_RX[0]	IMCR[205]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010	I/O-Pad	I[7]
			0011	I/O-Pad	G[8]
			0100-1111	—	Reserved
SENT_0	SENT_RX[1]	IMCR[206]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[11]
			0010	I/O-Pad	J[5]
			0011	I/O-Pad	A[9]
			0100	I/O-Pad	G[10]
			0101-1111	—	Reserved
SENT_1	SENT_RX[0]	IMCR[213]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[7]
			0010	I/O-Pad	I[8]
			0011	I/O-Pad	G[9]
			0100	I/O-Pad	C[12]
			0101-1111	—	Reserved

Table continues on the next page...

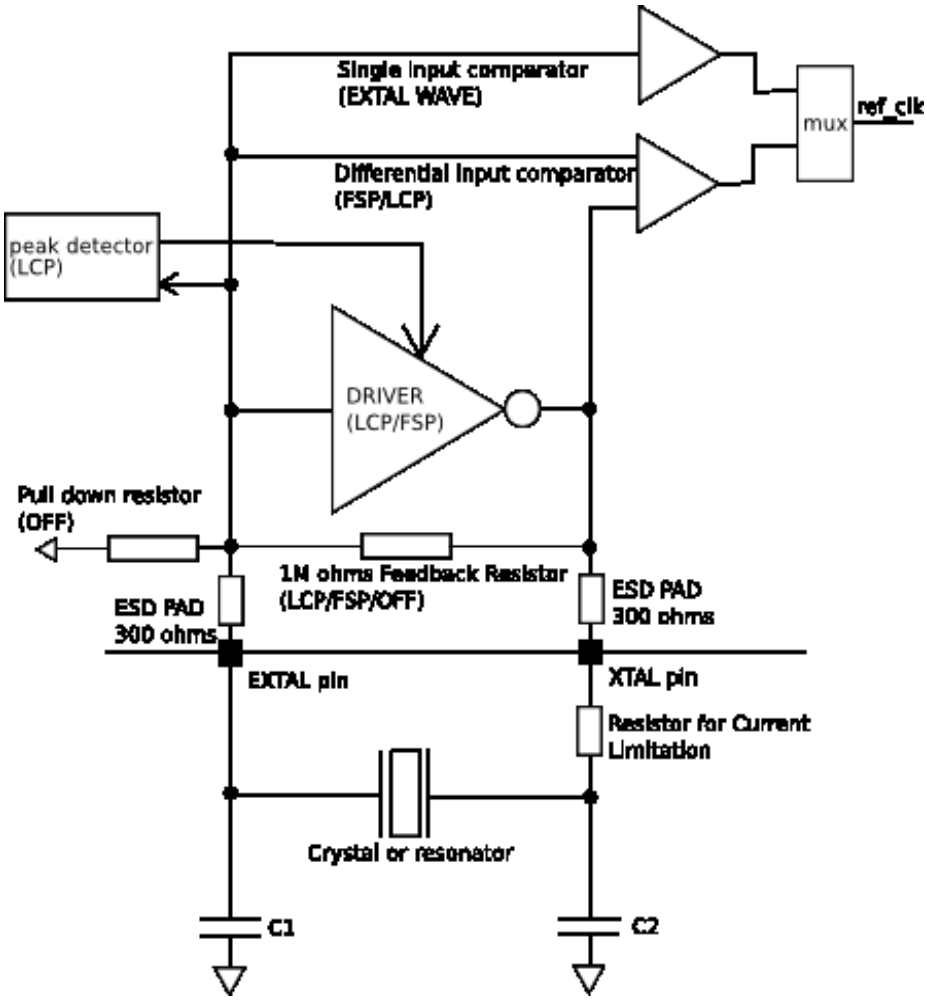

Figure 5. Oscillator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions[1]	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP	—	4[2]	—	40	MHz
$g_{mXOSCHS}$	Driver transconductance	LCP	$V_{DD\_HV\_OSC}$ = 3.3V	—	20	—	mA/V
		FSP	–5%, +10%	—	30	—	
V_{XOSCHS}	Oscillation amplitude	LCP	f_{OSC} = 4, 8, 16 MHz	1.1	1.3	2.6	V
			f_{OSC} = 40 MHz	1.2	1.5	1.7	V
$T_{XOSCHSSU}$	Oscillator startup time	FSP/LCP[3]	f_{OSC} = 4 MHz	1.75	2.5	2.9	ms
			f_{OSC} = 8, 16, 40 MHz	0.25	0.5	1.1	ms

Table continues on the next page...

3.15.1 Input equivalent circuit and ADC conversion characteristics

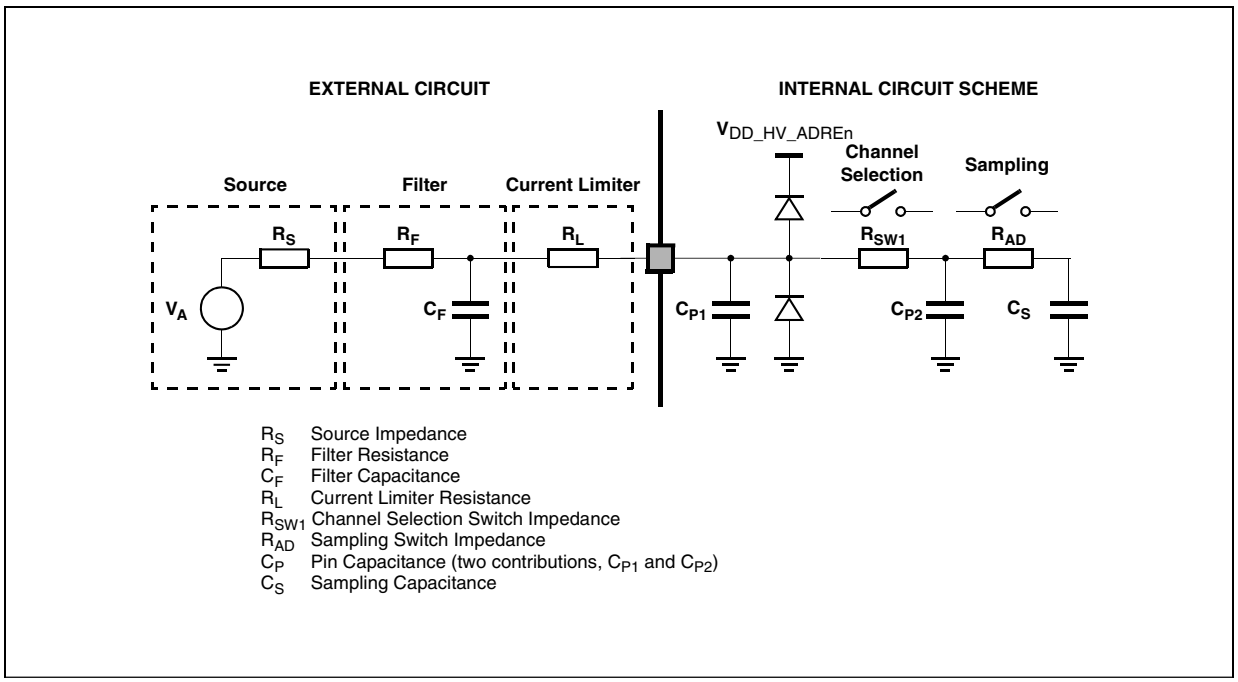

Figure 8. Input equivalent circuit

NOTE

Unless noted otherwise, the specifications in Table 27 assume the use of 12-bit resolution (high accuracy, recommended): In ADC_CALBISTREG, set OPMODE to 110b.

Table 27. ADC conversion characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	20	—	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz, 12-bit resolution	250	—	—	ns
		80 MHz, 12-bit resolution (high accuracy, recommended)	250	—	—	
t_{conv}	Conversion time[4]	80 MHz, 12-bit resolution	650	—	—	ns
		80 MHz, 12-bit resolution (high accuracy, recommended)	700	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5[6]	pF

Table continues on the next page...

3.16.1.2 Flash memory Array Integrity and Margin Read specifications

Table 29. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.1.3 Flash memory module life specifications

Table 30. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

Table 33. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.2.3 Flash memory module life specifications

Table 34. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	-	250,000	-	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	-	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	-	Years
		Blocks with 100,000 P/E cycles.	20	-	Years
		Blocks with 250,000 P/E cycles.	10	-	Years

1. Program and erase supported across standard temperature specs. Up to 10,000 program and erase cycles may be done between 150 °C and 165 °C out of the total specified number of cycles.
2. Program and erase supported across standard temperature specs.

3.16.2.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.

Table 41. Reset ($\overline{\text{EXT\_POR}}$) electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
W_{FPORST}	PORST input filtered pulse	—	—	—	500	ns
$W_{NFPORST}$	PORST input not filtered pulse	—	2000	—	—	ns
W_{IH}	Input high level	—	2	—	$V_{DD\_HV\_IO}$ +0.4	V
W_{IL}	Input low level	—	-0.4	—	0.8	V

3.19.2 WKUP/NMI timing

Table 42. WKUP/NMI glitch filter

Symbol	Parameter	Min	Typ	Max	Unit
W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
W_{NFNMI}	NMI pulse width that is passed	400	—	—	ns

3.19.3 Debug/JTAG/Nexus/Aurora timing

3.19.3.1 JTAG interface timing

Table 43. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time	36	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	15	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

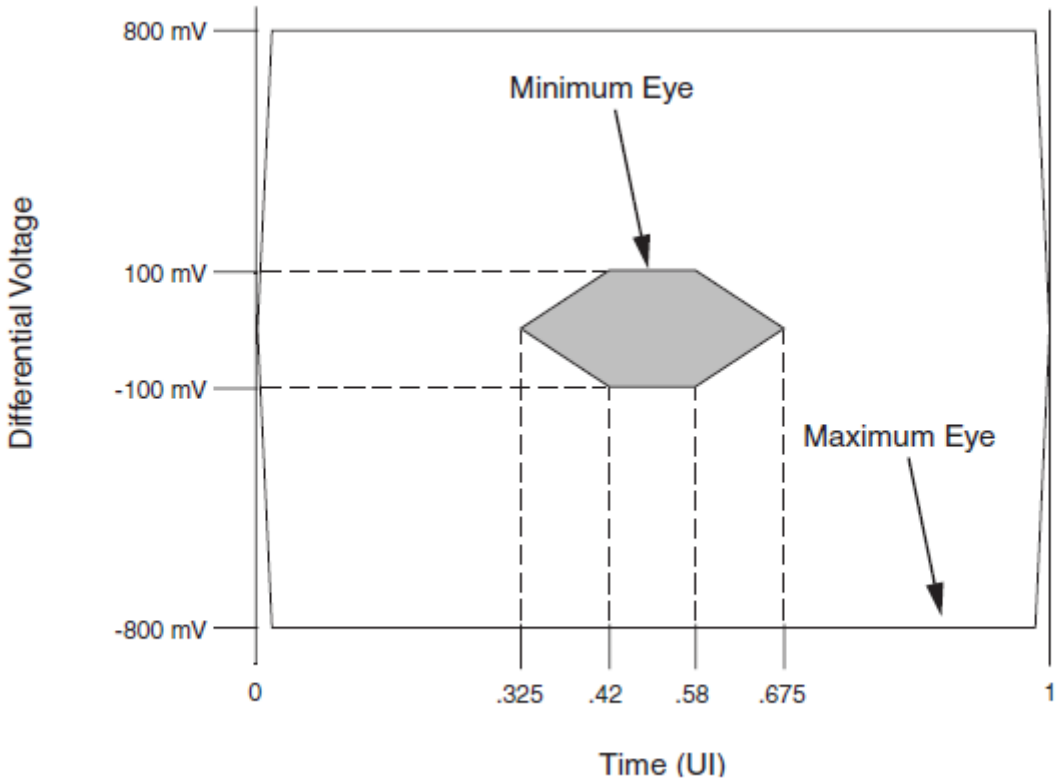

Figure 19. Nexus Aurora receiver "eye" diagram

3.19.4 External interrupt timing (IRQ pin)

Table 47. External interrupt timing

#	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

Table 48. SPI timing (continued)

#	Symbol	Parameter	Conditions	Min	Max	Unit
			Master (MTFE = 1, CPHA = 0)	–4	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. P is the number of clock cycles added to delay the SPI input sample point and is software programmable.
3. t_{SYS} is the period of the DSPI_CLKn clock, the input clock to the SPI module. Maximum frequency is 50 MHz (min t_{SYS} = 20 ns).

NOTE

For numbers shown in the following figures, see Table 48.

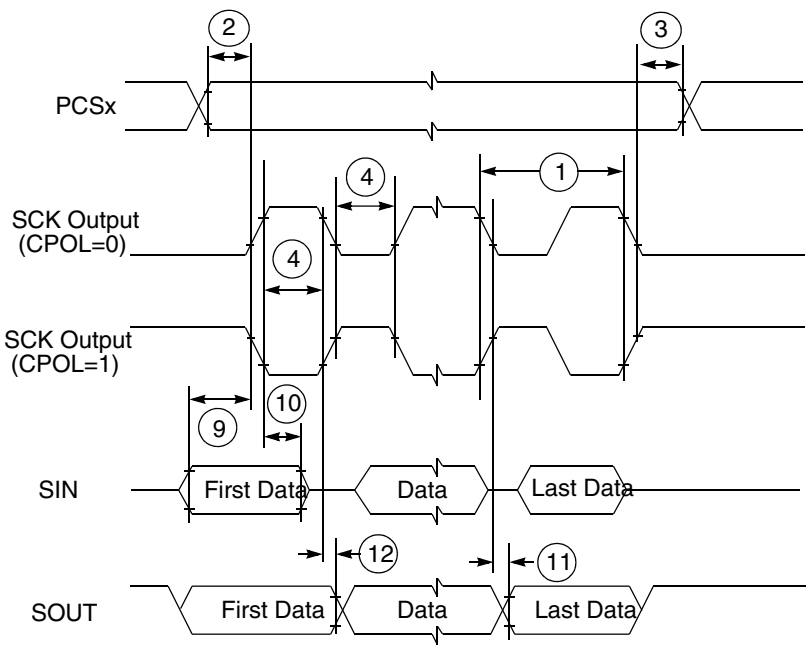

Figure 21. DSPI classic SPI timing — master, CPHA = 0

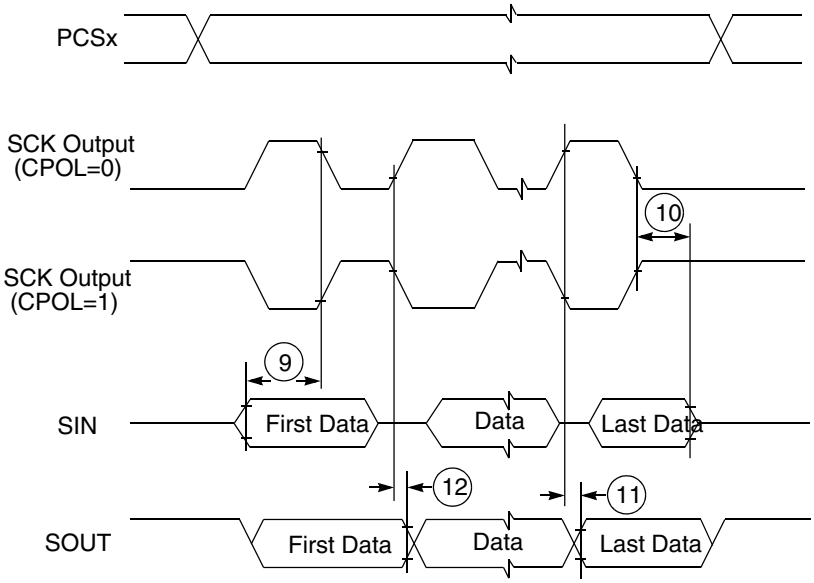

Figure 22. DSPI classic SPI timing — master, CPHA = 1

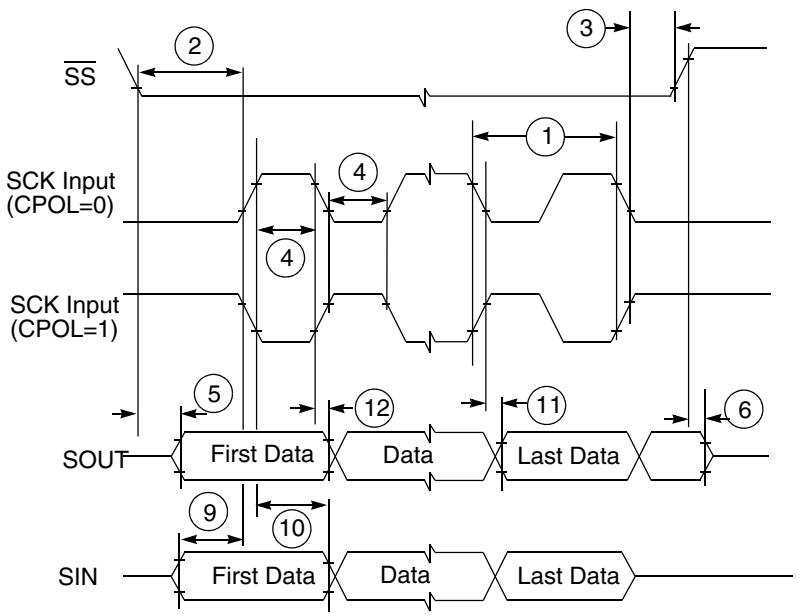

Figure 23. DSPI classic SPI timing — slave, CPHA = 0

1. All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. Not all configurations are available in the PPC parts.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 58. Revision history

Revision	Date	Description of changes

6	05/2017	Changed Freescale to NXP throughout the document.
		
		Extensively updated Generic pins/balls.
		
		Absolute maximum ratings
		• In Table 12
		  • for row set I_{INJ} changed "Maximum DC injection current per pin, 5 V pads" to "Maximum DC injection current per pin, 5V ADC pads".
		  • For row set I_{INJ} updated the footnote.
		
		Voltage regulator electrical characteristics
		• In Table 17
		  • Added the note, "The device has to.....which drives the EXT_POR".
		  • In existing row C_{ld} added Maximum value 18.8.
		  • In existing row C_{pd} added Maximum value 300.
		  • Renamed parameter from "Load Current transient" to "Load current transient time" and updated the Min and Max value.
		  • Renamed the following parameters:
		  • Supply ramp rate VDD12_CORE to Supply ramp rate VDD_LV_COR
		  • Supply ramp rate VDD33_REG to Supply ramp rate VDD_HV_PMU
		  • POR VDD12_CORE to POR_COR
		  • POR VDD33_REG to POR_PMU
		• In Figure 4 changed VDD33_REG to VDD_HV_PMU.
		
		16 MHz Internal RC Oscillator (IRCOSC) electrical specifications
		• In Table 26
		  • Changed the Min and Max values for IRCOSC frequency (untrimmed) parameter.
		  • Added IRC frequency variation with temperature and voltage compensation parameter row.
		
		ADC electrical characteristics
		• Changed the Note from "Unless noted otherwise, the specifications in Table 27 assume the use of 13-bit resolution: In ADC_CALBISTREG, set OPMODE to 110b" to "Unless noted otherwise, the specifications in Table 27 assume the use of 12-bit resolution (high accuracy, recommended): In ADC_CALBISTREG, set OPMODE to 110b".
		• In Table 27 for existing rows t_{sample} and t_{conv} changed the "13 bit resolution" to "12-bit resolution (high accuracy, recommended)".
		
		• In Flash memory program and erase specifications changed symbols for specifications:
		  • Quad-page (1024 bits) program time: Changed symbol from t_{qppgn} to t_{qppgm}
		  • 16 KB Block program time: Changed symbol from t_{16kpgn} to t_{16kpgm}
		• In Flash memory Array Integrity and Margin Read specifications incorporated minor editorial changes
		• In Flash memory AC timing specifications for t_{psus}:

Table continues on the next page...