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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 150MHz |
| Connectivity | CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | 79 |
| Program Memory Size | 2.5MB (2.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.15V ~ 5.5V |
| Data Converters | A/D 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5744pk1amlq5 |

## 2.2 Pin/ball descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the device. Note that this section is under development.

### 2.2.1 Pin/ball startup and reset states

The following table provides startup state and reset state information for device pins/balls.

The startup state and subsequent states of the following pins/balls cannot be configured by the user:

- JCOMP
- TMS
- TCK
- XTAL/EXTAL
- FCCU_F[0] and FCCU_F[1]
- EXT_POR_B
- RESET_B

The user can configure the state after reset of the following pins/balls by programming the applicable MSCRs/IMCRs:

- GPIOs
- Analog inputs
- TDI
- TDO
- NMI_B
- FAB
- ABS[0]
- ABS[2]

**Table 3. Pin/ball startup and reset states**

| Pin/ball | Startup state[1], [2] | State during reset | State after reset | 144LQFP | 257MAPBGA |
|---|---|---|---|---|---|
| GPIOs | hi-z | hi-z | hi-z | Note[3] | Note[3] |
| Analog inputs[4] | hi-z | hi-z | hi-z | Note[3] | Note[3] |
| JCOMP (TRST) | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |
| TDI | hi-z | input, weak pull-up | input, weak pull-up | Note[5] | Note[5] |
| TDO | hi-z | output, hi-z | output, hi-z | Note[5] | Note[5] |
| TMS[6] | hi-z | input, weak pull-up | input, weak pull-up | Note[5] | Note[5] |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[48] | 0001 | SCK | DSPI2 | DSPI 2 Input Serial Clock | I | | |
| | IMCR[59] | 0010 | ETC0 | eTimer_0 | eTimer_0 Input Data Channel 0 | I | | |
| | IMCR[173] | 0001 | REQ0 | SIUL2 | SIUL2 External Interrupt 0 | I | | |
| A[1] | MSCR[1] | 0000 (Default) | GPIO[1] | SIUL2-GPIO[1] | General Purpose IO A[1] | I/O | 74 | T14 |
| | | 0001 | ETC1 | eTimer_0 | eTimer_0 Input/Output Data Channel 1 | I/O | | |
| | | 0010 | SOUT | DSPI2 | DSPI 2 Serial Data Out | O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[60] | 0010 | ETC1 | eTimer_0 | eTimer_0 Input Data Channel 1 | I | | |
| | IMCR[174] | 0001 | REQ1 | SIUL2 | SIUL2 External Interrupt Source 1 | I | | |
| A[2] | MSCR[2] | 0000 (Default) | GPIO[2] | SIUL2-GPIO[2] | General Purpose IO A[2] | I/O | 84 | L14 |
| | | 0001 | ETC2 | eTimer_0 | eTimer_0 Input/Output Data Channel 2 | I/O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[169] | 0000 (Default) | ABS0 | MC_RGM | RGM external boot mode 1 | I | | |
| | IMCR[47] | 0010 | SIN | DSPI2 | DSPI 2 Serial Data Input | I | | |
| | IMCR[61] | 0010 | ETC2 | eTimer_0 | eTimer_0 Input Data Channel 2 | I | | |
| | IMCR[97] | 0001 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input 3 | I | | |
| | IMCR[175] | 0001 | REQ2 | SIUL2 | SIUL2 External Interrupt Source 2 | I | | |
| A[3] | MSCR[3] | 0000 (Default) | GPIO[3] | SIUL2-GPIO[3] | General Purpose IO A[3] | I/O | 92 | G15 |
| | | 0001 | ETC3 | eTimer_0 | eTimer_0 Input/Output Data Channel 3 | I/O | | |
| | | 0010 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | I/O | | |
| | | 0011 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[171] | 0000 (Default) | ABS2 | MC_RGM | RGM external boot mode 2 | I | | |
| | IMCR[62] | 0010 | ETC3 | eTimer_0 | eTimer_0 Input Data Channel 3 | I | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0011 | X2 | FlexPWM_0 | FlexPWM_0 Auxiliary Input/ Output 2 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[49] | 0010 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | I/O | | |
| | IMCR[89] | 0001 | B0 | FlexPWM_0 | FlexPWM_0 Channel B Input 0 | I | | |
| | IMCR[96] | 0001 | X2 | FlexPWM_0 | FlexPWM_0 Auxiliary Input 2 | I | | |
| | IMCR[182] | 0001 | REQ9 | SIUL2 | SIUL2 External Interrupt Source 9 | I | | |
| | IMCR[214] | 0011 | SENT_RX[1] | SENT_1 | SENT 1 Receiver channel 1 | I | | |
| A[11] | MSCR[11] | 0000 (Default) | GPIO[11] | SIUL2-GPIO[11] | General Purpose IO A[11] | I/O | 120 | D10 |
| | | 0001 | SCK | DSPI2 | DSPI 2 Input/Output Serial Clock | I/O | | |
| | | 0010 | A0 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 0 | I/O | | |
| | | 0011 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 2 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[48] | 0010 | SCK | DSPI2 | DSPI 2 Input Serial Clock | I | | |
| | IMCR[88] | 0001 | A0 | FlexPWM_0 | FlexPWM_0 Channel A Input 0 | I | | |
| | IMCR[94] | 0001 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input 2 | I | | |
| | IMCR[183] | 0001 | REQ10 | SIUL2 | SIUL2 External Interrupt Source 10 | I | | |
| A[12] | MSCR[12] | 0000 (Default) | GPIO[12] | SIUL2-GPIO[12] | General Purpose IO A[12] | I/O | 122 | D7 |
| | | 0001 | SOUT | DSPI2 | DSPI 2 Serial Data Out | O | | |
| | | 0010 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 2 | I/O | | |
| | | 0011 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 2 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[94] | 0010 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input 2 | I | | |
| | IMCR[95] | 0001 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input 2 | I | | |
| | IMCR[184] | 0001 | REQ11 | SIUL2 | SIUL2 External Interrupt Source 11 | I | | |
| A[13] | MSCR[13] | 0000 (Default) | GPIO[13] | SIUL2-GPIO[13] | General Purpose IO A[13] | I/O | 136 | C5 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 2 | I/O | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[191] | 0001 | REQ18 | SIUL2 | SIUL2 External Interrupt Source 18 | I | | |
| B[7] | MSCR[23] | 0000 (Default) | GPI[23][4] ADC0_AN[0] | SIUL2-GPI[23] | General Purpose Input B[7] | I | 43 | R5 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[165] | 0010 | RXD | LIN0 | LIN 0 Receive Pin | I | | |
| B[8] | MSCR[24] | 0 | GPI[24][4] ADC0_AN[1] | SIUL2-GPI[24] | General Purpose Input B[8] | I | 47 | P7 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[64] | 0001 | ETC5 | eTimer_0 | eTimer_0 Input Data Channel 5 | I | | |
| B[9] | MSCR[25] | 0000 (Default) | GPI[25][4] ADC0_ADC1_AN[11] | SIUL2-GPI[25] | General Purpose Input B[9] | I | 52 | U7 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[10] | MSCR[26] | 0000 (Default) | GPI[26][4] ADC0_ADC1_AN[12] | SIUL2-GPI[26] | General Purpose Input B[10] | I | 53 | R8 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[11] | MSCR[27] | 0000 (Default) | GPI[27][4] ADC0_ADC1_AN[13] | SIUL2-GPI[27] | General Purpose Input B[11] | I | 54 | T8 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[12] | MSCR[28] | 0000 (Default) | GPI[28][4] ADC0_ADC1_AN[14] | SIUL2-GPI[28] | General Purpose Input B[12] | I | 55 | U8 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[13] | MSCR[29] | 0000 (Default) | GPI[29][4] ADC1_AN[0] | SIUL2-GPI[29] | General Purpose Input B[13] | I | 60 | R10 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[166] | 0001 | RXD | LIN1 | LIN 1 Receive Pin | I | | |
| B[14] | MSCR[30] | 0000 (Default) | GPI[30][4] ADC1_AN[1] | SIUL2-GPI[30] | General Purpose Input B[14] | I | 64 | P11 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0010 | ETC1 | eTimer_2 | eTimer_2 Input/Output Data Channel 1 | I/O | | |
| | | 0011 | MDIO | ENET_0 | Ethernet MDIO input/output data | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[72] | 0001 | ETC1 | eTimer_2 | eTimer_2 Input Data Channel 1 | I | | |
| H[8] | MSCR[120] | 0000 (Default) | GPIO[120] | SIUL2-GPIO[120] | General Purpose IO H[8] | I/O | | L1 |
| | | 0001 | A1 | FlexPWM_1 | FlexPWM_1 Channel A Input/ Output 1 | I/O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | CS6 | DSPI0 | DSPI 0 Peripheral Chip Select 6 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[109] | 0010 | A1 | FlexPWM_1 | FlexPWM_1 Channel A Input 1 | I | | |
| | IMCR[228] | 0001 | RX_D2 | ENET_0 | Ethernet MII Receive Data 2 | I | | |
| H[9] | MSCR[121] | 0000 (Default) | GPIO[121] | SIUL2-GPIO[121] | General Purpose IO H[9] | I/O | | B13 |
| | | 0001 | B1 | FlexPWM_1 | FlexPWM_1 Channel B Input/ Output 1 | I/O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | CS7 | DSPI0 | DSPI 0 Peripheral Chip Select 7 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[110] | 0010 | B1 | FlexPWM_1 | FlexPWM_1 Channel B Input 1 | I | | |
| H[10] | MSCR[122] | 0000 (Default) | GPIO[122] | SIUL2-GPIO[122] | General Purpose IO H[10] | I/O | | C7 |
| | | 0001 | X2 | FlexPWM_1 | FlexPWM_1 Auxiliary Input/ Output 2 | I/O | | |
| | | 0010 | ETC2 | eTimer_2 | eTimer_2 Input/Output Data Channel 2 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[73] | 0010 | ETC2 | eTimer_2 | eTimer_2 Input Data Channel 2 | I | | |
| H[11] | MSCR[123] | 0000 (Default) | GPIO[123] | SIUL2-GPIO[123] | General Purpose IO H[11] | I/O | | C9 |
| | | 0001 | A2 | FlexPWM_1 | FlexPWM_1 Channel A Input/ Output 2 | I/O | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[112] | 0010 | A2 | FlexPWM_1 | FlexPWM_1 Channel A Input 2 | I | | |
| H[12] | MSCR[124] | 0000 (Default) | GPIO[124] | SIUL2-GPIO[124] | General Purpose IO H[12] | I/O | | A7 |

*Table continues on the next page...*

## Table 10. Peripheral muxing (continued)

| Destination peripheral | Destination functions | IMCR number | IMCR[SSS] field value | Source peripherals | Source functions |
|---|---|---|---|---|---|
| | | | 0100-1111 | — | Reserved |
| FlexPWM_0 | X2 | IMCR[96] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[10] |
| | | | 0010 | I/O-Pad | G[2] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_0 | A3 | IMCR[97] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[2] |
| | | | 0010 | I/O-Pad | C[10] |
| | | | 0011 | I/O-Pad | D[3] |
| | | | 0100 | I/O-Pad | G[6] |
| | | | 0101-1111 | — | Reserved |
| FlexPWM_0 | B3 | IMCR[98] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[3] |
| | | | 0010 | I/O-Pad | A[9] |
| | | | 0011 | I/O-Pad | D[4] |
| | | | 0100 | I/O-Pad | G[7] |
| | | | 0101-1111 | — | Reserved |
| FlexPWM_0 | X3 | IMCR[99] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | D[2] |
| | | | 0010 | I/O-Pad | D[6] |
| | | | 0011 | I/O-Pad | G[5] |
| | | | 0100-1111 | — | Reserved |
| FlexPWM_1 | FAULT0 | IMCR[100] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[0] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | FAULT1 | IMCR[101] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[1] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | FAULT2 | IMCR[102] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[2] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | FAULT3 | IMCR[103] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[3] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | A0 | IMCR[105] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | C[13] |
| | | | 0010 | I/O-Pad | H[5] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_1 | B0 | IMCR[106] | 0000 (Default) | — | Disable |

*Table continues on the next page...*

## Table 10. Peripheral muxing (continued)

| Destination peripheral | Destination functions | IMCR number | IMCR[SSS] field value | Source peripherals | Source functions |
|---|---|---|---|---|---|
| | | | 0001 | I/O-Pad | C[14] |
| | | | 0010 | I/O-Pad | H[6] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_1 | A1 | IMCR[109] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | F[12] |
| | | | 0010 | I/O-Pad | H[8] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_1 | B1 | IMCR[110] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | F[13] |
| | | | 0010 | I/O-Pad | H[9] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_1 | A2 | IMCR[112] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[4] |
| | | | 0010 | I/O-Pad | H[11] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_1 | B2 | IMCR[113] | 0000 | — | Disable |
| | | | 0001 | I/O-Pad | E[14] |
| | | | 0010 | I/O-Pad | H[12] |
| | | | 0011-1111 | — | Reserved |
| FlexRay | FR_A_RX | IMCR[136] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | D[1] |
| | | | 0010-1111 | — | Reserved |
| FlexRay | FR_B_RX | IMCR[137] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | D[2] |
| | | | 0010-1111 | — | Reserved |
| LIN_0 | RXD | IMCR[165] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | B[3] |
| | | | 0010 | I/O-Pad | B[7] |
| | | | 0011-1111 | — | Reserved |
| LIN_1 | RXD | IMCR[166] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | B[13] |
| | | | 0010 | I/O-Pad | D[12] |
| | | | 0011 | I/O-Pad | F[15] |
| | | | 0100-1111 | — | Reserved |
| MC_RGM | ABS0 | IMCR[169] | 0000 (Default) | I/O-Pad | A[2] |
| | | | 0001 | — | Disable |
| | | | 0010-1111 | — | Reserved |
| MC_RGM | ABS2 | IMCR[171] | 0000 (Default) | I/O-Pad | A[3] |
| | | | 0001 | — | Disable |

*Table continues on the next page...*

**Table 11. Peripheral muxing example**

| SSS field value in IMCR[214] | Result |
|---|---|
| 0001 | I/O-Pad I[12] is connected to SENT_1 Receive input SENT_RX[1] |
| 0010 | I/O-Pad J[6] is connected to SENT_1 Receive input SENT_RX[1] |

See Table 9 concerning the availability of port pins on the packages.

# 3 Electrical characteristics

## 3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 200 MHz.

## 3.2 165°C junction temperature option

For orderable parts whose device marking shows they support this extended temperature option:

- Operation at 150°C < $T_J$ < 165°C is allowed for a maximum cumulative time of 200 hours over the device lifetime.
- Production parameters at 165°C reflect testing over an ambient temperature range of –40°C to 150°C with appropriate guardbanding to guarantee operation at 165°C.

## 3.3 Absolute maximum ratings

**NOTE**

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

- Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 6.0 V (10 hours, device in reset—no switching)
- Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 5.5 V (always)
- Absolute maximum ADC input pin voltage = 7.0 V (60 seconds lifetime), when $V_{DD\_HV}$ is connected to the 5 V
- Absolute maximum ADC input pin voltage = 6.5 V (always while respecting 5 mA maximum injection), when $V_{DD\_HV}$ is connected to the 5 V

## 3.4 Recommended operating conditions

**NOTE**

Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and DC electrical specifications for I/Os might not be guaranteed.

**Table 13. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_PMU}$[1] | 3.3 V voltage regulator supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_IO}$[2] | 3.3 V input/output supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_IO}$ | Input/output ground voltage | — | 0 | 0 | V |
| $V_{DD\_HV\_FLA}$[3] | 3.3 V flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_FLA}$ | Flash memory ground | — | 0 | 0 | V |
| $V_{DD\_HV\_OSC}$[4] | 3.3 V crystal oscillator amplifier supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_OSC}$ | 3.3 V crystal oscillator amplifier ground | — | 0 | 0 | V |
| $V_{DD\_HV\_ADRE0}$<br>$V_{DD\_HV\_ADRE1}$ | 3.3 V / 5.0 V ADC_0 high reference voltage<br>3.3 V / 5.0 V ADC_1 high reference voltage | $T_J \le 150°C$ | 3.15 to 5.5 | | V |
| $V_{DD\_HV\_ADRE0}$[5]<br>$V_{DD\_HV\_ADRE1}$ | 3.3 V / 5.0 V ADC_0 high reference voltage<br>3.3 V / 5.0 V ADC_1 high reference voltage | $150°C < T_J < 165°C$ (only for corresponding marked parts) | 3.15 to 5.25 | | V |
| $V_{SS\_HV\_ADRE0}$[5]<br>$V_{SS\_HV\_ADRE1}$ | ADC_0 ground and low reference voltage<br>ADC_1 ground and low reference voltage | — | 0 | 0 | V |
| $V_{DD\_HV\_ADV}$[6] | 3.3 V ADC supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_ADV}$ | 3.3 V ADC supply ground | — | 0 | 0 | V |
| $V_{DD\_LV\_COR}$[7] | Core supply, 1.25 V +/-5% | — | 1.19 | 1.32 | V |
| $V_{DD\_LV\_CORx}$ | Internal supply voltage | — | — | — | V |
| $V_{SS\_LV\_CORx}$ | Internal reference voltage | — | 0 | 0 | V |
| $V_{DD\_LV\_PLL}$ | Internal PLL supply voltage | — | 1.19 | 1.32 | V |
| $V_{SS\_LV\_PLL}$ | Internal PLL reference voltage | — | 0 | 0 | V |
| $V_{DD\_LV\_NEXUS}$ | Aurora LVDS supply voltage | — | 1.19 | 1.32 | V |
| $V_{SS\_LV\_NEXUS}$ | Aurora LVDS supply ground | — | 0 | 0 | V |
| $V_{DD\_LV\_LFAST}$ | LFAST PLL supply voltage | — | 1.19 | 1.32 | V |
| $V_{SS\_LV\_LFAST}$ | LFAST PLL supply ground | — | 0 | 0 | V |
| $I_{IC}$ | DC injection current per pin[8, 9, 10] | Digital pins | –3.0 | 3.0 | mA |
| | | Analog pins | –3.0 | 3.0 | |

*Table continues on the next page...*

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- $T_T$ = thermocouple temperature on top of the package (°C)
- $\Psi_{JT}$ = thermal characterization parameter (°C/W)
- $P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

#### 3.5.1.1 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

## 3.6 Electromagnetic compatibility (EMC)

Tests were carried out in accordance with the International Electrotechnical Commission specifications:

- IEC 61967: Integrated Circuits, Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz
- IEC 61967-2: Measurement of radiated emissions – TEM-cell and wideband TEM-cell method

| Parameter | Test # | Conditions[1] | | Classification level[2] | Unit |
|---|---|---|---|---|---|
| | | Comm. modules[3] | GPIO | | |
| $V_{EME}$ | 1 | On | Off, input pull-up | L | dBµV |
| | 2 | On | Off, input pull-up | L | dBµV |
| | 3 | On | Off, input pull-up | L | dBµV |
| | 4 | On | Off, input pull-up | —[4] | dBµV |
| | 5 | On | Off, input pull-up | L | dBµV |
| | 6 | On | PG1[5] input, pull-up | L | dBµV |
| | 7 | Off | PG1[5] output high, half drive | L | dBµV |
| | 8 | Off | PG1[5] output high, full drive | L | dBµV |
| | 9 | Off | PG1[5] output low, half drive | L | dBµV |
| | 10 | Off | PG1[5] output low, full drive | L | dBµV |
| | 11 | Off | All I/O tri-stated | I | dBµV |
| | 12 | Off | PG2[6] toggle @ 5 kHz, half drive, SR off | L | dBµV |
| | 13 | Off | PG2[6] toggle @ 5 kHz, half drive, SR on | L | dBµV |
| | 14 | Off | PG2[6] toggle @ 5 kHz, full drive, SR off | L | dBµV |
| | 15 | Off | PG2[6] toggle @ 5 kHz, full drive, SR on | I | dBµV |

1. All tests ran with core and bus frequency at 200 MHz. Test #2 had "weak" FM modulation and Test #3 had "strong" FM modulation.
2. I = Class 1 (36 dBµV), L = Class 2 (24 dBµV), N = Class 3 (12 dBµV)
3. LINFlex0/1 running at 19.2 kbd, SPI0 running at 2.5 MHz, SPI1 running at 7.5 MHz, SPI2 running at 4.5 MHz, CAN0/1 running at 500 kbd
4. Test #4 values were slightly above class I level.
5. PG1 = port group 1: pins F[3:15]
6. PG2 = port group 2: pins A[2:4], C[11:14], D14, F12, G6, J8

Each of the tests ran once across each of the following frequency bands.

| Frequency band | RBW (kHz) | VBW (kHz) | Sweep time (ms/MHz) | Pre-amplifier | Detector |
|---|---|---|---|---|---|
| 150 kHz to 30 MHz | 9 | 30 | 5 | ON (–20 dB) | Peak-Average |
| 30 MHz to 1000 MHz | 120 | 300 | | | |

**Table 21. Current consumption characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | Frequency: 200MHz | | | | |
| | | $T_J$ = 165 °C<br>3.3 V supplies<br>Frequency: 200MHz | — | — | 1.8 | |
| $I_{DD\_HV\_FLA}$ | Operating current | $T_J$ = 150 °C<br>3.3 V supplies<br>Frequency: 200MHz | — | — | 5.5 | mA |
| | | $T_J$ = 165 °C<br>3.3 V supplies<br>Frequency: 200MHz | — | — | 7.0 | |

1. The content of the Conditions column identifies the components that draw the specific current.
2. Enabled modules: ADC0/1, FlexPWM0, eTimer0, two SPIs, two FlexCANs, FlexRay, one LINFlexD, DMA. At maximum frequency. I/O supply current excluded.
3. Internal structures hold the input voltage less than $V_{DD\_HV\_ADV}$ + 1.0 V on all pads powered by $V_{DDA}$ supplies, if the maximum injection current specification is met (3 mA for all pins) and $V_{DDA}$ is within the operating voltage specifications.
4. This value is the total current for two ADCs.

## 3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

**Table 22. Temperature sensor electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| — | Temperature monitoring range | — | –40 | — | 165 | °C |
| $T_{SENS}$ | Sensitivity | — | — | 5.18 | — | mV/°C |
| $T_{ACC}$ | Accuracy for linear temperature sensor | $T_J$ = –40 to 150 °C | –3 | — | +3 | °C |
| | | $T_J$ = 150 to 165 °C | –5 | — | +5 | |
| — | Accuracy for temperature-threshold digital flags | $T_J$ = –40 to 150 °C | –5 | — | +5 | °C |
| — | Temperature variation for each customer-adjustable trim step | $T_J$ = –40 to 150 °C | 0.4 | 0.7 | 1.0 | °C |
| — | Operating current | $T_J$ = –40 to 165 °C | — | — | 675 | µA |

## 3.12 Main oscillator electrical characteristics

This device provides a driver for the oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing EMI and power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between the crystal and the MCU.

# 3.16 Flash memory specifications

## 3.16.1 Maximum junction temperature 150°C

### 3.16.1.1 Flash memory program and erase specifications

**NOTE**

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 28 shows the estimated Program/Erase times.

**Table 28. Flash memory program and erase specifications**

| Symbol | Characteristic[1] | Typ[2] | Factory Programming[3, 4] | | Field Update | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Initial Max | Initial Max, Full Temp | Typical End of Life[5] | Lifetime Max[6] | | |
| | | | $20°C \le T_A \le 30°C$ | $-40°C \le T_J \le 150°C$ | $-40°C \le T_J \le 150°C$ | ≤ 1,000 cycles | ≤ 250,000 cycles | |
| $t_{dwpgm}$ | Doubleword (64 bits) program time | 43 | 100 | 150 | 55 | 500 | | µs |
| $t_{ppgm}$ | Page (256 bits) program time | 73 | 200 | 300 | 108 | 500 | | µs |
| $t_{qppgm}$ | Quad-page (1024 bits) program time | 268 | 800 | 1,200 | 396 | 2,000 | | µs |
| $t_{16kers}$ | 16 KB Block erase time | 168 | 290 | 320 | 250 | 1,000 | | ms |
| $t_{16kpgm}$ | 16 KB Block program time | 34 | 45 | 50 | 40 | 1,000 | | ms |
| $t_{32kers}$ | 32 KB Block erase time | 217 | 360 | 390 | 310 | 1,200 | | ms |
| $t_{32kpgm}$ | 32 KB Block program time | 69 | 100 | 110 | 90 | 1,200 | | ms |
| $t_{64kers}$ | 64 KB Block erase time | 315 | 490 | 590 | 420 | 1,600 | | ms |
| $t_{64kpgm}$ | 64 KB Block program time | 138 | 180 | 210 | 170 | 1,600 | | ms |
| $t_{256kers}$ | 256 KB Block erase time | 884 | 1,520 | 2,030 | 1,080 | 4,000 | — | ms |
| $t_{256kpgm}$ | 256 KB Block program time | 552 | 720 | 880 | 650 | 4,000 | — | ms |

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: $-40°C \le T_J \le 150°C$, full spec voltage.

**Table 33. Flash memory Array Integrity and Margin Read specifications (continued)**

| Symbol | Characteristic | Min | Typical | Max[1] | Units[2] |
|---|---|---|---|---|---|
| $t_{ai32kseq}$ | Array Integrity time for sequential sequence on 32KB block. | — | — | 1024 x Tperiod x Nread | — |
| $t_{ai64kseq}$ | Array Integrity time for sequential sequence on 64KB block. | — | — | 2048 x Tperiod x Nread | — |
| $t_{ai256kseq}$ | Array Integrity time for sequential sequence on 256KB block. | — | — | 8192 x Tperiod x Nread | — |
| $t_{mr16kseq}$ | Margin Read time for sequential sequence on 16KB block. | 73.81 | — | 110.7 | µs |
| $t_{mr32kseq}$ | Margin Read time for sequential sequence on 32KB block. | 128.43 | — | 192.6 | µs |
| $t_{mr64kseq}$ | Margin Read time for sequential sequence on 64KB block. | 237.65 | — | 356.5 | µs |
| $t_{mr256kseq}$ | Margin Read time for sequential sequence on 256KB block. | 893.01 | — | 1,339.5 | µs |

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

### 3.16.2.3 Flash memory module life specifications

**Table 34. Flash memory module life specifications**

| Symbol | Characteristic | Conditions | Min | Typical | Units |
|---|---|---|---|---|---|
| Array P/E cycles | Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1] | - | 250,000 | - | P/E cycles |
| | Number of program/erase cycles per block for 256 KB blocks.[2] | - | 1,000 | 250,000 | P/E cycles |
| Data retention | Minimum data retention. | Blocks with 0 - 1,000 P/E cycles. | 50 | - | Years |
| | | Blocks with 100,000 P/E cycles. | 20 | - | Years |
| | | Blocks with 250,000 P/E cycles. | 10 | - | Years |

1. Program and erase supported across standard temperature specs. Up to 10,000 program and erase cycles may be done between 150 °C and 165 °C out of the total specified number of cycles.
2. Program and erase supported across standard temperature specs.

### 3.16.2.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.

**Maximum junction temperature 165°C**

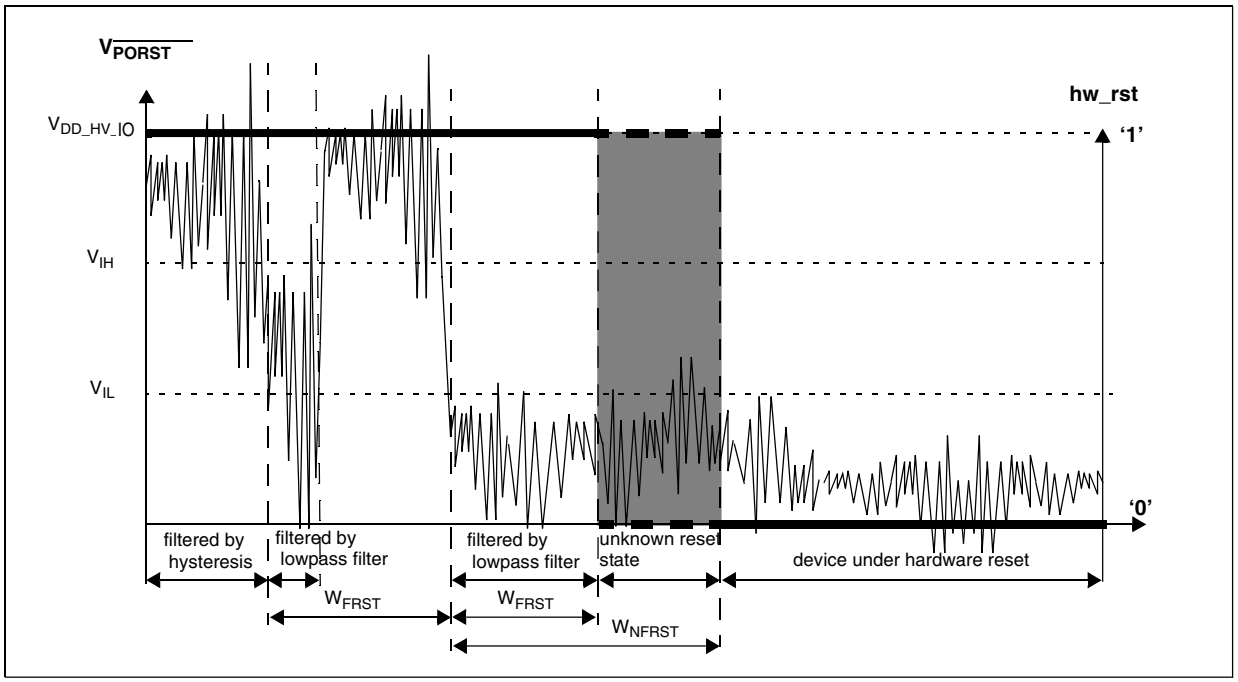



**Figure 10. Noise filtering on reset signal**

**Table 40. Reset ($\overline{RESET}$) electrical characteristics**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | Input high level TTL (Schmitt Trigger) | — | 2.0 | — | $V_{DD\_HV\_IO}$ + 0.4 | V |
| $V_{IL}$ | Input low level TTL (Schmitt Trigger) | — | –0.4 | — | 0.8 | V |
| $V_{HYS}$ | Input hysteresis TTL (Schmitt Trigger) | — | 300 | — | — | mV |
| $I_{OL\_R}$ | Strong pull-down current | Device under power-on reset<br>$V_{DD\_HV\_A}$=1.0 V<br>$V_{OL}$ = 0.35*$V_{DD\_HV\_IO}$ | 0.2 | — | — | mA |
| | | Device under power-on reset<br>$V_{DD\_HV\_IO}$=3.0 V<br>$V_{OL}$ = 0.35*$V_{DD\_HV\_IO}$ | 15 | — | — | mA |
| $W_{FRST}$ | ($\overline{RESET}$)-input filtered pulse | — | — | — | 500 | ns |
| $W_{NFRST}$ | ($\overline{RESET}$)-input not filtered pulse | — | 2 | — | — | µs |
| $\lvert I_{WPD} \rvert$ | Weak pull-down current absolute value | RESET pin<br>$V_{IN}$ = $V_{DD}$ | 30 | — | 80 | µA |

**Maximum junction temperature 165°C**

1. These specifications apply to JTAG boundary scan only.

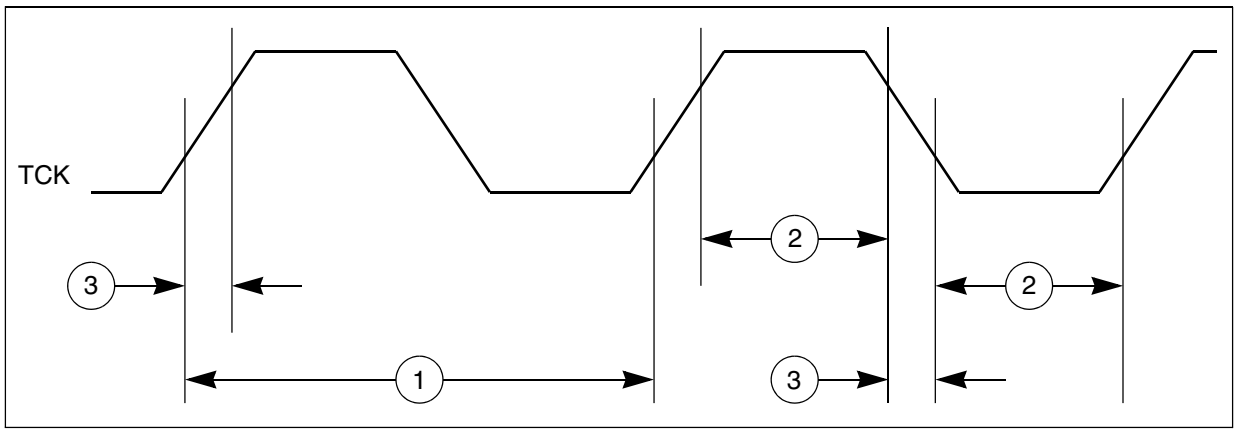



**Figure 11. JTAG test clock input timing**

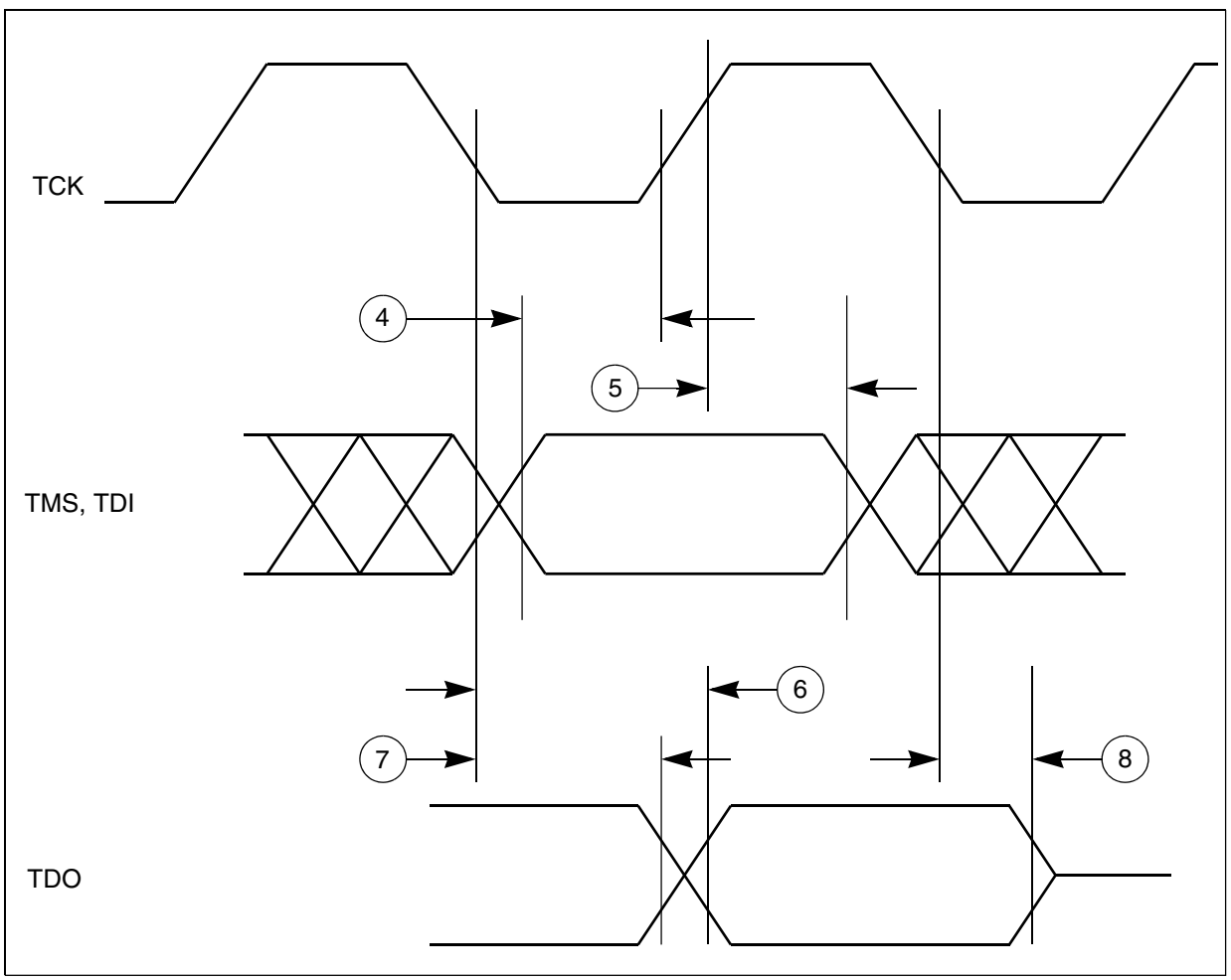



**Figure 12. JTAG test access port timing**

**Table 48. SPI timing (continued)**

| # | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | | Master (MTFE = 1, CPHA = 0) | –4 | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –4 | — | |

1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. P is the number of clock cycles added to delay the SPI input sample point and is software programmable.
3. $t_{SYS}$ is the period of the DSPI_CLKn clock, the input clock to the SPI module. Maximum frequency is 50 MHz (min $t_{SYS}$ = 20 ns).

**NOTE**

For numbers shown in the following figures, see Table 48.

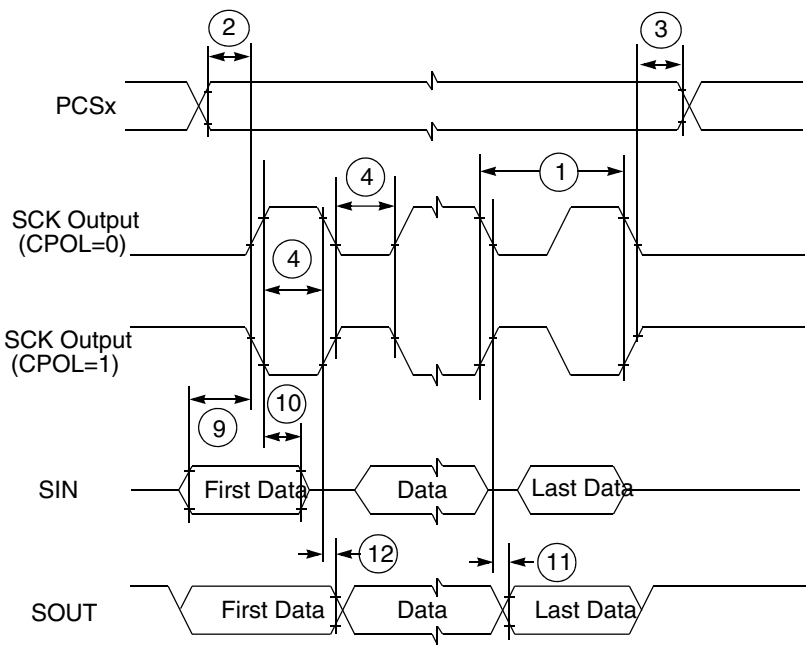



**Figure 21. DSPI classic SPI timing — master, CPHA = 0**

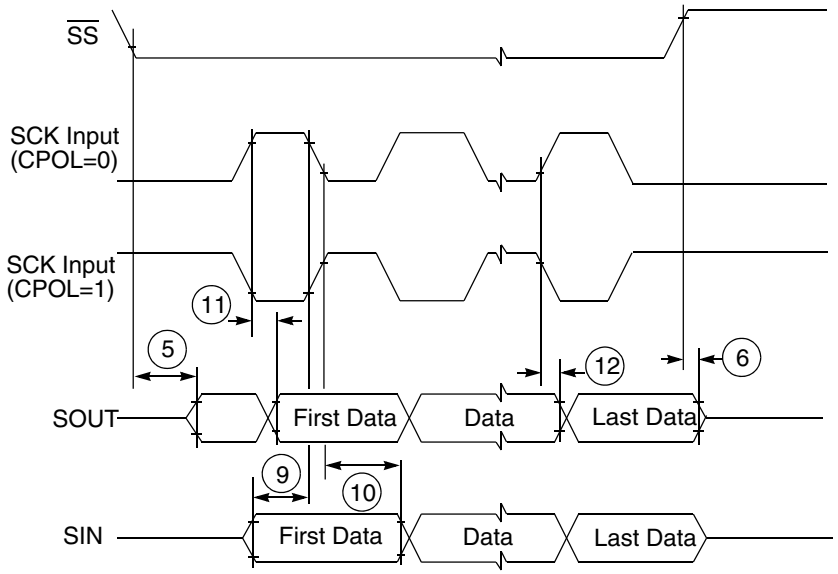



**Figure 28. DSPI modified transfer format timing — slave, CPHA = 1**

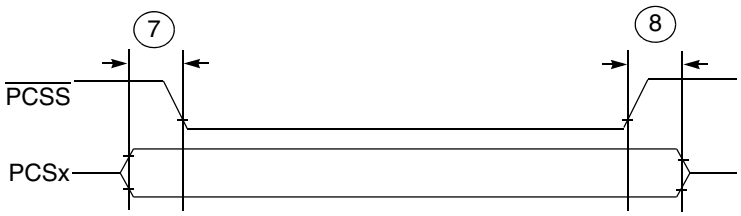



**Figure 29. DSPI PCS strobe (PCSS) timing**

## 3.19.6 LFAST

### 3.19.6.1 LFAST interface timing diagrams

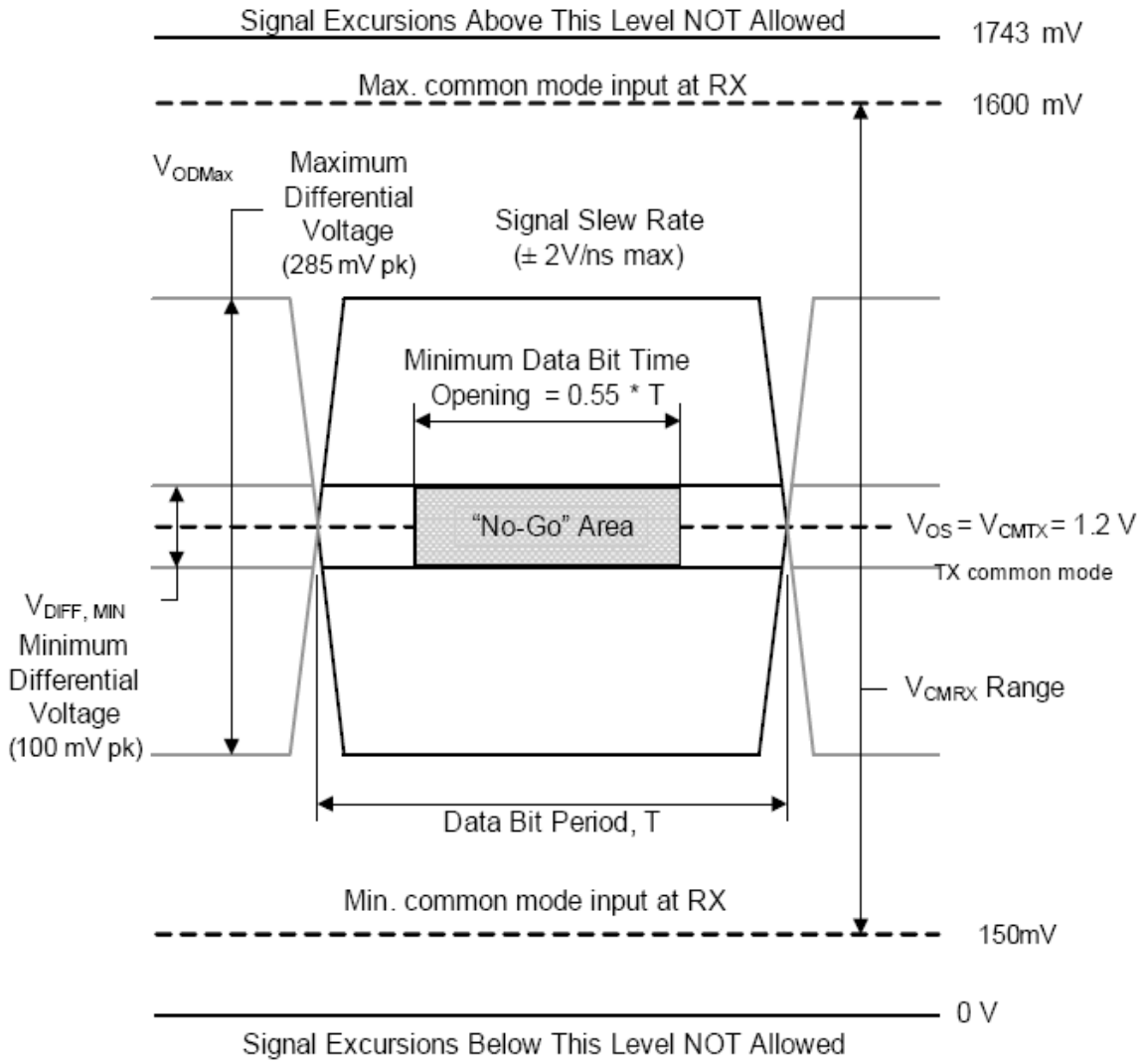
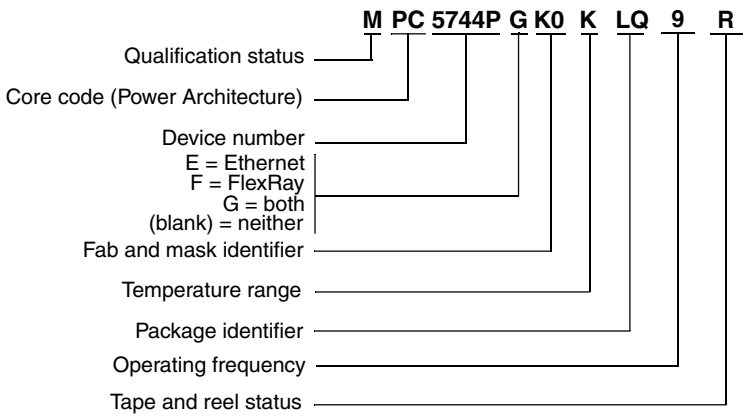



**Figure 30. LFAST timing definition**

# 5 Ordering information




| Temperature range | Package identifier | Operating frequency | Qualification status | Tape and reel status |
|---|---|---|---|---|
| M = –40°C to +125°C<br>K = –40°C to +135°C for extended temp (+165°C $T_J$) | LQ = 144 LQFP<br>MM = 257 MAPBGA | 9 = 200 MHz<br>8 = 180 MHz<br>5 = 150 MHz | P = Pre-qualification<br>M = Fully spec. qualified, general market flow<br>S = Fully spec. qualified, automotive flow | R = Tape and reel<br>(blank) = Trays |

**Note:** Not all options are available on all devices.

**Table 57. Orderable part number examples**

| Part number[1] | Flash/SRAM | Package | Other features |
|---|---|---|---|
| SPC5744PFK1MLQ9 | 2.5 MB/384 KB | 144 LQFP (Pb free) | -40 to +125 °C |
| SPC5744PGK1MMM9 | 2.5 MB/384 KB | 257 MAPBGA (Pb free) | Ethernet interface<br>LFAST interface<br>Nexus Aurora<br>-40 to +125 °C |
| SPC5743PFK1MLQ9 | 2 MB/256 KB | 144 LQFP (Pb free) | -40 to +125 °C |
| SPC5743PGK1MMM9 | 2 MB/256 KB | 257 MAPBGA (Pb free) | Ethernet interface<br>LFAST interface<br>Nexus Aurora<br>-40 to +125 °C |
| SPC5742PFK1MLQ9 | 1.5 MB/192 KB | 144 LQFP (Pb free) | -40 to +125 °C |
| SPC5742PGK1MMM9 | 1.5 MB/192 KB | 257 MAPBGA (Pb free) | Ethernet interface<br>LFAST interface<br>Nexus Aurora<br>-40 to +125 °C |
| SPC5741PFK1MLQ9 | 1 MB/128 KB | 144 LQFP (Pb free) | -40 to +125 °C |
| SPC5741PGK1MMM9 | 1 MB/128 KB | 257 MAPBGA (Pb free) | Ethernet interface<br>LFAST interface<br>Nexus Aurora<br>-40 to +125 °C |