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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	79
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pk1amlq8

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1 Introduction

1.1 Features

The following table summarizes the features of the MPC5744P.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution speed	0 MHz to 200 MHz (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory—see Table 2 for additional details	
Code/data flash memory	**2.5 MB**, ECC, RWW
Data flash memory	Supported with RWW
SRAM	**384 KB**, ECC
Overlay access to SRAM from Flash Memory Controller	Yes
Modules	
Interrupt controller	32 interrupt priority levels, 16 SW programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules

Table continues on the next page...

Table 2. Flash memory and SRAM sizes of MPC5744P, MPC5743P, MPC5742P, and MPC5741P

Part number	Flash memory	SRAM
MPC5744P	2.5 MB	384 KB
MPC5743P	2.0 MB	256 KB
MPC5742P	1.5 MB	192 KB
MPC5741P	1.0 MB	128 KB

1.2 Block Diagram

The following figure is a top-level diagram that shows the functional organization of the system.

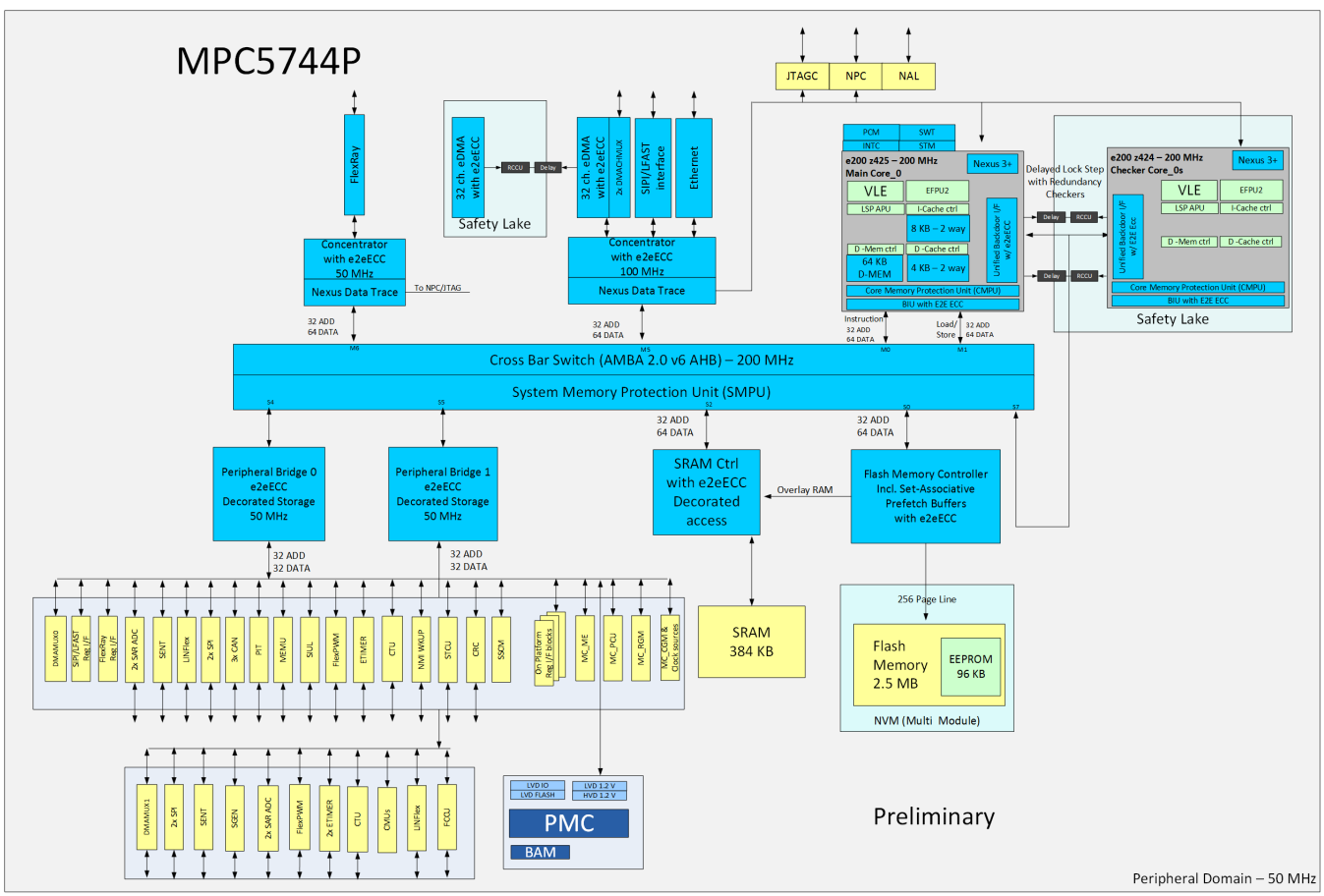

Figure 1. System Block Diagram

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	Type	Description	144LQFP	257MAPBGA
				L6
				L12
				M6
				M7
				M8
				M9
				M10
				M11
				M12
$V_{SS\_LV\_COR}$	Ground	Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144LQFP (pin 35).	17	B1
			35	G7
			40	G8
			71	G9
			94	G10
			96	G11
			132	H7
			137	H8
				H9
				H10
				H11
				J7
				J8
				J9
				J10
				J11
				K7
				K8
				K9
				K10
				K11
				L7
				L8
				L9
				L10
				L11
$V_{DD\_LV\_PLL}$	Power	PLL low voltage Supply	36	P4
$V_{SS\_LV\_PLL}$	Ground	PLL low voltage Ground	35	N4

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0011-1111	—	Reserved	—	—		
	IMCR[48]	0001	SCK	DSPI2	DSPI 2 Input Serial Clock	I		
	IMCR[59]	0010	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I		
	IMCR[173]	0001	REQ0	SIUL2	SIUL2 External Interrupt 0	I		
A[1]	MSCR[1]	0000 (Default)	GPIO[1]	SIUL2-GPIO[1]	General Purpose IO A[1]	I/O	74	T14
		0001	ETC1	eTimer_0	eTimer_0 Input/Output Data Channel 1	I/O		
		0010	SOUT	DSPI2	DSPI 2 Serial Data Out	O		
		0011-1111	—	Reserved	—	—		
	IMCR[60]	0010	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I		
	IMCR[174]	0001	REQ1	SIUL2	SIUL2 External Interrupt Source 1	I		
A[2]	MSCR[2]	0000 (Default)	GPIO[2]	SIUL2-GPIO[2]	General Purpose IO A[2]	I/O	84	L14
		0001	ETC2	eTimer_0	eTimer_0 Input/Output Data Channel 2	I/O		
		0010	—	Reserved	—	—		
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[169]	0000 (Default)	ABS0	MC_RGM	RGM external boot mode 1	I		
	IMCR[47]	0010	SIN	DSPI2	DSPI 2 Serial Data Input	I		
	IMCR[61]	0010	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I		
	IMCR[97]	0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I		
	IMCR[175]	0001	REQ2	SIUL2	SIUL2 External Interrupt Source 2	I		
A[3]	MSCR[3]	0000 (Default)	GPIO[3]	SIUL2-GPIO[3]	General Purpose IO A[3]	I/O	92	G15
		0001	ETC3	eTimer_0	eTimer_0 Input/Output Data Channel 3	I/O		
		0010	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[171]	0000 (Default)	ABS2	MC_RGM	RGM external boot mode 2	I		
	IMCR[62]	0010	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[199]	0001	REQ26	SIUL2	SIUL2 External Interrupt Source 26	I		
E[15]	MSCR[79]	0000 (Default)	GPIO[79]	SIUL2-GPIO[79]	General Purpose IO E[15]	I/O	121	C8
		0001	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O		
		0010	—	Reserved	—	—		
		0011	TIMER1	ENET_0	Ethernet TIMER Outputs (Output Compare Events)	O		
		0100-1111	—	Reserved	—	—		
	IMCR[50]	0100	SIN	DSPI3	DSPI 3 Serial Data Input	I		
	IMCR[200]	0001	REQ27	SIUL2	SIUL2 External Interrupt Source 27	I		
F[0]	MSCR[80]	0000 (Default)	GPIO[80]	SIUL2-GPIO[80]	General Purpose IO F[0]	I/O	133	B6
		0001	A1	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 1	I/O		
		0010	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	O		
		0011	MDC	ENET_0	Ethernet MDIO clock output	O		
		0100-1111	—	Reserved	—	—		
	IMCR[61]	0001	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I		
	IMCR[91]	0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input 1	I		
	IMCR[201]	0001	REQ28	SIUL2	SIUL2 External Interrupt Source 28	I		
F[3]	MSCR[83]	0000 (Default)	GPIO[83]	SIUL2-GPIO[83]	General Purpose IO F[3]	I/O	139	B3
		0001	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O		
		0010	—	Reserved	—	—		
		0011	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0100	TIMER2	ENET_0	Ethernet TIMER Outputs 2 (Output Compare Events)	O		
		0101-1111	—	Reserved	—	—		
F[4]	MSCR[84]	0000 (Default)	GPIO[84]	SIUL2-GPIO[84]	General Purpose IO F[4]	I/O	4	E1
		0001	—	Reserved	—	O		
		0010	MDO[3]	NPC_WRAPPER	Nexus - Message Data Out Pin 3	O		
		0011	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
F[11]	MSCR[91]	0000 (Default)	GPIO[91]	SIUL2-GPIO[91]	General Purpose IO F[11]	I/O	25	L2
		0001	—	Reserved	—	—		
		0010	EVTI_IN	NPC_WRAPPER	Nexus Event In Pin	I		
		0011-1111	—	Reserved	—	—		
F[12]	MSCR[92]	0000 (Default)	GPIO[92]	SIUL2-GPIO[92]	General Purpose IO F[12]	I/O	106	D17
		0001	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O		
		0010-0011	—	Reserved	—	—		
		0100	A1	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 1	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[68]	0011	ETC3	eTimer_1	eTimer_1 Input Data Channel 3	I		
	IMCR[109]	0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I		
	IMCR[203]	0001	REQ30	SIUL2	SIUL2 External Interrupt Source 30	I		
F[13]	MSCR[93]	0000 (Default)	GPIO[93]	SIUL2-GPIO[93]	General Purpose IO F[13]	I/O	112	A15
		0001	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O		
		0010-0011	—	Reserved	—	—		
		0100	B1	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 1	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[69]	0100	ETC4	eTimer_1	eTimer_1 Input Data Channel 4	I		
	IMCR[110]	0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I		
	IMCR[204]	0001	REQ31	SIUL2	SIUL2 External Interrupt Source 31	I		
F[14]	MSCR[94]	0000 (Default)	GPIO[94]	SIUL2-GPIO[94]	General Purpose IO F[14]	I/O	115	D12
		0001	TXD	LIN1	LINFlexD 1 Transmit Pin	O		
		0010	TXD	CAN2	CAN 2 Transmit Pin	O		
		0011-1111	—	Reserved	—	—		
F[15]	MSCR[95]	0000 (Default)	GPIO[95]	SIUL2-GPIO[95]	General Purpose IO F[15]	I/O	113	A13
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[166]	0011	RXD	LIN1	LIN1 RXD	I		
	IMCR[34]	0001	RXD	CAN2	CAN2 RXD	I		

Table continues on the next page...

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[11]	MSCR[107]	0000 (Default)	GPIO[107]	SIUL2-GPIO[107]	General Purpose IO G[11]	I/O	75	T15
		0001	FR_DBG[3]	FLEXRAY	FlexRay Debug Strobe Signal 3	O		
		0010	—	Reserved	—	—		
		0011	TX_D3	ENET_0	Ethernet MII/RMII transmit data 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0011	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		
	IMCR[214]	0100	SENT_RX[1]	SENT_1	SENT 1 Receiver channel 1	I		
H[4]	MSCR[116]	0000 (Default)	GPIO[116]	SIUL2-GPIO[116]	General Purpose IO H[4]	I/O		F4
		0001	X0	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 0	I/O		
		0010	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[71]	0001	ETC0	eTimer_2	eTimer_2 Input Data Channel 0	I		
	IMCR[231]	0001	CRS	ENET_0	Ethernet MII Carrier Sense	I		
H[5]	MSCR[117]	0000 (Default)	GPIO[117]	SIUL2-GPIO[117]	General Purpose IO H[5]	I/O		F3
		0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[105]	0010	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I		
	IMCR[230]	0001	COL	ENET_0	Ethernet MII Collision	I		
H[6]	MSCR[118]	0000 (Default)	GPIO[118]	SIUL2-GPIO[118]	General Purpose IO H[6]	I/O		C13
		0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[106]	0010	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I		
H[7]	MSCR[119]	0000 (Default)	GPIO[119]	SIUL2-GPIO[119]	General Purpose IO H[7]	I/O		F2
		0001	X1	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 1	I/O		

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0001	I/O-Pad	C[5]
			0010	I/O-Pad	D[8]
			0011	I/O-Pad	G[11]
			0100-1111	—	Reserved
FlexPWM_0	EXT_SYNC	IMCR[87]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved
FlexPWM_0	A0	IMCR[88]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010	I/O-Pad	D[10]
			0011-1111	—	Reserved
FlexPWM_0	B0	IMCR[89]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010	I/O-Pad	D[11]
			0011-1111	—	Reserved
FlexPWM_0	A1	IMCR[91]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[7]
			0010	I/O-Pad	C[15]
			0011	I/O-Pad	F[0]
			0100-1111	—	Reserved
FlexPWM_0	B1	IMCR[92]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[6]
			0010	I/O-Pad	D[0]
			0011	I/O-Pad	D[14]
			0100-1111	—	Reserved
FlexPWM_0	X1	IMCR[93]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[4]
			0010	I/O-Pad	D[12]
			0011-1111	—	Reserved
FlexPWM_0	A2	IMCR[94]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[11]
			0010	I/O-Pad	A[12]
			0011	I/O-Pad	G[3]
			0100-1111	—	Reserved
FlexPWM_0	B2	IMCR[95]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[12]
			0010	I/O-Pad	A[13]
			0011	I/O-Pad	G[4]

Table continues on the next page...

- High voltage detector (HVD_CORE_BK) for the self-test of HVD_CORE
- Power on Reset (POR)

NOTE

When the external regulator mode is used either the EXT_POR_B signal needs to be driven by external circuitry until all power supplies are in recommended ranges or the internal LVDs keep the device in POR until all power supply are in recommended range. There needs to be used the external over voltage detectors for all power supplies in both regulator modes for safety operation.

The following bipolar transistor is supported:

- ON Semiconductor™ NJD2873 (requires a heat sink to operate up to 165 °C): See Table 16.

Table 16. Recommended operating characteristics: NJD2873

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Minimum peak collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_c	Minimum voltage at transistor collector	2.5	V

Table 17. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ld}	External decoupling / stability capacitor	Min value granted with respect to tolerance, voltage, temperature, and aging variations. 4 capacitors are recommended – one for each side of the chip.	4	—	18.8	µF
—	Combined ESR of external capacitor	—	0.03	—	0.15	Ω
t_{SU}	Start-up time after main supply stabilization	C_{ld} = 4 µF	—	—	2.5	ms
L_{bw}	Bonding inductance	—	—	—	13	nH
R_{bw}	Bonding wire and pad resistance	—	—	—	0.5	Ω
R_{sd}	Series resistance of on-chip power grid	—	—	—	0.1	Ω

Table continues on the next page...

Table 18. FlexRay (SYM) configuration output buffer electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
F_{max_Y}	Output frequency SYM configuration	C_L = 20 pF, $V_{DD\_HV\_IO}$=3.3 V –5%, +10%	—	—	50	MHz
T_{tr_Y}	Transition time output pin SYM configuration	C_L = 20 pF, $V_{DD\_HV\_IO}$=3.3 V –5%, +10%	1	—	6	ns
$\lvert T_{skew\_Y} \rvert$	Difference between rise and fall time	—	0	—	1	ns

1. $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 165 °C, unless otherwise specified.

NOTE

See the LFAST section for parameters dedicated to this interface.

Table 19. LFAST output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$\lvert \Delta_{VO\_L} \rvert$	Absolute value for differential output voltage swing (terminated)	—	100	200	285	mV
V_{ICOM_L}	Common mode voltage	—	1.08	1.2	1.32	V
T_{tr_L}	Transition time output pin LVDS configuration	—	0.2	—	1.5	ns

1. $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 165 °C, unless otherwise specified.

NOTE

Fast IOs must be specified only as fast (and not as high current). See Table 20.

Table 20. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DD_LV}	LV (core) Supply Voltage	—	1.19	—	1.32	V
$V_{DD\_HV\_IO}$[1]	I/O Supply Voltage	—	3.15	—	3.6	V
V_{IH}	CMOS Input Buffer High Voltage (with hysteresis disabled)	—	0.55 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	—	Vss - 0.3	—	0.40 * $V_{DD\_HV\_IO}$	V
V_{HYS}	CMOS Input Buffer Hysteresis	—	0.1 * $V_{DD\_HV\_IO}$	—	—	V
Pull_I_{OH}	Weak Pullup Current[2]	—	10	—	80	µA
Pull_I_{OL}	Weak Pulldown Current[3]	—	10	—	80	µA

Table continues on the next page...

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	90	230	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	120	310	
$I_{DD\_LV\_HALT}$	Operating current in V_{DD} HALT mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	25	40	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	110	300	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	140	400	
$I_{DD\_LV\_LFAST}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.6	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.8	
$I_{DD\_LV\_NEXUS}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.1	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.5	
$I_{DD\_HV\_ADV}$[3]	Operating current	T_J = 150 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.4	4.2	mA
		T_J = 165 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.5	4.5	
$I_{DD\_HV\_ADRE}$'[4]	Operating current	T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.20	0.28	mA
		T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.32	0.50	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.24	0.40	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.40	0.70	
$I_{DD\_HV\_OSC}$	Operating current	T_J = 150 °C 3.3 V supplies	—	—	1.6	mA

Table continues on the next page...

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		Frequency: 200MHz				
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	1.8	
$I_{DD\_HV\_FLA}$	Operating current	T_J = 150 °C 3.3 V supplies Frequency: 200MHz	—	—	5.5	mA
		T_J = 165 °C 3.3 V supplies Frequency: 200MHz	—	—	7.0	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Enabled modules: ADC0/1, FlexPWM0, eTimer0, two SPIs, two FlexCANs, FlexRay, one LINFlexD, DMA. At maximum frequency. I/O supply current excluded.
3. Internal structures hold the input voltage less than $V_{DD\_HV\_ADV}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
4. This value is the total current for two ADCs.

3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 22. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range	—	–40	—	165	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy for linear temperature sensor	T_J = –40 to 150 °C	–3	—	+3	°C
		T_J = 150 to 165 °C	–5	—	+5	
—	Accuracy for temperature-threshold digital flags	T_J = –40 to 150 °C	–5	—	+5	°C
—	Temperature variation for each customer-adjustable trim step	T_J = –40 to 150 °C	0.4	0.7	1.0	°C
—	Operating current	T_J = –40 to 165 °C	—	—	675	µA

3.12 Main oscillator electrical characteristics

This device provides a driver for the oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing EMI and power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between the crystal and the MCU.

Table 26. Internal RC Oscillator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
δf_{var}	IRC frequency variation with temperature and voltage compensation	T_J < 150 °C	-3	—	3	%
		T_J < 165 °C	-4	—	4	
δf_{var_noT}[1]	IRC frequency variation without temperature compensation (only voltage compensation)	T_J < 150 °C	–8	—	8	%
		T_J < 165 °C	–10	—	10	
$T_{startup}$	Startup time without temperature compensation	—	—	—	5	µs
I_{VDD3}	Current consumption on 3.3 V power supply	After $T_{startup}$	—	—	55	µA
I_{VDD12}	Current consumption on 1.2 V power supply	After $T_{startup}$	—	—	270	µA

1. The typical user trim step size (dfTRIM) is +48kHz for frequencies trimmed above nominal and -40kHz for frequencies trimmed below nominal based on characterization results.

3.15 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

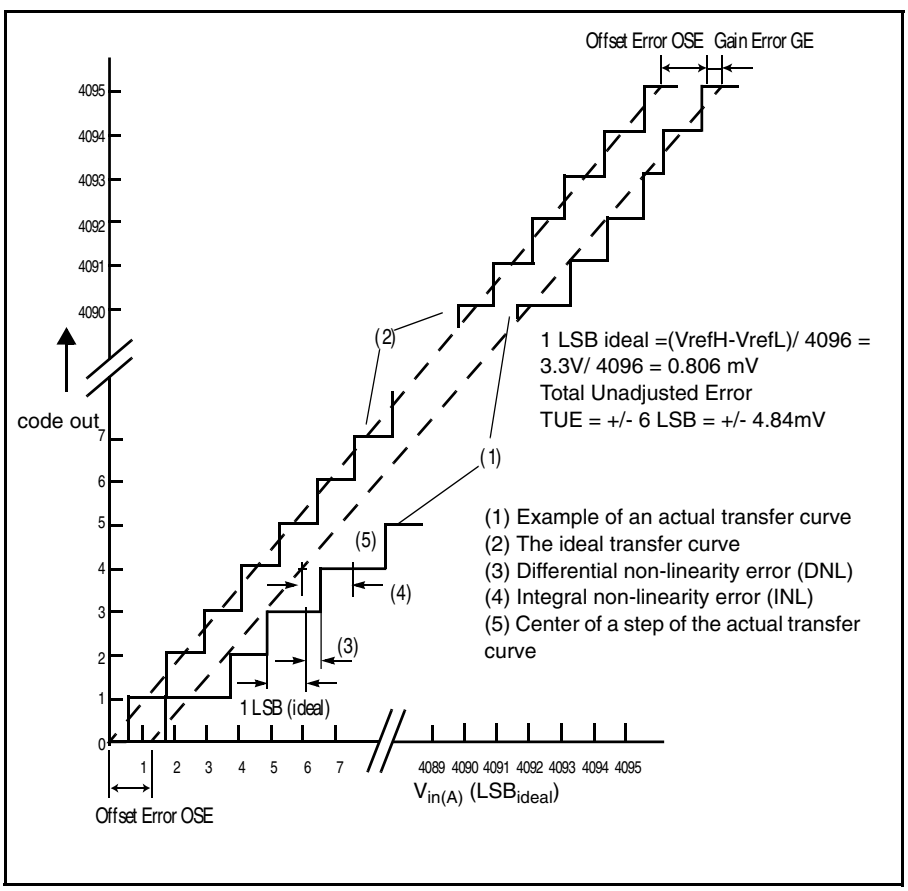

Figure 7. ADC characteristics and error definitions

Table 27. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
Input (single ADC channel)	Max leakage	150 °C	—	—	250	nA
	Max positive/negative injection	—	–3	—	3	mA
Input (double ADC channel)	Max leakage	150 °C	—	—	300	nA
	Max positive/negative injection	$\lvert V_{REF\_AD0} - V_{REF\_AD1} \rvert$ < 150mV	–3.6	—	3.6	mA
SNR	Signal-to-noise ratio	V_{REF} = 3.3 V, Fin < 125kHz	67	—	—	dB
SNR[7]	Signal-to-noise ratio	V_{REF} = 5.0 V, Fin < 125kHz	69	—	—	dB
THD	Total harmonic distortion	Fin ≤ 125 kHz	65	70	—	dB
ENOB	Effective number of bits	Fin < 125 kHz	10.5	—	—	bits
SINAD	Signal-to-noise and distortion	See ENOB	(6.02 * ENOB) + 1.76			dB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ (single ADC channels)	Current injection: ±3 mA for each channel, max 3 channels	–8	—	8	LSB

1. $V_{DD\_HV\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to +165 °C, unless otherwise specified, and analog input voltage from V_{AGND} to V_{AREF}
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 2.
6. For the 144-pin package.
7. Test conditions have an influence on the achieved performance. Please contact FSL personnel to share the conditions for these results.

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

3.19.3.2 Nexus timing

Table 44. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	t_{TCYC}
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	t_{MCYC}
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

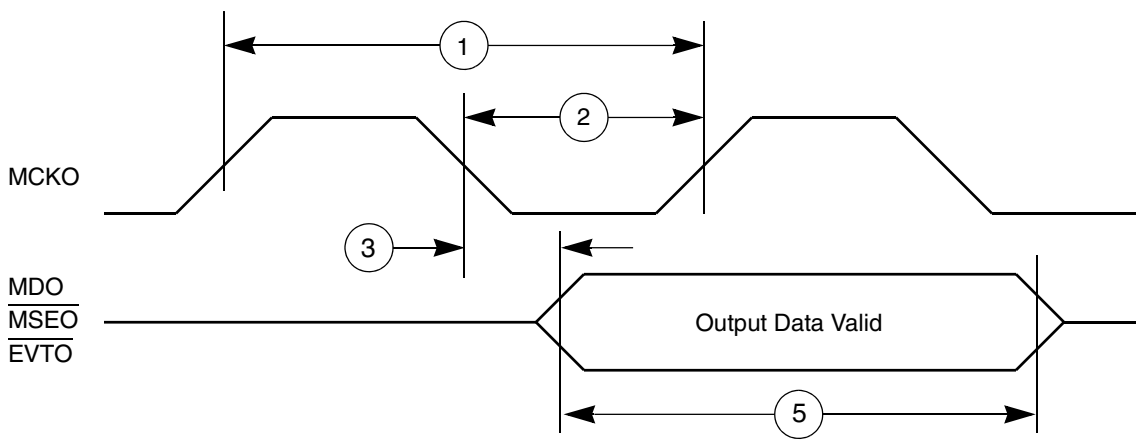

Figure 15. Nexus output timing

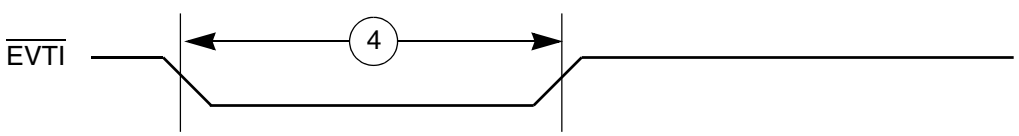

Figure 16. Nexus EVTI Input Pulse Width

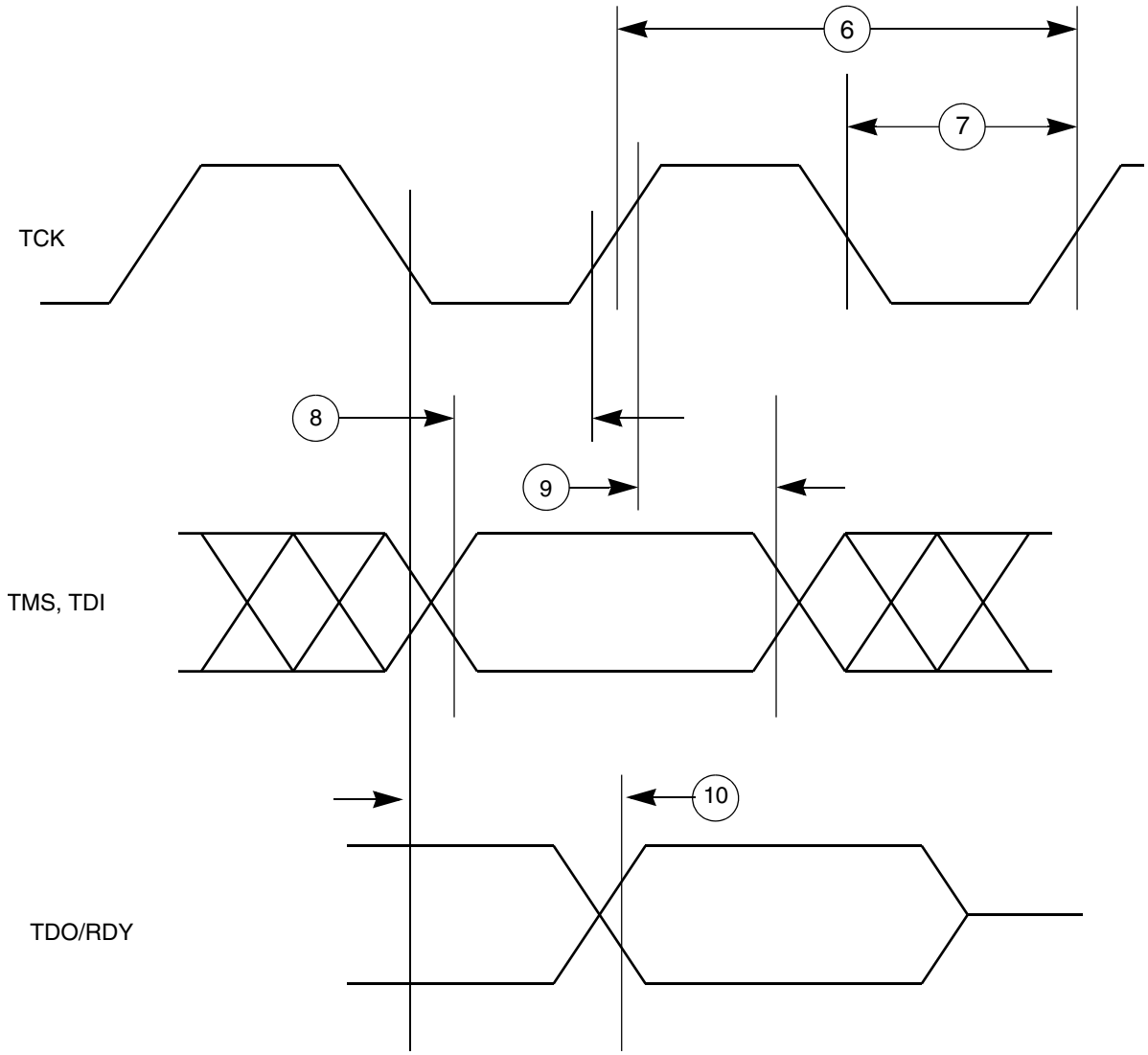

Figure 17. Nexus TDI, TMS, TDO timing

3.19.3.3 Aurora LVDS driver electrical characteristics

Table 45. Aurora LVDS driver electrical characteristics

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
Data Rate					
DATARATE	Data rate	—	1250	Typ+0.1%	Mbps
STARTUP					
T_{STRT_BIAS}	Bias startup time[2]	—	—	5	µs
T_{STRT_TX}	Transmitter startup time[3]	—	—	5	µs
T_{STRT_RX}	Receiver startup time[4]	—	—	4	µs

1. Conditions for these values are $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.

Table 48. SPI timing (continued)

#	Symbol	Parameter	Conditions	Min	Max	Unit
			Master (MTFE = 1, CPHA = 0)	–4	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. P is the number of clock cycles added to delay the SPI input sample point and is software programmable.
3. t_{SYS} is the period of the DSPI_CLKn clock, the input clock to the SPI module. Maximum frequency is 50 MHz (min t_{SYS} = 20 ns).

NOTE

For numbers shown in the following figures, see Table 48.

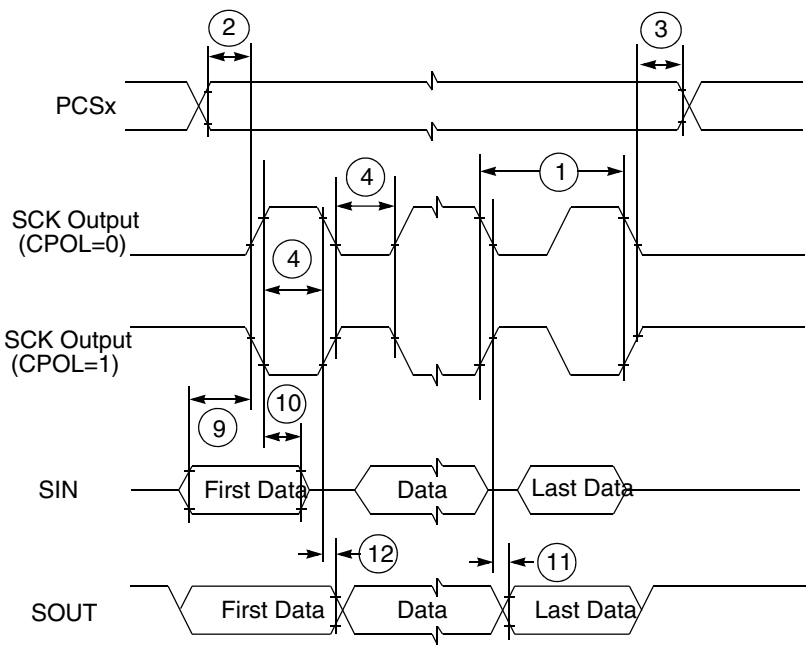

Figure 21. DSPI classic SPI timing — master, CPHA = 0

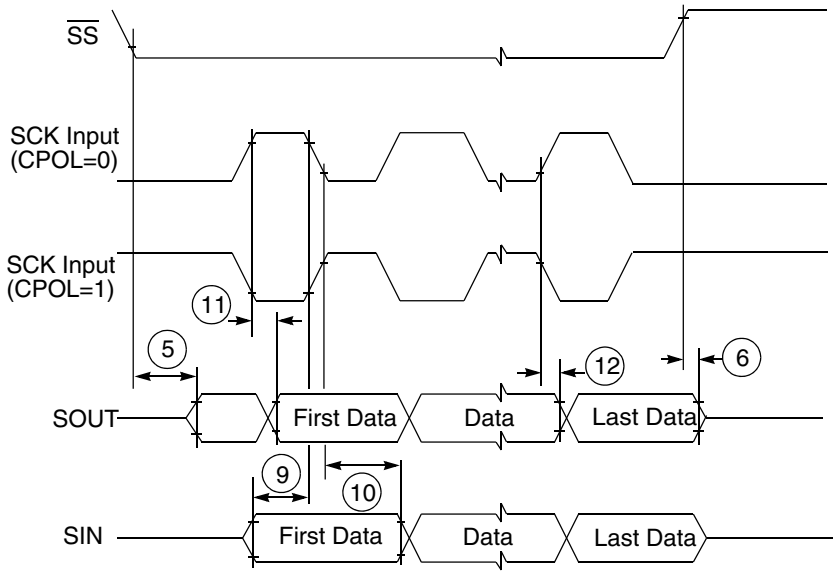

Figure 28. DSPI modified transfer format timing — slave, CPHA = 1

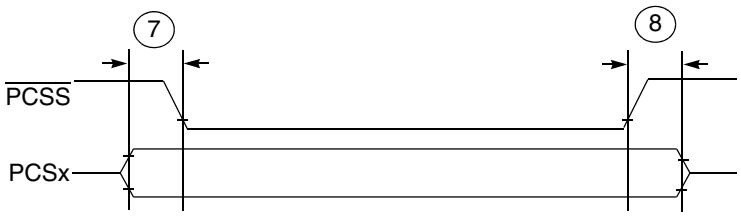

Figure 29. DSPI PCS strobe (PCSS) timing

3.19.6 LFAST

Table 51. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C, TxEN pin load maximum 25 pF

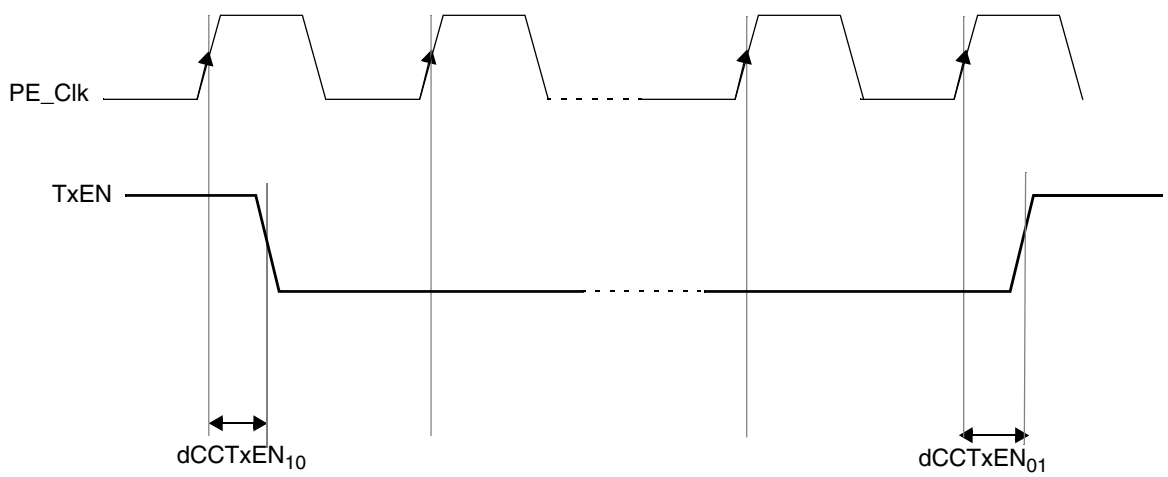

Figure 34. FlexRay TxEN signal propagation delays