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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	79
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pk1amlq8r

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[49]	0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I		
	IMCR[98]	0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I		
A[4]	MSCR[4]	0000 (Default)	GPIO[4]	SIUL2-GPIO[4]	General Purpose IO A[4]	I/O	108	D16
		0001	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O		
		0010	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O		
		0011	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O		
		0100	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[112]	0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I		
	IMCR[177]	0001	REQ4	SIUL2	SIUL2 External Interrupt Source 4	I		
	IMCR[172]	0000 (Default)	FAB	MC_RGM	RGM Force Alternate Boot Mode	I		
	IMCR[65]	0001	ETC0	eTimer_1	eTimer_1 Input Data Channel 0	I		
	IMCR[63]	0011	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
A[5]	MSCR[5]	0000 (Default)	GPIO[5]	SIUL2-GPIO[5]	General Purpose IO A[5]	I/O	14	H4
		0001	CS0	DSPI1	DSPI 1 Peripheral Chip Select 0	I/O		
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[70]	0001	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[178]	0001	REQ5	SIUL2	SIUL2 External Interrupt Source 5	I		
A[6]	MSCR[6]	0000 (Default)	GPIO[6]	SIUL2-GPIO[6]	General Purpose IO A[6]	I/O	2	D1
		0001	SCK	DSPI1	DSPI 1 Input/Output Serial Clock	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
	IMCR[63]	0001	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
	IMCR[192]	0001	REQ19	SIUL2	SIUL2 External Interrupt Source 19	I		
B[15]	MSCR[31]	0000 (Default)	GPI[31][4] ADC1_AN[2]	SIUL2-GPI[31]	General Purpose Input B[15]	I	62	R11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
	IMCR[193]	0001	REQ20	SIUL2	SIUL2 External Interrupt Source 20	I		
C[0]	MSCR[32]	0000 (Default)	GPI[32][4] ADC1_AN[3]	SIUL2-GPI[32]	General Purpose Input C[0]	I	66	R12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[1]	MSCR[33]	0000 (Default)	GPI[33][4] ADC0_AN[2]	SIUL2-GPI[33]	General Purpose Input C[1]	I	41	T4
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[2]	MSCR[34]	0000 (Default)	GPI[34][4] ADC0_AN[3]	SIUL2-GPI[34]	General Purpose Input C[2]	I	45	U5
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
C[4]	MSCR[36]	0000 (Default)	GPIO[36]	SIUL2-GPIO[36]	General Purpose IO C[4]	I/O	11	H3
		0001	CS0	DSPI0	DSPI 0 Peripheral Chip Select 0	I/O		
		0010	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0011	DEBUG4	SSCM	SSCM Debug Output 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[93]	0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input 1	I		
	IMCR[195]	0001	REQ22	SIUL2	SIUL2 External Interrupt Source 22	I		
C[5]	MSCR[37]	0000 (Default)	GPIO[37]	SIUL2-GPIO[37]	General Purpose IO C[5]	I/O	13	G3
		0001	SCK	DSPI0	DSPI 0 Input/Output Serial Clock	I/O		
		0010	—	Reserved	—	—		
		0011	DEBUG5	SSCM	SSCM Debug Output 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0001	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0011-1111	—	Reserved	—	—		
D[10]	MSCR[58]	0000 (Default)	GPIO[58]	SIUL2-GPIO[58]	General Purpose IO D[10]	I/O	76	R16
		0001	A0	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	TX_D2	ENET_0	Ethernet MII transmit data	O		
		0100	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	I/O		
		0110-1111	—	Reserved	—	—		
	IMCR[52]	0010	CS0	DSPI3	DSPI 3 Peripheral chip Select 0	I		
	IMCR[59]	0001	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I		
	IMCR[88]	0010	A0	FlexPWM_0	FlexPWM_0 Channel A Input 0	I		
D[11]	MSCR[59]	0000 (Default)	GPIO[59]	SIUL2-GPIO[59]	General Purpose IO D[11]	I/O	78	P17
		0001	B0	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O		
		0100	SCK	DSPI3	DSPI 3 Input/Output Serial Clock	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0010	SCK	DSPI3	DSPI 3 Input Serial Clock	I		
	IMCR[60]	0001	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I		
	IMCR[89]	0010	B0	FlexPWM_0	FlexPWM_0 Channel B Input 0	I		
D[12]	MSCR[60]	0000 (Default)	GPIO[60]	SIUL2-GPIO[60]	General Purpose IO D[12]	I/O	99	F15
		0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 1	I/O		
		0010	CS6	DSPI1	DSPI 1 Peripheral Chip Select 6	O		
		0011	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O		
		0100	SOUT	DSPI3	DSPI 3 Serial Data Output	O		
		0101-1111	—	Reserved	—	—		
	IMCR[93]	0010	X1	FlexPWM_0	FlexPWM_0 Channel X Input 1	I		
	IMCR[166]	0010	RXD	LIN1	LIN 1 Receive Pin	I		
D[14]	MSCR[62]	0000 (Default)	GPIO[62]	SIUL2-GPIO[62]	General Purpose IO D[14]	I/O	105	E17

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[2]	MSCR[98]	0000 (Default)	GPIO[98]	SIUL2-GPIO[98]	General Purpose IO G[2]	I/O	102	F17
		0001	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 2	I/O		
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O		
		0011-1111	—	Reserved	—	—		
	IMCR[96]	0010	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input 2	I		
G[3]	MSCR[99]	0000 (Default)	GPIO[99]	SIUL2-GPIO[99]	General Purpose IO G[3]	I/O	104	E16
		0001	A2	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[63]	0010	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I		
	IMCR[94]	0011	A2	FlexPWM_0	FlexPWM_0 Channel A Input 2	I		
G[4]	MSCR[100]	0000 (Default)	GPIO[100]	SIUL2-GPIO[100]	General Purpose IO G[4]	I/O	100	F16
		0001	B2	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[64]	0010	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I		
	IMCR[95]	0011	B2	FlexPWM_0	FlexPWM_0 Channel B Input 2	I		
G[5]	MSCR[101]	0000 (Default)	GPIO[101]	SIUL2-GPIO[101]	General Purpose IO G[5]	I/O	85	M17
		0001	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/ Output 3	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	TX_EN	ENET_0	Ethernet Transmit Data Valid	O		
		0100-1111	—	Reserved	—	—		
	IMCR[99]	0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input 3	I		
G[6]	MSCR[102]	0000 (Default)	GPIO[102]	SIUL2-GPIO[102]	General Purpose IO G[6]	I/O	98	G17
		0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input/ Output 3	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[97]	0100	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I		
G[7][5]	MSCR[103]	0000 (Default)	GPIO[103]	SIUL2-GPIO[103]	General Purpose IO G[7][9]	I/O	83	M16
		0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0010	—	Reserved	—	—		
		0011	LFAST_RXP	LFAST	SIPI/LFAST LVDS receive positive terminal	I		
		0100-1111	—	Reserved	—	—		
	IMCR[98]	0100	B3	FlexPWM_0	FlexPWM_0 Channel B Input 3	I		
G[8]	MSCR[104]	0000 (Default)	GPIO[104]	SIUL2-GPIO[104]	General Purpose IO G[8]	I/O	81	N14
		0001	FR_DBG[0]	FLEXRAY	FlexRay Debug Strobe Signal 0	O		
		0010	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O		
		0011	RMII_CLK	ENET_0	Ethernet RMII Clock (used in MII to RMII Gaskets)	O		
		0100-1111	—	Reserved	—	—		
	IMCR[83]	0011	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I		
	IMCR[194]	0001	REQ21	SIUL2	SIUL2 External Interrupt Source 21	I		
	IMCR[205]	0011	SENT_RX[0]	SENT_0	SENT 0 Receiver channel 0	I		
	IMCR[233]	0001	TX_CLK	ENET_0	Ethernet Transmit Clock	I		
G[9]	MSCR[105]	0000 (Default)	GPIO[105]	SIUL2-GPIO[105]	General Purpose IO G[9]	I/O	79	P14
		0001	FR_DBG[1]	FLEXRAY	FlexRay Debug Strobe Signal 1	O		
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O		
		0011	TX_D0	ENET_0	Ethernet MII/RMII transmit data 0	O		
		0100-1111	—	Reserved	—	—		
	IMCR[84]	0011	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I		
	IMCR[202]	0001	REQ29	SIUL2	SIUL2 External Interrupt Source 29	I		
	IMCR[213]	0011	SENT_RX[0]	SENT_1	SENT 1 Receiver channel 0	I		
G[10]	MSCR[106]	0000 (Default)	GPIO[106]	SIUL2-GPIO[106]	General Purpose IO G[10]	I/O	77	R17
		0001	FR_DBG[2]	FLEXRAY	FlexRay Debug Strobe Signal 2	O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	TX_D1	ENET_0	Ethernet MII/RMII transmit data 1	O		
		0100-1111	—	Reserved	—	—		
	IMCR[85]	0010	FAULT2	FlexPWM_0	FlexPWM_0 Fault Input 2	I		
	IMCR[206]	0100	SENT_RX[1]	SENT_0	SENT 0 Receiver channel 1	I		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
G[11]	MSCR[107]	0000 (Default)	GPIO[107]	SIUL2-GPIO[107]	General Purpose IO G[11]	I/O	75	T15
		0001	FR_DBG[3]	FLEXRAY	FlexRay Debug Strobe Signal 3	O		
		0010	—	Reserved	—	—		
		0011	TX_D3	ENET_0	Ethernet MII/RMII transmit data 3	O		
		0100-1111	—	Reserved	—	—		
	IMCR[86]	0011	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I		
	IMCR[214]	0100	SENT_RX[1]	SENT_1	SENT 1 Receiver channel 1	I		
H[4]	MSCR[116]	0000 (Default)	GPIO[116]	SIUL2-GPIO[116]	General Purpose IO H[4]	I/O		F4
		0001	X0	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 0	I/O		
		0010	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[71]	0001	ETC0	eTimer_2	eTimer_2 Input Data Channel 0	I		
	IMCR[231]	0001	CRS	ENET_0	Ethernet MII Carrier Sense	I		
H[5]	MSCR[117]	0000 (Default)	GPIO[117]	SIUL2-GPIO[117]	General Purpose IO H[5]	I/O		F3
		0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O		
		0100-1111	—	Reserved	—	—		
	IMCR[105]	0010	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I		
	IMCR[230]	0001	COL	ENET_0	Ethernet MII Collision	I		
H[6]	MSCR[118]	0000 (Default)	GPIO[118]	SIUL2-GPIO[118]	General Purpose IO H[6]	I/O		C13
		0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 0	I/O		
		0010	—	Reserved	—	—		
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O		
		0100-1111	—	Reserved	—	—		
	IMCR[106]	0010	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I		
H[7]	MSCR[119]	0000 (Default)	GPIO[119]	SIUL2-GPIO[119]	General Purpose IO H[7]	I/O		F2
		0001	X1	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 1	I/O		

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
		0010	ETC1	eTimer_2	eTimer_2 Input/Output Data Channel 1	I/O		
		0011	MDIO	ENET_0	Ethernet MDIO input/output data	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[72]	0001	ETC1	eTimer_2	eTimer_2 Input Data Channel 1	I		
H[8]	MSCR[120]	0000 (Default)	GPIO[120]	SIUL2-GPIO[120]	General Purpose IO H[8]	I/O		L1
		0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O		
		0100-1111	—	Reserved	—	—		
	IMCR[109]	0010	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I		
	IMCR[228]	0001	RX_D2	ENET_0	Ethernet MII Receive Data 2	I		
H[9]	MSCR[121]	0000 (Default)	GPIO[121]	SIUL2-GPIO[121]	General Purpose IO H[9]	I/O		B13
		0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 1	I/O		
		0010	—	Reserved	—	—		
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O		
		0100-1111	—	Reserved	—	—		
	IMCR[110]	0010	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I		
H[10]	MSCR[122]	0000 (Default)	GPIO[122]	SIUL2-GPIO[122]	General Purpose IO H[10]	I/O		C7
		0001	X2	FlexPWM_1	FlexPWM_1 Auxiliary Input/ Output 2	I/O		
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O		
		0011-1111	—	Reserved	—	—		
	IMCR[73]	0010	ETC2	eTimer_2	eTimer_2 Input Data Channel 2	I		
H[11]	MSCR[123]	0000 (Default)	GPIO[123]	SIUL2-GPIO[123]	General Purpose IO H[11]	I/O		C9
		0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input/ Output 2	I/O		
		0010-1111	—	Reserved	—	—		
	IMCR[112]	0010	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I		
H[12]	MSCR[124]	0000 (Default)	GPIO[124]	SIUL2-GPIO[124]	General Purpose IO H[12]	I/O		A7

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0001	I/O-Pad	A[15]
			0010	I/O-Pad	B[1]
			0011-1111	—	Reserved
FlexCAN_2	RXD	IMCR[34]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[15]
			0010	I/O-Pad	I[6]
			0011	I/O-Pad	J[8]
			0100-1111	—	Reserved
CTU_0	EXT_IN	IMCR[38]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved
CTU_1	EXT_IN	IMCR[39]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[4]
			0010	I/O-Pad	J[9]
			0011-1111	—	Reserved
DSPI_0	SIN	IMCR[41]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[7]
			0010-1111	—	Reserved
DSPI_1	SIN	IMCR[44]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[8]
			0010-1111	—	Reserved
DSPI_2	SIN	IMCR[47]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[13]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
DSPI_2	SCK	IMCR[48]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[0]
			0010	I/O-Pad	A[11]
			0011-1111	—	Reserved
DSPI_2	SC0	IMCR[49]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010	I/O-Pad	A[10]
			0011-1111	—	Reserved
DSPI_3	SIN	IMCR[50]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[1]
			0010	I/O-Pad	D[7]
			0011	I/O-Pad	D[14]
			0100	I/O-Pad	E[15]

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0101-1111	—	Reserved
DSPI_3	SCK	IMCR[51]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010	I/O-Pad	D[11]
			0011	I/O-Pad	E[13]
			0100	I/O-Pad	I[15]
			0101-1111	—	Reserved
DSPI_3	CS0	IMCR[52]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[11]
			0010	I/O-Pad	D[10]
			0011	I/O-Pad	F[5]
			0100	I/O-Pad	I[14]
			0101-1111	—	Reserved
eTimer_0	ETC0	IMCR[59]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[10]
			0010	I/O-Pad	A[0]
			0011-1111	—	Reserved
eTimer_0	ETC1	IMCR[60]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[11]
			0010	I/O-Pad	A[1]
			0011-1111	—	Reserved
eTimer_0	ETC2	IMCR[61]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
eTimer_0	ETC3	IMCR[62]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[14]
			0010	I/O-Pad	A[3]
			0011-1111	—	Reserved
eTimer_0	ETC4	IMCR[63]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[14]
			0010	I/O-Pad	G[3]
			0011	I/O-Pad	A[4]
			0100	I/O-Pad	C[11]
			0101-1111	—	Reserved
eTimer_0	ETC5	IMCR[64]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[8]
			0010	I/O-Pad	G[4]
			0011	I/O-Pad	C[12]

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3.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

Table 15. ESD ratings

No.	Symbol	Parameter	Conditions[1]	Class	Max value	Unit
1	$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator (external NPN to support core current)
- Low voltage detector (LVD_IO) for 3.3 V supply to IO ($V_{DD\_HV\_IO}$)
- Low voltage detector (LVD_PMC) for 3.3 V supply ($V_{DD\_HV\_PMU}$)
- Low voltage detector (LVD_FLASH) for 3.3 V flash memory supply ($V_{DD\_HV\_FLA}$)
- Low voltage detector (LVD_ADC) for 3.3 V ADC supply ($V_{DD\_HV\_ADV}$)
- Low voltage detector (LVD_OSC) for 3.3 V OSC supply ($V_{DD\_HV\_OSC}$)
- Low voltage detector (LVD_CORE) for 1.25 V digital core supply (V_{DD_LV})
- Low voltage detector (LVD_CORE_BK) for the self-test of LVD_CORE
- High voltage detector (HVD_CORE) for 1.25 V digital core supply (V_{DD_LV})

Table 24. PLL0 electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	5	mA

1. V_{DD_LV} =1.25 V ± 5%, T_J = -40 to 165 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock. Input characteristics are granted when using IRCOSC or when external oscillator is used in functional mode.
3. VDD_LV noise due to application in the range V_{DD_LV} = 1.25 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

Table 25. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL1IN}	PLL1 input clock	—	38	—	78	MHz
Δ_{PLL1IN}	PLL0 input clock duty cycle[2]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.76	—	200	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. V_{DD_LV} = 1.25 V ± 5%, T_J = -40 to 165 °C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or when external oscillator is used in functional mode.

3.14 16 MHz Internal RC Oscillator (IRCOSC) electrical specifications

NOTE

Unless stated otherwise, specifications in Table 26 assume the following: $V_{DD\_HV\_PMU}$=3.15V to 3.6V, V_{SS}=0V, V_{DD_LV}=1.18V to 1.32V, V_{SS}=0V, T_J=–40 to 165°C.

Table 26. Internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{Target}	IRCOSC target frequency	—	—	16	—	MHz
$f_{Untrimmed}$	IRCOSC frequency (untrimmed)	—	11	—	17	MHz

Table continues on the next page...

3.16 Flash memory specifications

3.16.1 Maximum junction temperature 150°C

3.16.1.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 28 shows the estimated Program/Erase times.

Table 28. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			$20°C \le T_A \le 30°C$	$-40°C \le T_J \le 150°C$	$-40°C \le T_J \le 150°C$	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: $-40°C \le T_J \le 150°C$, full spec voltage.

Table 31. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.16.2 Maximum junction temperature 165°C

3.16.2.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 32 shows the estimated Program/Erase times.

Table 33. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.16.2.3 Flash memory module life specifications

Table 34. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	-	250,000	-	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	-	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	-	Years
		Blocks with 100,000 P/E cycles.	20	-	Years
		Blocks with 250,000 P/E cycles.	10	-	Years

1. Program and erase supported across standard temperature specs. Up to 10,000 program and erase cycles may be done between 150 °C and 165 °C out of the total specified number of cycles.
2. Program and erase supported across standard temperature specs.

3.16.2.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.

Table 35. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UTO-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UTO-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.16.3 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

NOTE

If the user does not follow these recommended settings, the user must run the flash memory's array integrity (AI) check with breakpoints disabled: Set the Array Integrity Break Point Enable bit in the C55FMC's UTest 0 register (C55FMC_UT0[AIBPE]) to 0.

Table 36. Flash memory read wait-state and address-pipeline control combinations

Operating frequency (f_{CPU} = SYS_CLK)		RWSC	APC	Flash read latency on mini-cache miss (# of f_{CPU} clock periods)	Flash read latency on mini-cache hit (# of f_{CPU} clock periods)
–40°C to 150°C	Max 165°C option				
0 MHz < f_{CPU} ≤ 33 MHz	0 MHz < f_{CPU} ≤ 30 MHz	0	0	3	1
33 MHz < f_{CPU} ≤ 100 MHz	30 MHz < f_{CPU} ≤ 90 MHz	2	1	5	1
100 MHz < f_{CPU} ≤ 133 MHz	90 MHz < f_{CPU} ≤ 120 MHz	3	1	6	1

Table continues on the next page...

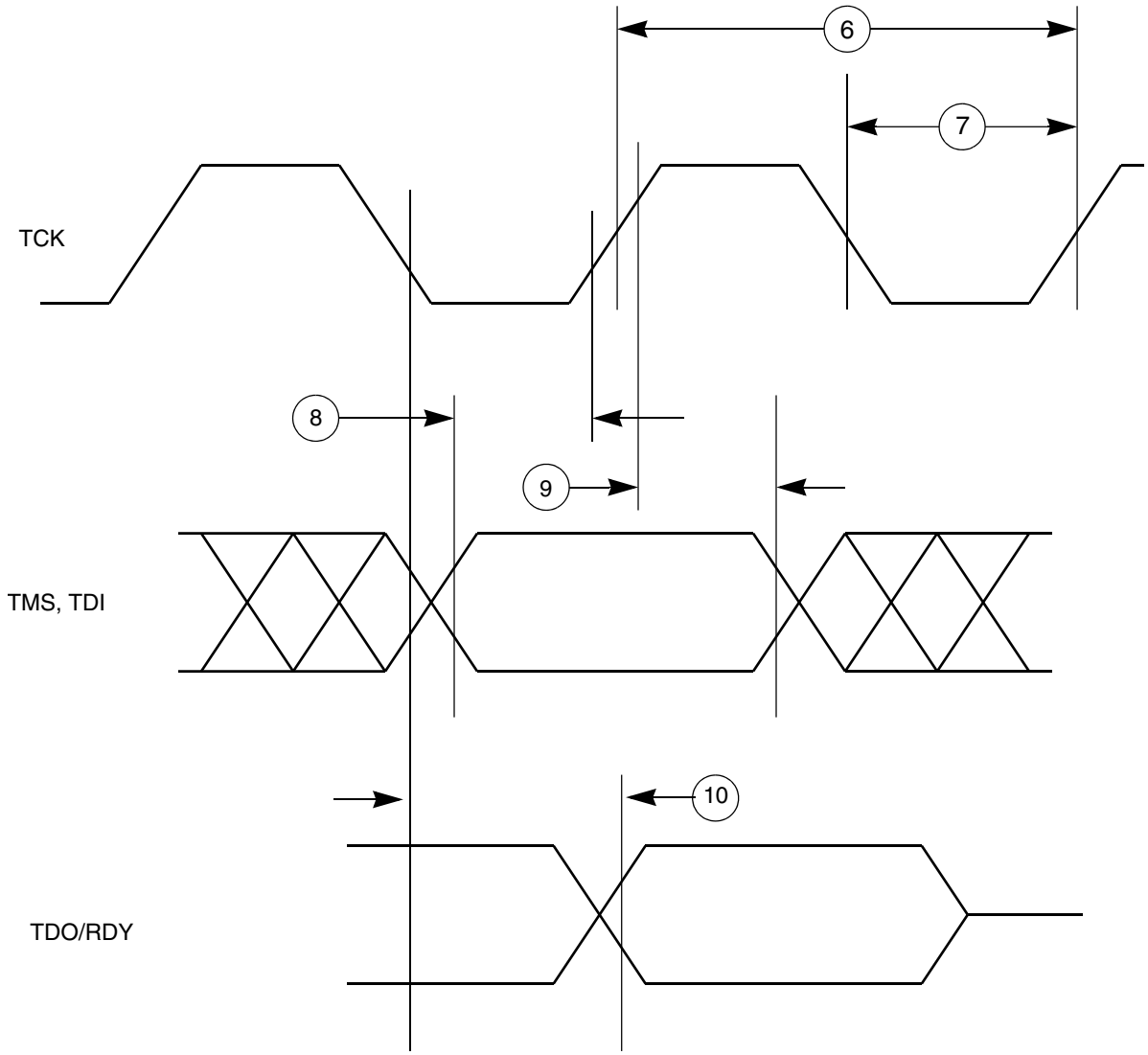

Figure 17. Nexus TDI, TMS, TDO timing

3.19.3.3 Aurora LVDS driver electrical characteristics

Table 45. Aurora LVDS driver electrical characteristics

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
Data Rate					
DATARATE	Data rate	—	1250	Typ+0.1%	Mbps
STARTUP					
T_{STRT_BIAS}	Bias startup time[2]	—	—	5	µs
T_{STRT_TX}	Transmitter startup time[3]	—	—	5	µs
T_{STRT_RX}	Receiver startup time[4]	—	—	4	µs

1. Conditions for these values are $V_{DD\_HV\_IO}$ = 3.3 V (–5%, +10%), T_J = –40 to 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.

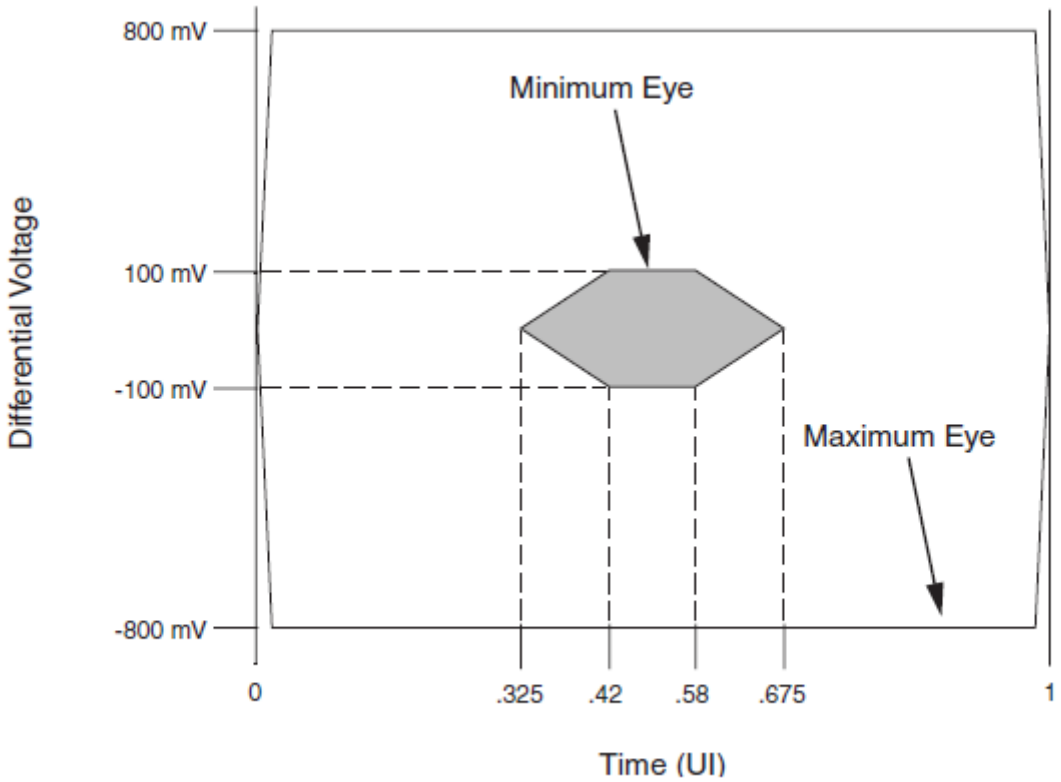

Figure 19. Nexus Aurora receiver "eye" diagram

3.19.4 External interrupt timing (IRQ pin)

Table 47. External interrupt timing

#	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

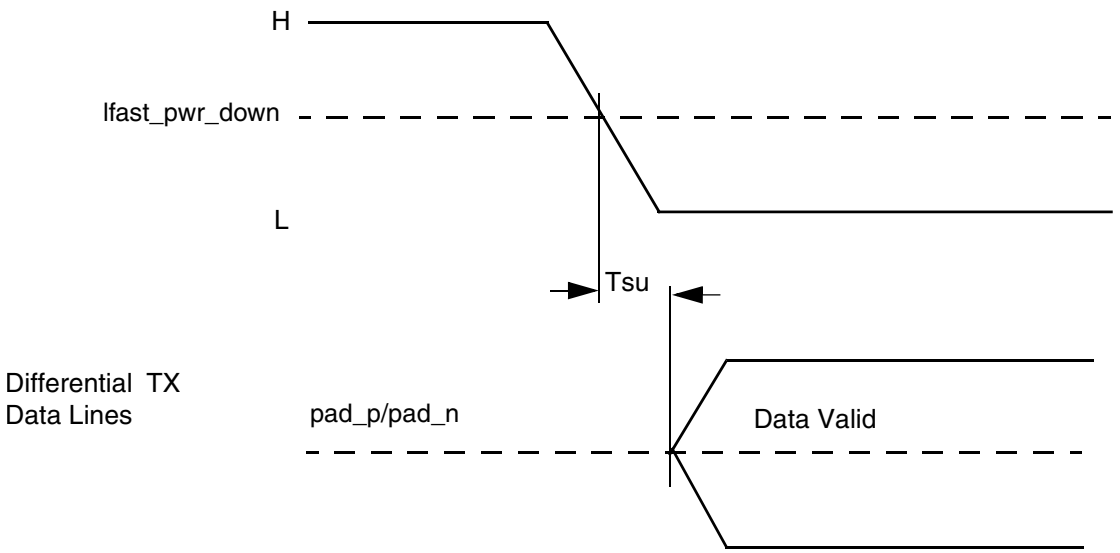

Figure 31. Power-down exit time

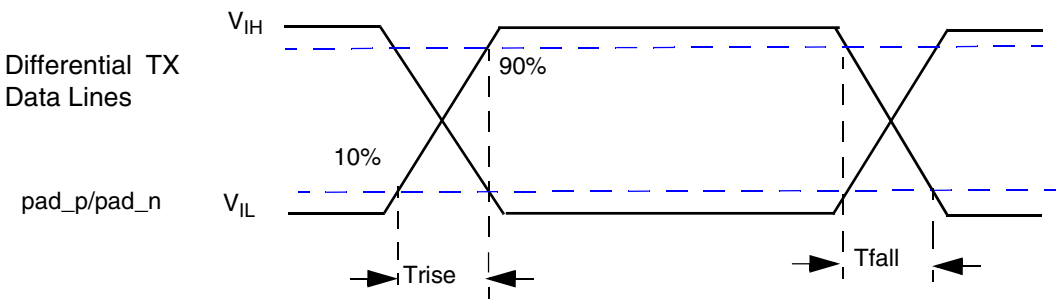

Figure 32. Rise/fall time

3.19.6.2 LFAST interface electrical characteristics

Table 49. LFAST electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$V_{DD\_HV\_IO}$	Operating supply conditions		3.15	—	3.6	V
Data Rate						
DATARATE	Data rate	—	—	312/320	Typ+0.1%	Mbps
STARTUP						
T_{STRT_BIAS}	Bias startup time[2]	—	—	0.5	3	µs
T_{PD2NM_TX}	Transmitter startup time (power down to normal mode)[3]	—	—	0.2	2	µs
T_{SM2NM_TX}	Transmitter startup time (sleep mode to normal mode)	—	—	0.2	0.5	µs
T_{PD2NM_RX}	Receiver startup time[5] (Power down to Normal mode)	—	—	20	40	ns
T_{PD2SM_RX}	Receiver startup time[4] (Power down to Sleep mode)	—	—	20	50	ns

Table continues on the next page...

Table 51. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C, TxEN pin load maximum 25 pF

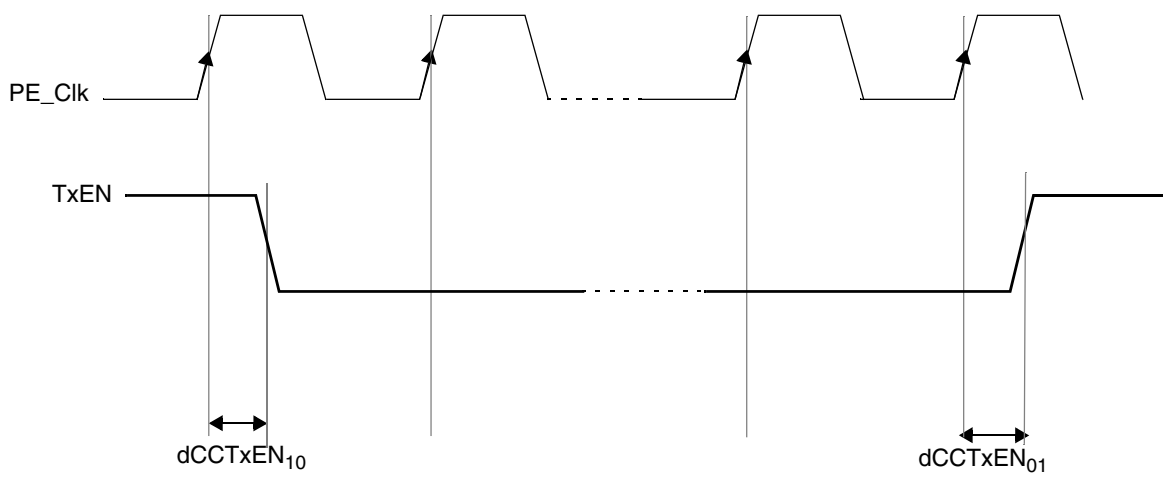

Figure 34. FlexRay TxEN signal propagation delays

3.19.7.3 TxD

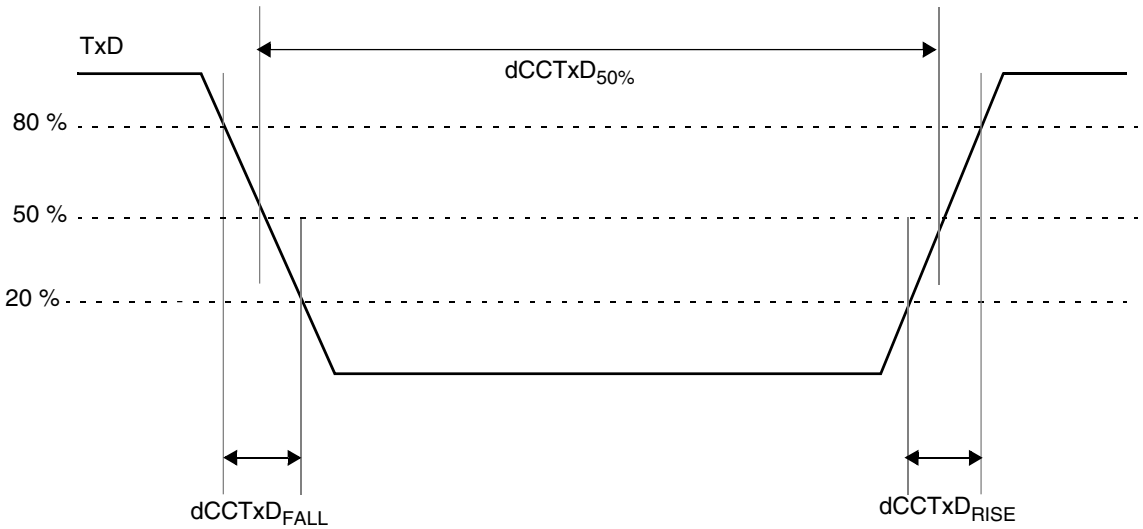

Figure 35. FlexRay TxD signal

Table 52. TxD output characteristics

Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load (=$dCCTxD_{50\%}$ - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9	ns
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C, TxD pin load maximum 25 pF