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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	-
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5744pk1ammm8

1 Introduction

1.1 Features

The following table summarizes the features of the MPC5744P.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution speed	0 MHz to 200 MHz (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory—see Table 2 for additional details	
Code/data flash memory	**2.5 MB**, ECC, RWW
Data flash memory	Supported with RWW
SRAM	**384 KB**, ECC
Overlay access to SRAM from Flash Memory Controller	Yes
Modules	
Interrupt controller	32 interrupt priority levels, 16 SW programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules

Table continues on the next page...

Table 4. Power supply and reference voltage pins/balls (continued)

Supply			Package	
Symbol	**Type**	**Description**	**144LQFP**	**257MAPBGA**
$V_{DD\_HV\_IO}$	Power	High voltage Power Supply for I/O	6	A9
			21	B2
			72	B16
			91	D8
			126	D14
				G2
				M2
				T2
				T16
				U14
$V_{SS\_HV\_IO}$	Ground	High voltage Ground Supply for I/O	7	A1
			22	A2
			90	A16
			127	A17
				B1
				B9
				B17
				C3
				C15
				D9
				H2
				N2
				R3
				R15
				T1
				T17
				U1
				U2
				U16
				U17
$V_{DD\_HV\_PMU}$ $V_{DD\_HV\_PMU\_AUX}$	Power	PMU high voltage Supply	72	U14
$V_{DD\_HV\_OSC}$	Power	Power Supply for the oscillator	27	M1
$V_{SS\_HV\_OSC}$	Ground	Ground Supply for the oscillator	28	P1
$V_{DD\_HV\_FLA}$	Power	Power Supply and decoupling pin for flash memory	97	H16
$V_{DD\_HV\_ADV}$	Power	High voltage Supply for ADC, TSENS, SGEN (3.3 V)	58	T10
$V_{SS\_HV\_ADV}$	Ground	High voltage Ground for ADC	59	U9

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Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
E[10]	MSCR[74]	0000 (Default)	GPI[74][4] ADC1_AN[8]/ ADC3_AN[7]	SIUL2-GPI[74]	General Purpose Input E[10]	I	63	T11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[11]	MSCR[75]	0000 (Default)	GPI[75][4] ADC1_AN[4]/ ADC3_AN[3]	SIUL2-GPI[75]	General Purpose Input E[11]	I	65	U11
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[12]	MSCR[76]	0000 (Default)	GPI[76][4] ADC1_AN[6]/ ADC3_AN[5]	SIUL2-GPI[76]	General Purpose Input E[12]	I	67	T12
		0001	—	Reserved	—	—		
		0010-1111	—	Reserved	—	—		
E[13]	MSCR[77]	0000 (Default)	GPIO[77]	SIUL2-GPIO[77]	General Purpose IO E[13]	I/O	117	A11
		0001	ETC5	eTimer_0	eTimer_0 Input/Output Data Channel 5	I/O		
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O		
		0011	CS4	DSPI1	DSPI 1 Peripheral Chip Select 4	O		
		0100	SCK	DSPI3	DSPI 3 Input/Output Serial Clock	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[51]	0011	SCK	DSPI3	DSPI 3 Input Serial Clock	I		
	IMCR[198]	0001	REQ25	SIUL2	SIUL2 External Interrupt Source 25	I		
	IMCR[64]	0100	ETC5	eTimer_0	eTimer_0 Input Data Channel	I		
E[14]	MSCR[78]	0000 (Default)	GPIO[78]	SIUL2-GPIO[78]	General Purpose IO E[14]	I/O	119	B10
		0001	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O		
		0010	SOUT	DSPI3	DSPI 3 Serial Data Out	O		
		0011	CS5	DSPI1	DSPI 1 Peripheral Chip Select 5	O		
		0100	B2	FlexPWM_1	FlexPWM_1 Channel B Input/ Output 2	I/O		
		0101-1111	—	Reserved	—	—		
	IMCR[70]	0100	ETC5	eTimer_1	eTimer_1 Input Data Channel 5	I		
	IMCR[113]	0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I		

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0001	I/O-Pad	A[15]
			0010	I/O-Pad	B[1]
			0011-1111	—	Reserved
FlexCAN_2	RXD	IMCR[34]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[15]
			0010	I/O-Pad	I[6]
			0011	I/O-Pad	J[8]
			0100-1111	—	Reserved
CTU_0	EXT_IN	IMCR[38]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	C[15]
			0011-1111	—	Reserved
CTU_1	EXT_IN	IMCR[39]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[4]
			0010	I/O-Pad	J[9]
			0011-1111	—	Reserved
DSPI_0	SIN	IMCR[41]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[7]
			0010-1111	—	Reserved
DSPI_1	SIN	IMCR[44]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[8]
			0010-1111	—	Reserved
DSPI_2	SIN	IMCR[47]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[13]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
DSPI_2	SCK	IMCR[48]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[0]
			0010	I/O-Pad	A[11]
			0011-1111	—	Reserved
DSPI_2	SC0	IMCR[49]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010	I/O-Pad	A[10]
			0011-1111	—	Reserved
DSPI_3	SIN	IMCR[50]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[1]
			0010	I/O-Pad	D[7]
			0011	I/O-Pad	D[14]
			0100	I/O-Pad	E[15]

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0101-1111	—	Reserved
DSPI_3	SCK	IMCR[51]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010	I/O-Pad	D[11]
			0011	I/O-Pad	E[13]
			0100	I/O-Pad	I[15]
			0101-1111	—	Reserved
DSPI_3	CS0	IMCR[52]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[11]
			0010	I/O-Pad	D[10]
			0011	I/O-Pad	F[5]
			0100	I/O-Pad	I[14]
			0101-1111	—	Reserved
eTimer_0	ETC0	IMCR[59]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[10]
			0010	I/O-Pad	A[0]
			0011-1111	—	Reserved
eTimer_0	ETC1	IMCR[60]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[11]
			0010	I/O-Pad	A[1]
			0011-1111	—	Reserved
eTimer_0	ETC2	IMCR[61]	0000 (Default)	—	Disable
			0001	I/O-Pad	F[0]
			0010	I/O-Pad	A[2]
			0011-1111	—	Reserved
eTimer_0	ETC3	IMCR[62]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[14]
			0010	I/O-Pad	A[3]
			0011-1111	—	Reserved
eTimer_0	ETC4	IMCR[63]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[14]
			0010	I/O-Pad	G[3]
			0011	I/O-Pad	A[4]
			0100	I/O-Pad	C[11]
			0101-1111	—	Reserved
eTimer_0	ETC5	IMCR[64]	0000 (Default)	—	Disable
			0001	I/O-Pad	B[8]
			0010	I/O-Pad	G[4]
			0011	I/O-Pad	C[12]

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Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
			0100-1111	—	Reserved
FlexPWM_0	X2	IMCR[96]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[10]
			0010	I/O-Pad	G[2]
			0011-1111	—	Reserved
FlexPWM_0	A3	IMCR[97]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[2]
			0010	I/O-Pad	C[10]
			0011	I/O-Pad	D[3]
			0100	I/O-Pad	G[6]
			0101-1111	—	Reserved
FlexPWM_0	B3	IMCR[98]	0000 (Default)	—	Disable
			0001	I/O-Pad	A[3]
			0010	I/O-Pad	A[9]
			0011	I/O-Pad	D[4]
			0100	I/O-Pad	G[7]
			0101-1111	—	Reserved
FlexPWM_0	X3	IMCR[99]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[2]
			0010	I/O-Pad	D[6]
			0011	I/O-Pad	G[5]
			0100-1111	—	Reserved
FlexPWM_1	FAULT0	IMCR[100]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[0]
			0010-1111	—	Reserved
FlexPWM_1	FAULT1	IMCR[101]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[1]
			0010-1111	—	Reserved
FlexPWM_1	FAULT2	IMCR[102]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[2]
			0010-1111	—	Reserved
FlexPWM_1	FAULT3	IMCR[103]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[3]
			0010-1111	—	Reserved
FlexPWM_1	A0	IMCR[105]	0000 (Default)	—	Disable
			0001	I/O-Pad	C[13]
			0010	I/O-Pad	H[5]
			0011-1111	—	Reserved
FlexPWM_1	B0	IMCR[106]	0000 (Default)	—	Disable

Table continues on the next page...

Table 10. Peripheral muxing (continued)

Destination peripheral	Destination functions	IMCR number	IMCR[SSS] field value	Source peripherals	Source functions
SENT_1	SENT_RX[1]	IMCR[214]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[12]
			0010	I/O-Pad	J[6]
			0011	I/O-Pad	A[10]
			0100	I/O-Pad	G[11]
			0101-1111	—	Reserved
ENET_0	RX_CLK	IMCR[224]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[8]
			0010-1111	—	Reserved
ENET_0	RX_DV	IMCR[225]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[7]
			0010-1111	—	Reserved
ENET_0	RX_D0	IMCR[226]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[6]
			0010-1111	—	Reserved
ENET_0	RX_D1	IMCR[227]	0000 (Default)	—	Disable
			0001	I/O-Pad	D[5]
			0010-1111	—	Reserved
ENET_0	RX_D2	IMCR[228]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[8]
			0010-1111	—	Reserved
ENET_0	RX_D3	IMCR[229]	0000 (Default)	—	Disable
			0001	I/O-Pad	J[9]
			0010-1111	—	Reserved
ENET_0	COL	IMCR[230]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[5]
			0010-1111	—	Reserved
ENET_0	CRS	IMCR[231]	0000 (Default)	—	Disable
			0001	I/O-Pad	H[4]
			0010-1111	—	Reserved
ENET_0	RX_ER	IMCR[232]	0000 (Default)	—	Disable
			0001	I/O-Pad	I[1]
			0010-1111	—	Reserved
ENET_0	TX_CLK	IMCR[233]	0000 (Default)	—	Disable
			0001	I/O-Pad	G[8]
			0010-1111	—	Reserved

1. (Default) = configuration after reset
2. Selecting an alternate function with a 'Reserved' source function causes the pin to enter a null state (Input buffer and Output buffer enables both at 0).

CAUTION

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 12. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD_LV}	1.25 V core supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_LV\_PLL}$	1.25 V PLL supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_LV\_LFAST}$	1.25 V LFAST PLL supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_LV\_NEXUS}$	1.25 V Aurora LVDS supply voltage[1, 2, 3]	—	–0.3	1.5	V
$V_{DD\_HV\_PMU}$	3.3 V voltage regulator supply voltage	—	–0.3	4.0[4, 5]	V
$V_{DD\_HV\_IO}$	3.3 V input/output supply voltage	—	–0.3	3.63[4, 5]	V
$V_{SS\_HV\_IO}$	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	3.3 V flash supply voltage	—	–0.3	3.63[4, 5]	V
$V_{SS\_HV\_FLA}$	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.0[4, 5]	V
$V_{SS\_HV\_OSC}$	3.3 V crystal oscillator amplifier ground	—	–0.1	0.1	V
$V_{DD\_HV\_ADRE0}$[6] $V_{DD\_HV\_ADRE1}$	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6	V
$V_{SS\_HV\_ADRE0}$ $V_{SS\_HV\_ADRE1}$	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	3.3 V ADC supply voltage	—	–0.3	4.0[4, 5]	V
$V_{SS\_HV\_ADV}$	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	Supply ramp rate	—	0.9 V/s	0.06 V/µs	
V_{INA}	Voltage on analog pin with respect to ground ($V_{SS\_HV\_IO}$)	—	–0.3	6	V
V_{IN}	Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IO}$)	Relative to $V_{DD\_HV\_IO}$	–0.3	$V_{DD\_HV\_IO}$ + 0.3[7]	V
I_{INJ}	Maximum DC injection current per pin, 5 V ADC pads	Note [8]	–5	5	mA
I_{INJPAD}	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	Storage temperature	—	–55	165	°C

1. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum T_J=165°C; remaining time as defined in note -1 and note -1.
2. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum T_J=165°C; remaining time as defined in note -1.
3. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J=165°C.
4. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
5. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
6. $V_{DD\_HV\_ADRE0}$ and $V_{DD\_HV\_ADRE1}$ cannot be operated at different voltages and must be supplied by the same voltage source.
7. Only when $V_{DD\_HV\_IO}$ < 3.63 V.
8. The following conditions apply:
   - Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 6.0 V (60 seconds lifetime, no restrictions—part can switch)

- Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 6.0 V (10 hours, device in reset—no switching)
- Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 5.5 V (always)
- Absolute maximum ADC input pin voltage = 7.0 V (60 seconds lifetime), when V_{DD_HV} is connected to the 5 V
- Absolute maximum ADC input pin voltage = 6.5 V (always while respecting 5 mA maximum injection), when V_{DD_HV} is connected to the 5 V

3.4 Recommended operating conditions

NOTE

Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and DC electrical specifications for I/Os might not be guaranteed.

Table 13. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_PMU}$[1]	3.3 V voltage regulator supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_IO}$[2]	3.3 V input/output supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_IO}$	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$[3]	3.3 V flash supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_FLA}$	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$[4]	3.3 V crystal oscillator amplifier supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_OSC}$	3.3 V crystal oscillator amplifier ground	—	0	0	V
$V_{DD\_HV\_ADRE0}$ $V_{DD\_HV\_ADRE1}$	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	$T_J \le 150°C$	3.15 to 5.5		V
$V_{DD\_HV\_ADRE0}$[5] $V_{DD\_HV\_ADRE1}$	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	$150°C < T_J < 165°C$ (only for corresponding marked parts)	3.15 to 5.25		V
$V_{SS\_HV\_ADRE0}$[5] $V_{SS\_HV\_ADRE1}$	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_ADV}$[6]	3.3 V ADC supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_ADV}$	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_COR}$[7]	Core supply, 1.25 V +/-5%	—	1.19	1.32	V
$V_{DD\_LV\_CORx}$	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$	Internal PLL supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_PLL}$	Internal PLL reference voltage	—	0	0	V
$V_{DD\_LV\_NEXUS}$	Aurora LVDS supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_NEXUS}$	Aurora LVDS supply ground	—	0	0	V
$V_{DD\_LV\_LFAST}$	LFAST PLL supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_LFAST}$	LFAST PLL supply ground	—	0	0	V
I_{IC}	DC injection current per pin[8, 9, 10]	Digital pins	–3.0	3.0	mA
		Analog pins	–3.0	3.0	

Table continues on the next page...

5. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
6. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
7. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic compatibility (EMC)

Tests were carried out in accordance with the International Electrotechnical Commission specifications:

3.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

Table 15. ESD ratings

No.	Symbol	Parameter	Conditions[1]	Class	Max value	Unit
1	$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator (external NPN to support core current)
- Low voltage detector (LVD_IO) for 3.3 V supply to IO ($V_{DD\_HV\_IO}$)
- Low voltage detector (LVD_PMC) for 3.3 V supply ($V_{DD\_HV\_PMU}$)
- Low voltage detector (LVD_FLASH) for 3.3 V flash memory supply ($V_{DD\_HV\_FLA}$)
- Low voltage detector (LVD_ADC) for 3.3 V ADC supply ($V_{DD\_HV\_ADV}$)
- Low voltage detector (LVD_OSC) for 3.3 V OSC supply ($V_{DD\_HV\_OSC}$)
- Low voltage detector (LVD_CORE) for 1.25 V digital core supply (V_{DD_LV})
- Low voltage detector (LVD_CORE_BK) for the self-test of LVD_CORE
- High voltage detector (HVD_CORE) for 1.25 V digital core supply (V_{DD_LV})

Table 21. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	90	230	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	120	310	
$I_{DD\_LV\_HALT}$	Operating current in V_{DD} HALT mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	25	40	mA
		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	110	300	
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	140	400	
$I_{DD\_LV\_LFAST}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.6	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	6.8	
$I_{DD\_LV\_NEXUS}$	Operating current	T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.1	mA
		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	12.5	
$I_{DD\_HV\_ADV}$[3]	Operating current	T_J = 150 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.4	4.2	mA
		T_J = 165 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	3.5	4.5	
$I_{DD\_HV\_ADRE}$'[4]	Operating current	T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.20	0.28	mA
		T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.32	0.50	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	0.24	0.40	
		T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	0.40	0.70	
$I_{DD\_HV\_OSC}$	Operating current	T_J = 150 °C 3.3 V supplies	—	—	1.6	mA

Table continues on the next page...

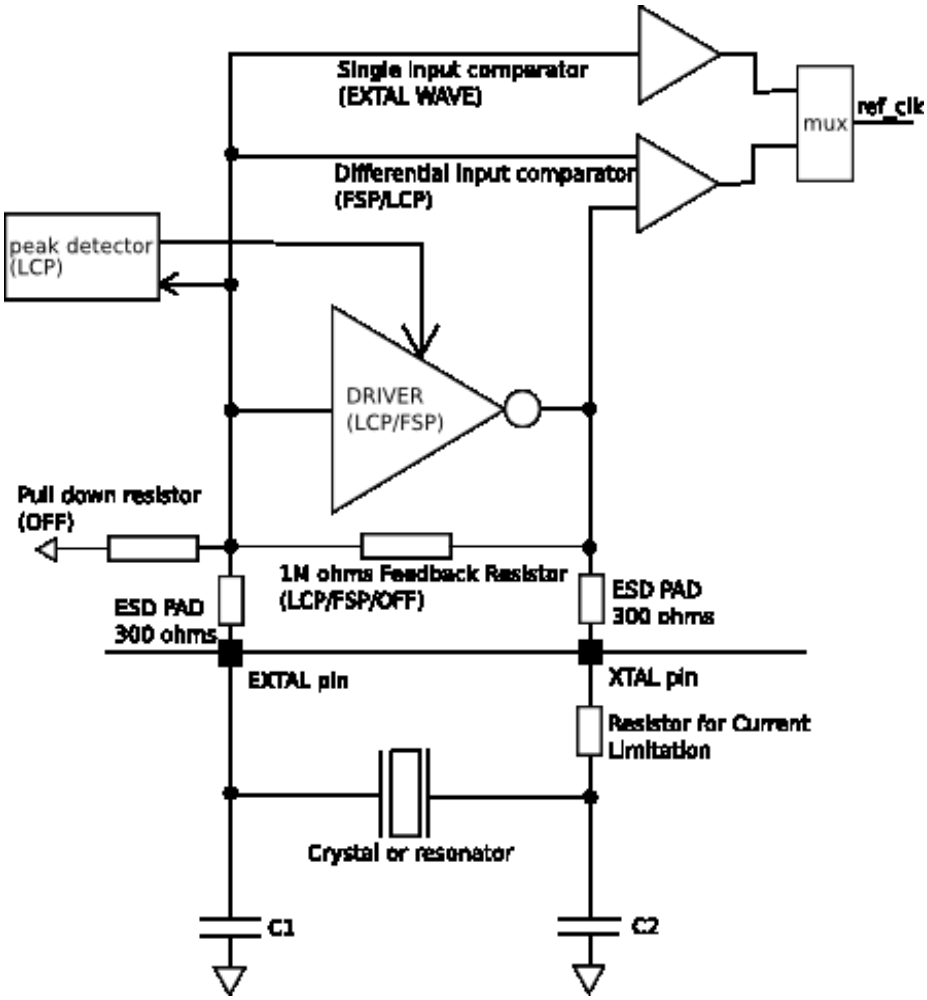


Figure 5. Oscillator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions[1]	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP	—	4[2]	—	40	MHz
$g_{mXOSCHS}$	Driver transconductance	LCP	$V_{DD\_HV\_OSC}$ = 3.3V	—	20	—	mA/V
		FSP	–5%, +10%	—	30	—	
V_{XOSCHS}	Oscillation amplitude	LCP	f_{OSC} = 4, 8, 16 MHz	1.1	1.3	2.6	V
			f_{OSC} = 40 MHz	1.2	1.5	1.7	V
$T_{XOSCHSSU}$	Oscillator startup time	FSP/LCP[3]	f_{OSC} = 4 MHz	1.75	2.5	2.9	ms
			f_{OSC} = 8, 16, 40 MHz	0.25	0.5	1.1	ms

Table continues on the next page...

3. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.19.3.4 Nexus Aurora debug port timing

Table 46. Nexus Aurora debug port timing

#	Symbol	Characteristic	Min	Max	Unit
1	t_{REFCLK}	Reference clock frequency	625	1250	MHz
2	t_{RCDC}	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	Reference Clock Stability	50	—	PPM
5	BER	Bit Error Rate	—	10^{-12}	—
6	J_D	Transmit lane Deterministic Jitter	—	0.17	OUI
7	J_T	Transmit lane Total Jitter	—	0.35	OUI
8	S_O	Differential output skew	—	20	ps
9	S_{MO}	Lane to lane output skew	—	1000	ps
10	UI	Aurora lane Unit Interval	800	1600	ps

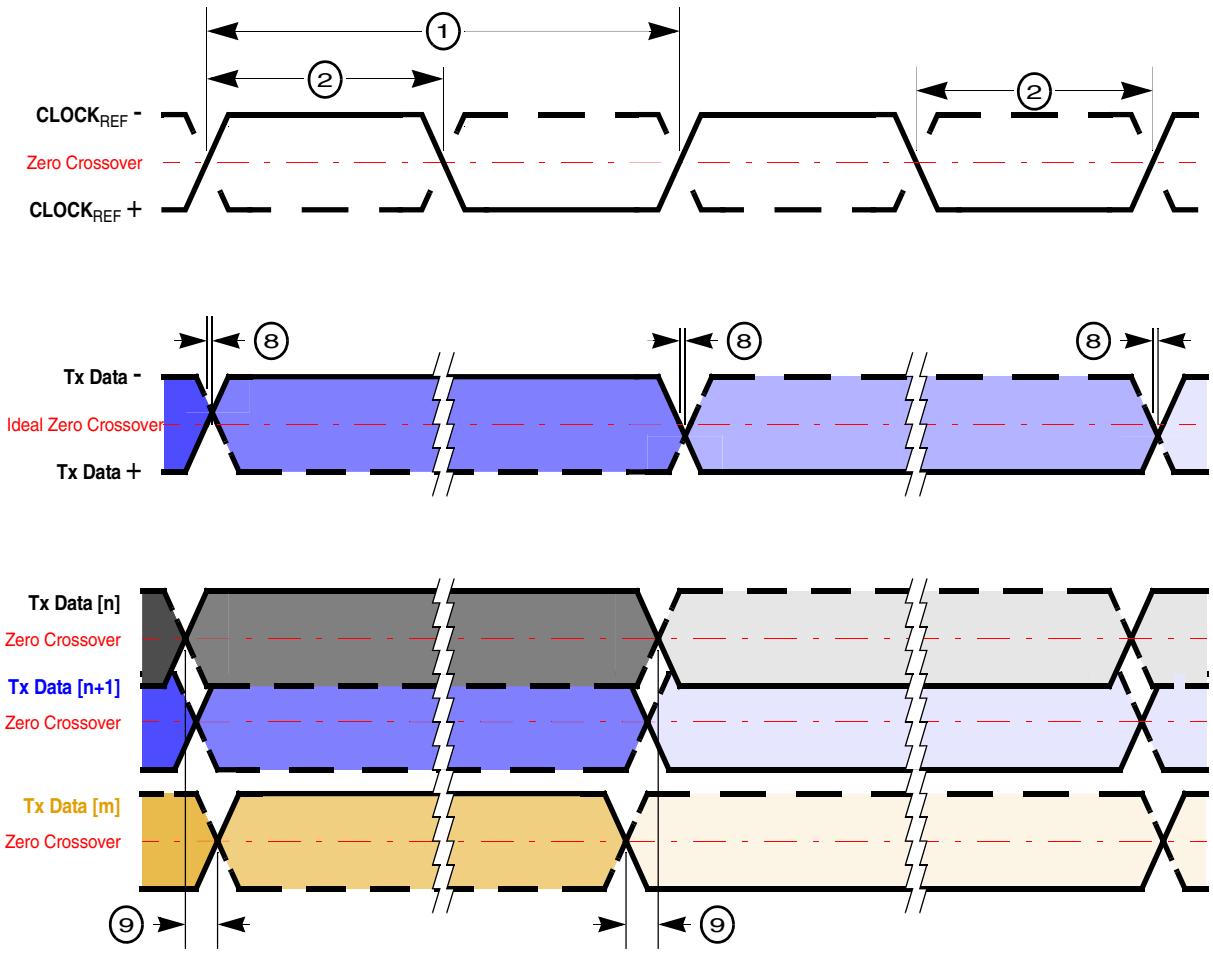


Figure 18. Nexus Aurora timings

Rise/fall timing for the Nexus Aurora debug port reference clock must conform to the area between the minimum and maximum value ranges shown in the following receiver "eye" diagram.

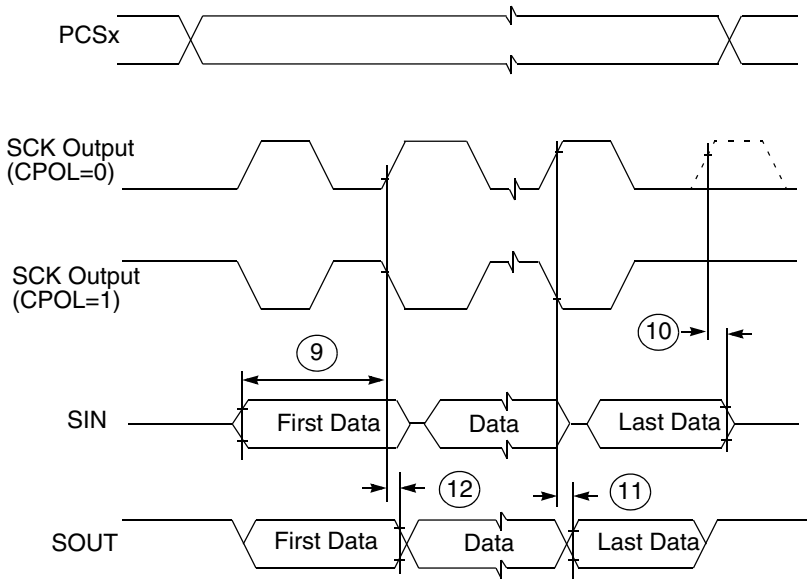


Figure 26. DSPI modified transfer format timing — master, CPHA = 1

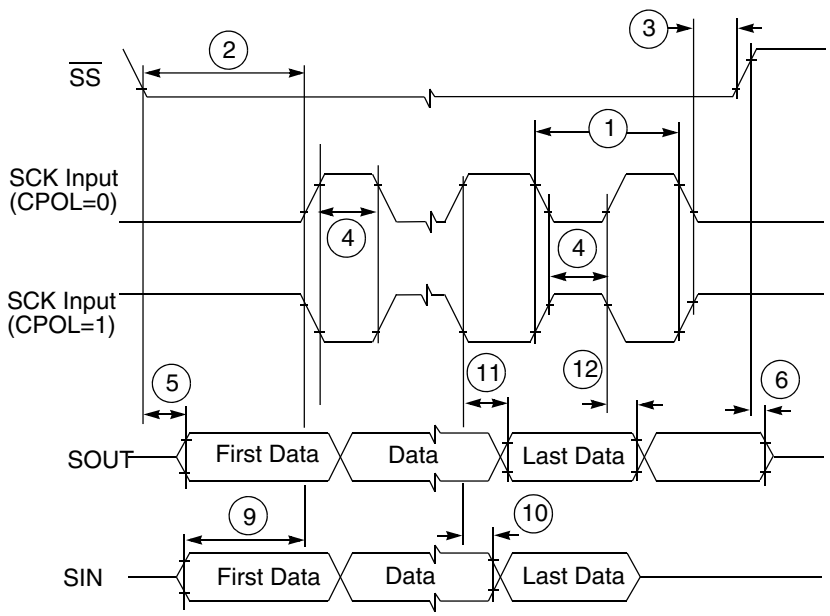
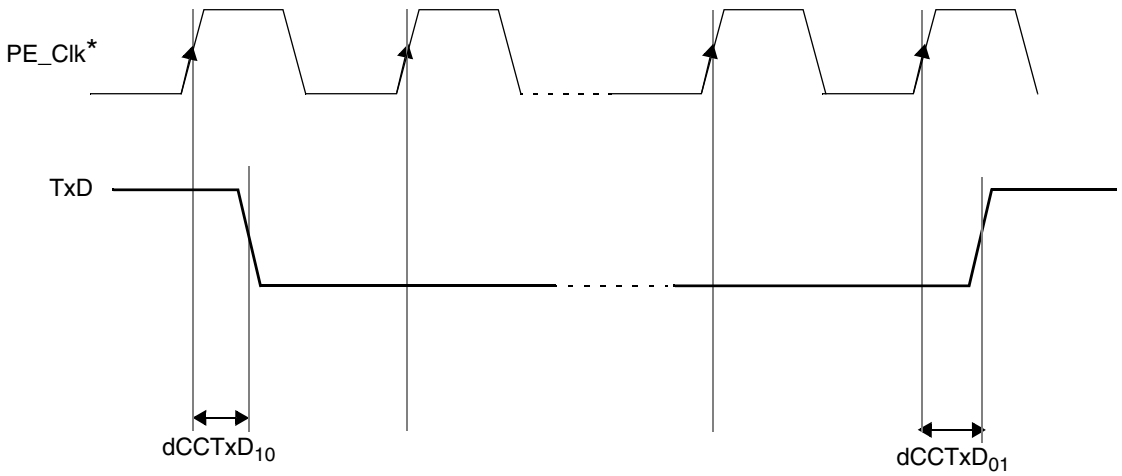


Figure 27. DSPI modified transfer format timing – slave, CPHA = 0



*FlexRay Protocol Engine Clock

Figure 36. FlexRay TxD signal propagation delays

3.19.7.4 RxD

Table 53. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, T_J = –40 / 165 °C

3.19.7.5 Receiver asymmetry

Table 54. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	–31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	–30.5	+43.0	ns

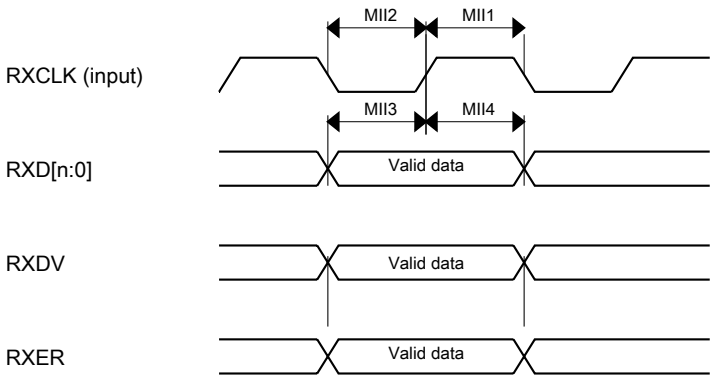


Figure 38. RMII/MII receive signal timing diagram

3.19.8.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 56. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

4 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
257-ball MAPBGA	98ASA00081D

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