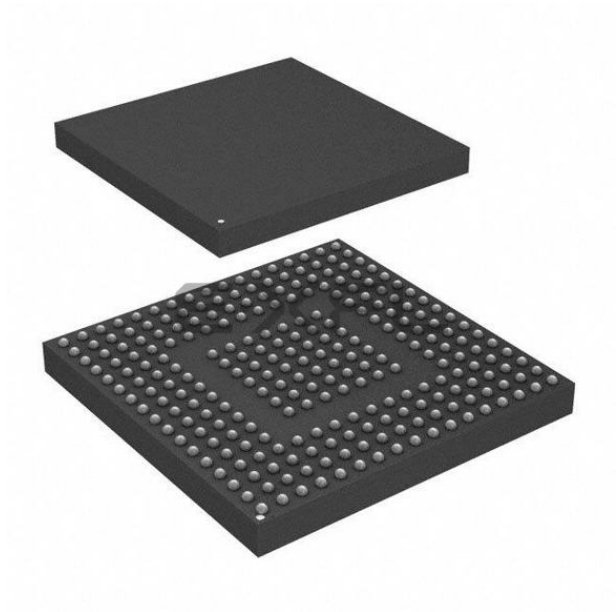

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 200MHz |
| Connectivity | CANbus, Ethernet, FlexRay, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | - |
| Program Memory Size | 2.5MB (2.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.15V ~ 5.5V |
| Data Converters | A/D 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 257-LFBGA |
| Supplier Device Package | 257-LFBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744pk1ammm9 |

# Table of Contents

# 1 Introduction

## 1.1 Features

The following table summarizes the features of the MPC5744P.

**Table 1. MPC5744P feature summary**

| Feature | Details |
|---|---|
| **CPU** | |
| Power Architecture | 2 x e200z4 in delayed lock step |
| Architecture | Harvard |
| Execution speed | 0 MHz to 200 MHz (+2% FM) |
| Embedded FPU | Yes |
| Core MPU | 24 regions |
| Instruction Set PPC | No |
| Instruction Set VLE | Yes |
| Instruction cache | 8 KB, EDC |
| Data cache | 4 KB, EDC |
| Data local memory | 64 KB, ECC |
| System MPU | Yes (16 regions) |
| **Buses** | |
| Core bus | AHB, 32-bit address, 64-bit data, e2e ECC |
| Internal periphery bus | 32-bit address, 32-bit data |
| **Crossbar** | |
| Master x slave ports | 4 x 5 |
| **Memory**—see Table 2 for additional details | |
| Code/data flash memory | **2.5 MB**, ECC, RWW |
| Data flash memory | Supported with RWW |
| SRAM | **384 KB**, ECC |
| Overlay access to SRAM from Flash Memory Controller | Yes |
| **Modules** | |
| Interrupt controller | 32 interrupt priority levels, 16 SW programmable interrupts |
| PIT | 1 module with 4 channels |
| System Timer Module (STM) | 1 module with 4 channels |
| Software Watchdog Timer (SWT) | Yes |
| eDMA | 32 channels, in delayed lock step |
| FlexRay | 1 module with 64 message buffer, dual channel |
| FlexCAN | 3 modules with 64 message buffer |
| LINFlexD (UART and LIN with DMA support) | 2 modules |

*Table continues on the next page...*

# 2 Pinouts

## 2.1 Package pinouts and ballmap

The following figures show the LQFP pinout and the BGA ballmap.

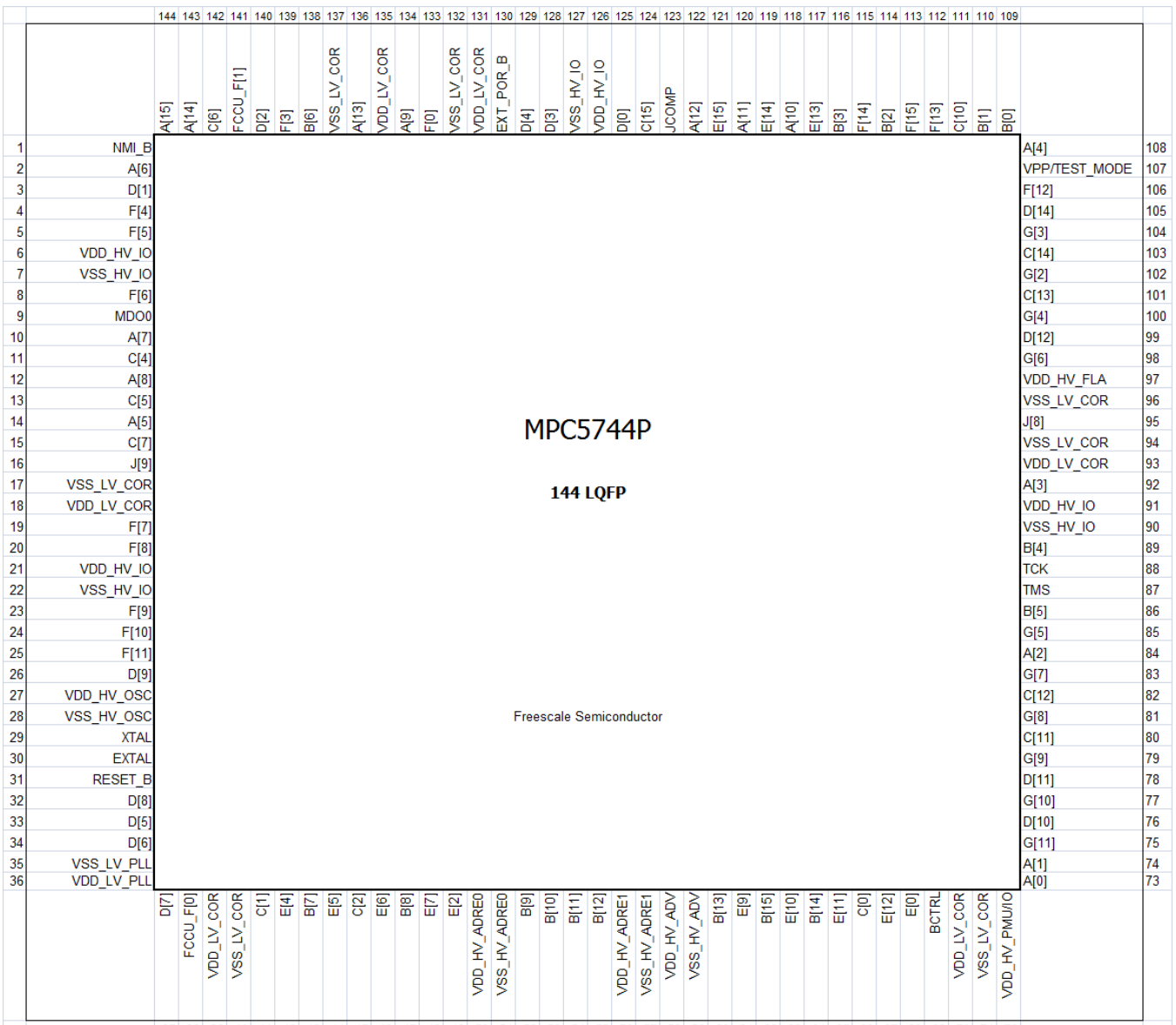



**Figure 2. 144LQFP pinout**

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[73] | 0001 | ETC2 | eTimer_2 | eTimer_2 Input Data Channel 2 | I | | |
| | IMCR[179] | 0001 | REQ6 | SIUL2 | SIUL2 External Interrupt Source 6 | I | | |
| A[7] | MSCR[7] | 0000 (Default) | GPIO[7] | SIUL2-GPIO[7] | General Purpose IO A[7] | I/O | 10 | G4 |
| | | 0001 | SOUT | DSPI1 | DSPI 1 Serial Data Out | O | | |
| | | 0010 | ETC3 | eTimer_2 | eTimer_2 Input/Output Data Channel 3 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[74] | 0001 | ETC3 | eTimer_2 | eTimer_2 Input Data Channel 3 | I | | |
| | IMCR[180] | 0001 | REQ7 | SIUL2 | SIUL2 External Interrupt Source 7 | I | | |
| A[8] | MSCR[8] | 0000 (Default) | GPIO[8] | SIUL2-GPIO[8] | General Purpose IO A[8] | I/O | 12 | H1 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | ETC4 | eTimer_2 | eTimer_2 Input/Output Data Channel 4 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[44] | 0001 | SIN | DSPI1 | DSPI 1 Serial Data Input | I | | |
| | IMCR[75] | 0001 | ETC4 | eTimer_2 | eTimer_2 Input Data Channel 4 | I | | |
| | IMCR[181] | 0001 | REQ8 | SIUL2 | SIUL2 External Interrupt Source 8 | I | | |
| A[9] | MSCR[9] | 0000 (Default) | GPIO[9] | SIUL2-GPIO[9] | General Purpose IO A[9] | I/O | 134 | A4 |
| | | 0001 | CS1 | DSPI2 | DSPI 2 Peripheral Chip Select 1 | O | | |
| | | 0010 | ETC5 | eTimer_2 | eTimer_2 Input/Output Data Channel 5 | I/O | | |
| | | 0011 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[76] | 0001 | ETC5 | eTimer_2 | eTimer_2 Input Data Channel 5 | I | | |
| | IMCR[98] | 0010 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input 3 | I | | |
| | IMCR[83] | 0001 | FAULT0 | FlexPWM_0 | FlexPWM_0 Fault Input 0 | I | | |
| | IMCR[206] | 0011 | SENT_RX[1] | SENT_0 | SENT 0 Receiver channel 1 | I | | |
| A[10] | MSCR[10] | 0000 (Default) | GPIO[10] | SIUL2-GPIO[10] | General Purpose IO A[10] | I/O | 118 | B11 |
| | | 0001 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | O | | |
| | | 0010 | B0 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 0 | I/O | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[68] | 0010 | ETC3 | eTimer_1 | eTimer_1 Input Data Channel 3 | I | | |
| | IMCR[99] | 0001 | X3 | FlexPWM_0 | FlexPWM_0 Auxiliary Input 3 | I | | |
| | IMCR[137] | 0001 | FR_B_RX | FLEXRAY | FlexRay Channel B Receive Pin | I | | |
| D[3] | MSCR[51] | 0000 (Default) | GPIO[51] | SIUL2-GPIO[51] | General Purpose IO D[3] | I/O | 128 | A5 |
| | | 0001 | FR_B_TX | FLEXRAY | FlexRay Transmit Data Channel B | O | | |
| | | 0010 | ETC4 | eTimer_1 | eTimer_1 Input/Output Data Channel 4 | I/O | | |
| | | 0011 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[69] | 0010 | ETC4 | eTimer_1 | eTimer_1 Input Data Channel 4 | I | | |
| | IMCR[97] | 0011 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input 3 | I | | |
| D[4] | MSCR[52] | 0000 (Default) | GPIO[52] | SIUL2-GPIO[52] | General Purpose IO D[4] | I/O | 129 | B7 |
| | | 0001 | FR_B_TXEN | FLEXRAY | FlexRay Transmit Enable Channel B | O | | |
| | | 0010 | ETC5 | eTimer_1 | eTimer_1 Input/Output Data Channel 5 | I/O | | |
| | | 0011 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[70] | 0011 | ETC5 | eTimer_1 | eTimer_1 Input Data Channel 5 | I | | |
| | IMCR[98] | 0011 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input 3 | I | | |
| D[5] | MSCR[53] | 0000 (Default) | GPIO[53] | SIUL2-GPIO[53] | General Purpose IO D[5] | I/O | 33 | M4 |
| | | 0001 | CS3 | DSPI0 | DSPI 0 Peripheral Chip Select 3 | O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0100 | SOUT | DSPI3 | DSPI 3 Serial Data Out | O | | |
| | | 0101-1111 | — | Reserved | — | — | | |
| | IMCR[85] | 0001 | FAULT2 | FlexPWM_0 | FlexPWM_0 Fault Input 2 | I | | |
| | IMCR[205] | 0001 | SENT_RX[0] | SENT0 | SENT 0 Receiver channel 0 | I | | |
| | IMCR[227] | 0001 | RX_D1 | ENET_0 | Ethernet MII/RMII receive data 1 | I | | |
| D[6] | MSCR[54] | 0000 (Default) | GPIO[54] | SIUL2-GPIO[54] | General Purpose IO D[6] | I/O | 34 | P3 |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0010 | CS5 | DSPI0 | DSPI 0 Peripheral Chip Select 5 | O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[72] | 0010 | ETC1 | eTimer_2 | eTimer_2 Input Data Channel 1 | I | | |
| | IMCR[101] | 0001 | FAULT1 | FlexPWM_1 | FlexPWM_1 Fault Input 1 | I | | |
| | IMCR[232] | 0001 | RX_ER | ENET_0 | Ethernet Receive Data Error | I | | |
| I[2] | MSCR[130] | 0000 (Default) | GPIO[130] | SIUL2-GPIO[130] | General Purpose IO I[2] | I/O | | D11 |
| | | 0001 | ETC2 | eTimer_2 | eTimer_2 Input/Output Data Channel 2 | I/O | | |
| | | 0010 | CS6 | DSPI0 | DSPI 0 Peripheral Chip Select 6 | O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[73] | 0011 | ETC2 | eTimer_2 | eTimer_2 Input Data Channel 2 | I | | |
| | IMCR[102] | 0001 | FAULT2 | FlexPWM_1 | FlexPWM_1 Fault Input 2 | I | | |
| I[3] | MSCR[131] | 0000 (Default) | GPIO[131] | SIUL2-GPIO[131] | General Purpose IO I[3] | I/O | | A10 |
| | | 0001 | ETC3 | eTimer_2 | eTimer_2 Input/Output Data Channel 3 | I/O | | |
| | | 0010 | CS7 | DSPI0 | DSPI 0 Peripheral Chip Select 7 | O | | |
| | | 0011 | EXT_TGR | CTU_0 | CTU0 External Trigger Output | O | | |
| | | 0100 | TIMER0 | ENET_0 | Ethernet TIMER Outputs 0 (Output Compare Events) | O | | |
| | | 0101-1111 | — | Reserved | — | — | | |
| | IMCR[74] | 0011 | ETC3 | eTimer_2 | eTimer_2 Input Data Channel 3 | I | | |
| | IMCR[103] | 0001 | FAULT3 | FlexPWM_1 | FlexPWM_1 Fault Input 3 | I | | |
| RDY_ B/I[4] | MSCR[132] | 0000 (Default) | GPIO[132] | SIUL2-GPIO[132] | General Purpose IO I[4] | I/O | | J2 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | NEX_RDY_B | NPC_WRAPPER | Nexus data ready for transfer (RDY_B) | O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| I[5][5] | MSCR[133] | 0000 (Default) | GPIO[133] | SIUL2-GPIO[133] | General Purpose IO I[5][10] | I/O | | N15 |
| | | 0001 | TXD | CAN2 | CAN 2 Transmit Pin | O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | LFAST_TXN | LFAST | SIPI/LFAST LVDS transmit negative terminal | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |

*Table continues on the next page...*

## Table 10. Peripheral muxing (continued)

| Destination peripheral | Destination functions | IMCR number | IMCR[SSS] field value | Source peripherals | Source functions |
|---|---|---|---|---|---|
| | | | 0100-1111 | — | Reserved |
| FlexPWM_0 | X2 | IMCR[96] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[10] |
| | | | 0010 | I/O-Pad | G[2] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_0 | A3 | IMCR[97] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[2] |
| | | | 0010 | I/O-Pad | C[10] |
| | | | 0011 | I/O-Pad | D[3] |
| | | | 0100 | I/O-Pad | G[6] |
| | | | 0101-1111 | — | Reserved |
| FlexPWM_0 | B3 | IMCR[98] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | A[3] |
| | | | 0010 | I/O-Pad | A[9] |
| | | | 0011 | I/O-Pad | D[4] |
| | | | 0100 | I/O-Pad | G[7] |
| | | | 0101-1111 | — | Reserved |
| FlexPWM_0 | X3 | IMCR[99] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | D[2] |
| | | | 0010 | I/O-Pad | D[6] |
| | | | 0011 | I/O-Pad | G[5] |
| | | | 0100-1111 | — | Reserved |
| FlexPWM_1 | FAULT0 | IMCR[100] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[0] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | FAULT1 | IMCR[101] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[1] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | FAULT2 | IMCR[102] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[2] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | FAULT3 | IMCR[103] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | I[3] |
| | | | 0010-1111 | — | Reserved |
| FlexPWM_1 | A0 | IMCR[105] | 0000 (Default) | — | Disable |
| | | | 0001 | I/O-Pad | C[13] |
| | | | 0010 | I/O-Pad | H[5] |
| | | | 0011-1111 | — | Reserved |
| FlexPWM_1 | B0 | IMCR[106] | 0000 (Default) | — | Disable |

*Table continues on the next page...*

- Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 6.0 V (10 hours, device in reset—no switching)
- Absolute maximum supply: $V_{DD\_HV\_ADREx}$ = 5.5 V (always)
- Absolute maximum ADC input pin voltage = 7.0 V (60 seconds lifetime), when $V_{DD\_HV}$ is connected to the 5 V
- Absolute maximum ADC input pin voltage = 6.5 V (always while respecting 5 mA maximum injection), when $V_{DD\_HV}$ is connected to the 5 V

## 3.4 Recommended operating conditions

**NOTE**

Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and DC electrical specifications for I/Os might not be guaranteed.

**Table 13. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_PMU}$[1] | 3.3 V voltage regulator supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_IO}$[2] | 3.3 V input/output supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_IO}$ | Input/output ground voltage | — | 0 | 0 | V |
| $V_{DD\_HV\_FLA}$[3] | 3.3 V flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_FLA}$ | Flash memory ground | — | 0 | 0 | V |
| $V_{DD\_HV\_OSC}$[4] | 3.3 V crystal oscillator amplifier supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_OSC}$ | 3.3 V crystal oscillator amplifier ground | — | 0 | 0 | V |
| $V_{DD\_HV\_ADRE0}$<br>$V_{DD\_HV\_ADRE1}$ | 3.3 V / 5.0 V ADC_0 high reference voltage<br>3.3 V / 5.0 V ADC_1 high reference voltage | $T_J \le 150°C$ | 3.15 to 5.5 | | V |
| $V_{DD\_HV\_ADRE0}$[5]<br>$V_{DD\_HV\_ADRE1}$ | 3.3 V / 5.0 V ADC_0 high reference voltage<br>3.3 V / 5.0 V ADC_1 high reference voltage | $150°C < T_J < 165°C$ (only for corresponding marked parts) | 3.15 to 5.25 | | V |
| $V_{SS\_HV\_ADRE0}$[5]<br>$V_{SS\_HV\_ADRE1}$ | ADC_0 ground and low reference voltage<br>ADC_1 ground and low reference voltage | — | 0 | 0 | V |
| $V_{DD\_HV\_ADV}$[6] | 3.3 V ADC supply voltage | — | 3.15 | 3.6 | V |
| $V_{SS\_HV\_ADV}$ | 3.3 V ADC supply ground | — | 0 | 0 | V |
| $V_{DD\_LV\_COR}$[7] | Core supply, 1.25 V +/-5% | — | 1.19 | 1.32 | V |
| $V_{DD\_LV\_CORx}$ | Internal supply voltage | — | — | — | V |
| $V_{SS\_LV\_CORx}$ | Internal reference voltage | — | 0 | 0 | V |
| $V_{DD\_LV\_PLL}$ | Internal PLL supply voltage | — | 1.19 | 1.32 | V |
| $V_{SS\_LV\_PLL}$ | Internal PLL reference voltage | — | 0 | 0 | V |
| $V_{DD\_LV\_NEXUS}$ | Aurora LVDS supply voltage | — | 1.19 | 1.32 | V |
| $V_{SS\_LV\_NEXUS}$ | Aurora LVDS supply ground | — | 0 | 0 | V |
| $V_{DD\_LV\_LFAST}$ | LFAST PLL supply voltage | — | 1.19 | 1.32 | V |
| $V_{SS\_LV\_LFAST}$ | LFAST PLL supply ground | — | 0 | 0 | V |
| $I_{IC}$ | DC injection current per pin[8, 9, 10] | Digital pins | –3.0 | 3.0 | mA |
| | | Analog pins | –3.0 | 3.0 | |

*Table continues on the next page...*

### Table 13. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V) (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| | | Shared analog pins | –3.6 | 3.6 | |
| $T_A$ | Ambient temperature under bias | $f_{CPU} \leq$ 200MHz | –40 | 135[11] | °C |
| $T_J$ | Junction temperature under bias | — | –40 | 165[12, 13] | °C |

1. The chip functions down to the point where LVD_PMC resets the chip. When the voltage drops below LVD_PMC, the chip resets.
2. The chip functions down to the point where LVD_IO resets the chip. When the voltage drops below LVD_IO, the chip resets.
3. The chip functions down to the point where LVD_FLASH resets the chip. When the voltage drops below LVD_FLASH, the chip resets.
4. The chip functions down to the point where LVD_OSC resets the chip. When the voltage drops below LVD_OSC, the chip resets.
5. $V_{DD\_HV\_ADRE0}$ and $V_{DD\_HV\_ADRE1}$ cannot be operated at different voltages and need to be supplied by the same voltage source.
6. The chip functions down to the point where LVD_ADC resets the chip. When the voltage drops below LVD_ADC, the chip resets.
7. The chip functions down to the point where LVD_CORE or up to the point where HVD_CORE resets the chip by default.
8. I/O and analog input specifications are valid only if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
9. Full device lifetime without performance degradation.
10. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
11. For a maximum $T_J$ of 150°C, the corresponding maximum $T_A$ is 125°C.
12. Some orderable parts have a maximum $T_J$ value of 150°C. See the device marking for the applicable temperature range.
13. For devices supporting the 165°C junction temperature option: Operation at 150°C < $T_J$ < 165°C is allowed for a maximum cumulative time of 200 hours over the device lifetime.

## 3.5 Thermal characteristics

### Table 14. Thermal characteristics for 144LQFP and 257MAPBGA packages

| Symbol | Parameter | Conditions | 144LQFP | 257MAPBGA | Unit |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient natural convection[2] | Single layer board - 1s | 39 | 45 | °C/W |
| | | Four layer board - 2s2p | 31 | 25 | |
| $R_{\theta JMA}$ | Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1] | Single layer board - 1s[3] | 31 | 36 | °C/W |
| | | Four layer board - 2s2p[4] | 25 | 21 | |
| $R_{\theta JB}$ | Thermal resistance junction-to-board[5] | — | 18 | 13 | °C/W |
| $R_{\theta JC}$ | Thermal resistance junction-to-case[6] | — | 8 | 8 | °C/W |
| $\Psi_{JT}$ | Junction-to-package-top natural convection[7] | — | 2 | 2 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
4. Per JEDEC JESD51-6 with the board horizontal.

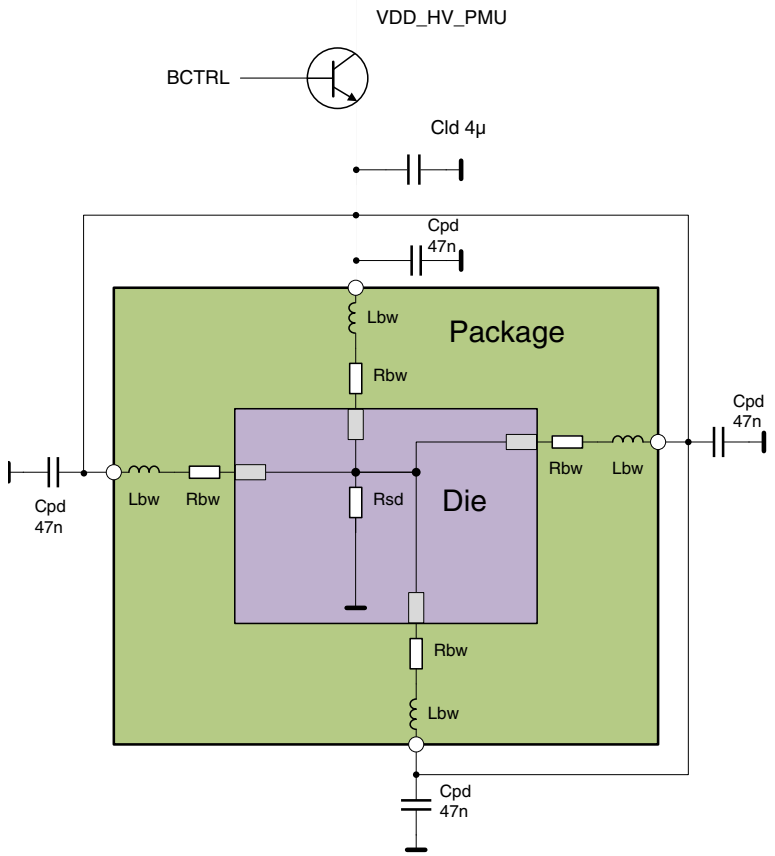



**Figure 4. Core supply decoupling and parasitics**

## 3.9 DC electrical characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 18 provides output driver characteristics FlexRay I/Os (SYM).
- Table 19 provides output driver characteristics for LFAST I/Os.

**NOTE**

See the FlexRay section for parameters dedicated to this interface.

**Table 18. FlexRay (SYM) configuration output buffer electrical characteristics**

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $R_{OH\_Y}$ | PMOS output impedance SYM configuration | Push Pull, $I_{OH}$ = 2 mA, $V_{OH} = V_{DD\_HV\_IO}$–(0.28...0.52V) | 35 | 50 | 65 | Ω |
| $R_{OL\_Y}$ | PMOS output impedance SYM configuration | Push Pull, $I_{OL}$ = 2 mA, $V_{OL}$ = 0.28...0.52 V | 35 | 50 | 65 | Ω |

*Table continues on the next page...*

## 3.15.1 Input equivalent circuit and ADC conversion characteristics

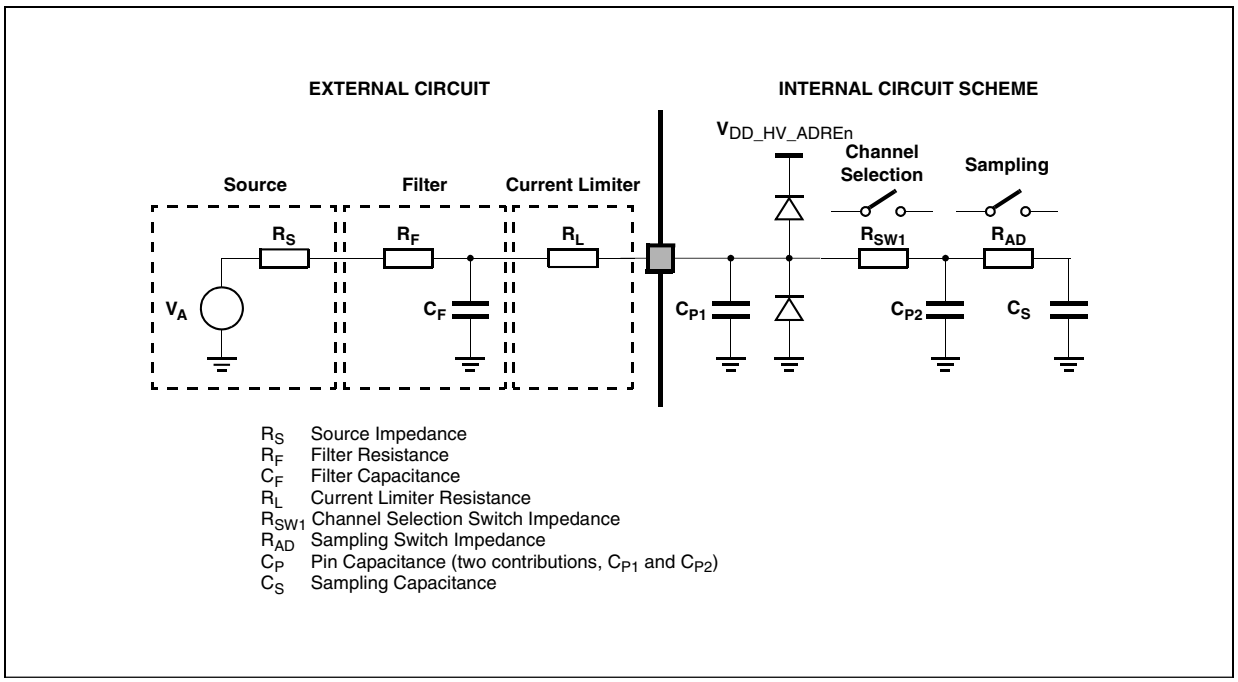



**Figure 8. Input equivalent circuit**

### NOTE

Unless noted otherwise, the specifications in Table 27 assume the use of 12-bit resolution (high accuracy, recommended): In ADC_CALBISTREG, set OPMODE to 110b.

**Table 27. ADC conversion characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.) | — | 20 | — | 80 | MHz |
| $f_s$ | Sampling frequency | — | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[3] | 80 MHz, 12-bit resolution | 250 | — | — | ns |
| | | 80 MHz, 12-bit resolution (high accuracy, recommended) | 250 | — | — | |
| $t_{conv}$ | Conversion time[4] | 80 MHz, 12-bit resolution | 650 | — | — | ns |
| | | 80 MHz, 12-bit resolution (high accuracy, recommended) | 700 | — | — | |
| $C_S$ | ADC input sampling capacitance | — | — | 3 | 5 | pF |
| $C_{P1}$[5] | ADC input pin capacitance 1 | — | — | — | 5[6] | pF |

*Table continues on the next page...*

## Table 27. ADC conversion characteristics (continued)

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{P2}$[5] | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| $R_{SW1}$[5] | Internal resistance of analog source | $V_{REF}$ range = 4.5 to 5.5 V | — | — | 0.3 | kΩ |
| | | $V_{REF}$ range = 3.15 to 3.6 V | — | — | 875 | Ω |
| $R_{AD}$[5] | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity | — | –2 | — | 2 | LSB |
| DNL | Differential non-linearity | — | –1 | — | 1 | LSB |
| OFS | Offset error | — | –4 | — | 4 | LSB |
| GNE | Gain error | — | –4 | — | 4 | LSB |
| Input (single ADC channel) | Max leakage | 150 °C | — | — | 250 | nA |
| | Max positive/negative injection | — | –3 | — | 3 | mA |
| Input (double ADC channel) | Max leakage | 150 °C | — | — | 300 | nA |
| | Max positive/negative injection | $\lvert V_{REF\_AD0} - V_{REF\_AD1} \rvert$ < 150mV | –3.6 | — | 3.6 | mA |
| SNR | Signal-to-noise ratio | $V_{REF}$ = 3.3 V, Fin < 125kHz | 67 | — | — | dB |
| SNR[7] | Signal-to-noise ratio | $V_{REF}$ = 5.0 V, Fin < 125kHz | 69 | — | — | dB |
| THD | Total harmonic distortion | Fin ≤ 125 kHz | 65 | 70 | — | dB |
| ENOB | Effective number of bits | Fin < 125 kHz | 10.5 | — | — | bits |
| SINAD | Signal-to-noise and distortion | See ENOB | (6.02 * ENOB) + 1.76 | | | dB |
| $TUE_{IS1WINJ}$ | Total unadjusted error for IS1WINJ (single ADC channels) | Without current injection | –6 | — | 6 | LSB |
| $TUE_{IS1WINJ}$ | Total unadjusted error for IS1WINJ (single ADC channels) | Current injection: ±3 mA for each channel, max 3 channels | –8 | — | 8 | LSB |

1. $V_{DD\_HV\_IO}$ = 3.3 V -5%,+10%, $T_J$ = –40 to +165 °C, unless otherwise specified, and analog input voltage from $V_{AGND}$ to $V_{AREF}$
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
4. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 2.
6. For the 144-pin package.
7. Test conditions have an influence on the achieved performance. Please contact FSL personnel to share the conditions for these results.

**NOTE**

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

### 3.16.1.2 Flash memory Array Integrity and Margin Read specifications

**Table 29. Flash memory Array Integrity and Margin Read specifications**

| Symbol | Characteristic | Min | Typical | Max[1] | Units[2] |
|---|---|---|---|---|---|
| $t_{ai16kseq}$ | Array Integrity time for sequential sequence on 16 KB block. | — | — | 512 x Tperiod x Nread | — |
| $t_{ai32kseq}$ | Array Integrity time for sequential sequence on 32 KB block. | — | — | 1024 x Tperiod x Nread | — |
| $t_{ai64kseq}$ | Array Integrity time for sequential sequence on 64 KB block. | — | — | 2048 x Tperiod x Nread | — |
| tai256kseq | Array Integrity time for sequential sequence on 256 KB block. | — | — | 8192 x Tperiod x Nread | — |
| $t_{mr16kseq}$ | Margin Read time for sequential sequence on 16 KB block. | 73.81 | — | 110.7 | µs |
| $t_{mr32kseq}$ | Margin Read time for sequential sequence on 32 KB block. | 128.43 | — | 192.6 | µs |
| $t_{mr64kseq}$ | Margin Read time for sequential sequence on 64 KB block. | 237.65 | — | 356.5 | µs |
| $t_{mr256kseq}$ | Margin Read time for sequential sequence on 256 KB block. | 893.01 | — | 1,339.5 | µs |

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

### 3.16.1.3 Flash memory module life specifications

**Table 30. Flash memory module life specifications**

| Symbol | Characteristic | Conditions | Min | Typical | Units |
|---|---|---|---|---|---|
| Array P/E cycles | Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1] | — | 250,000 | — | P/E cycles |
| | Number of program/erase cycles per block for 256 KB blocks.[2] | — | 1,000 | 250,000 | P/E cycles |
| Data retention | Minimum data retention. | Blocks with 0 - 1,000 P/E cycles. | 50 | — | Years |
| | | Blocks with 100,000 P/E cycles. | 20 | — | Years |
| | | Blocks with 250,000 P/E cycles. | 10 | — | Years |

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

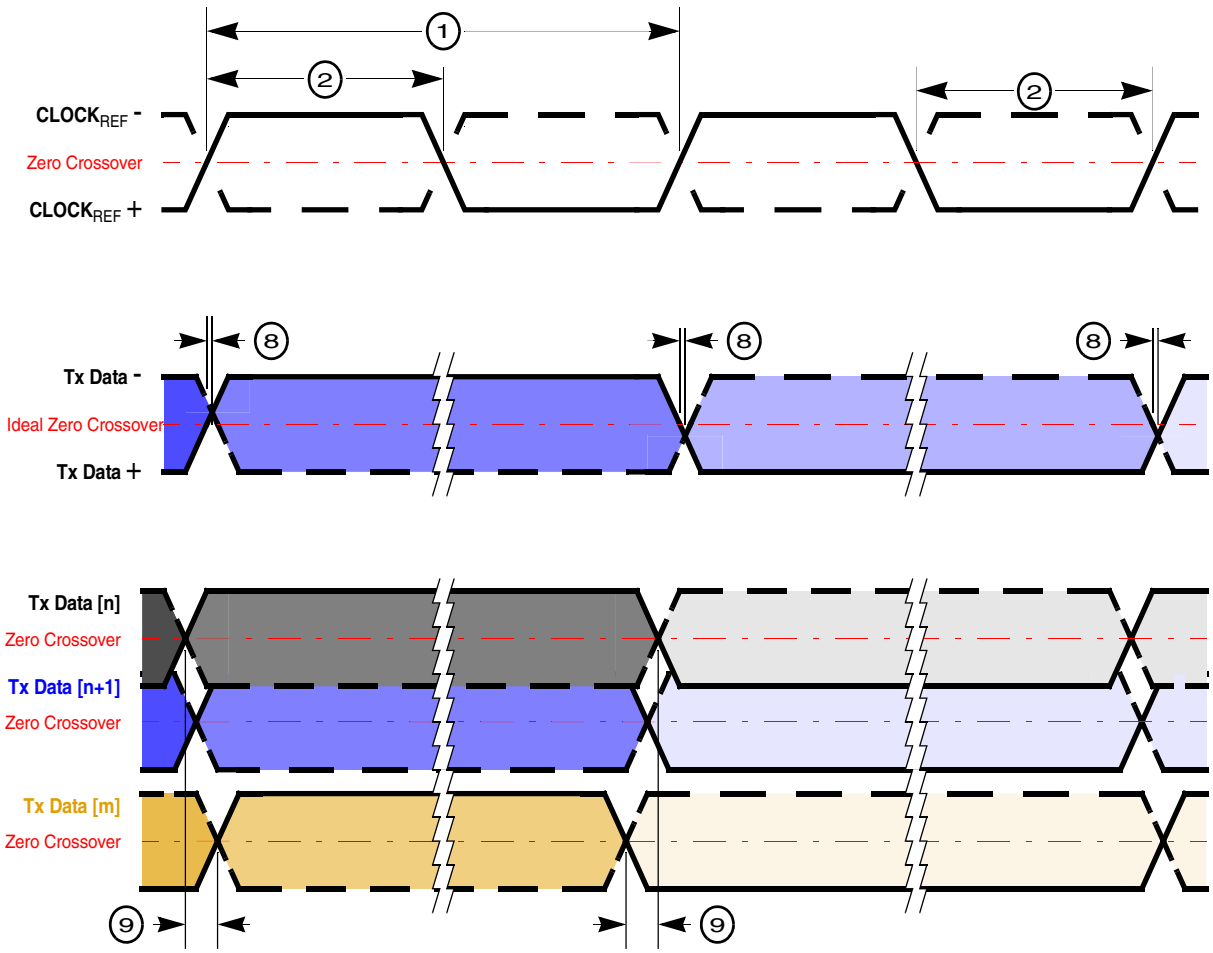



**Figure 18. Nexus Aurora timings**

Rise/fall timing for the Nexus Aurora debug port reference clock must conform to the area between the minimum and maximum value ranges shown in the following receiver "eye" diagram.

**Table 48. SPI timing (continued)**

| # | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | | Master (MTFE = 1, CPHA = 0) | –4 | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –4 | — | |

1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. P is the number of clock cycles added to delay the SPI input sample point and is software programmable.
3. $t_{SYS}$ is the period of the DSPI_CLKn clock, the input clock to the SPI module. Maximum frequency is 50 MHz (min $t_{SYS}$ = 20 ns).

**NOTE**

For numbers shown in the following figures, see Table 48.

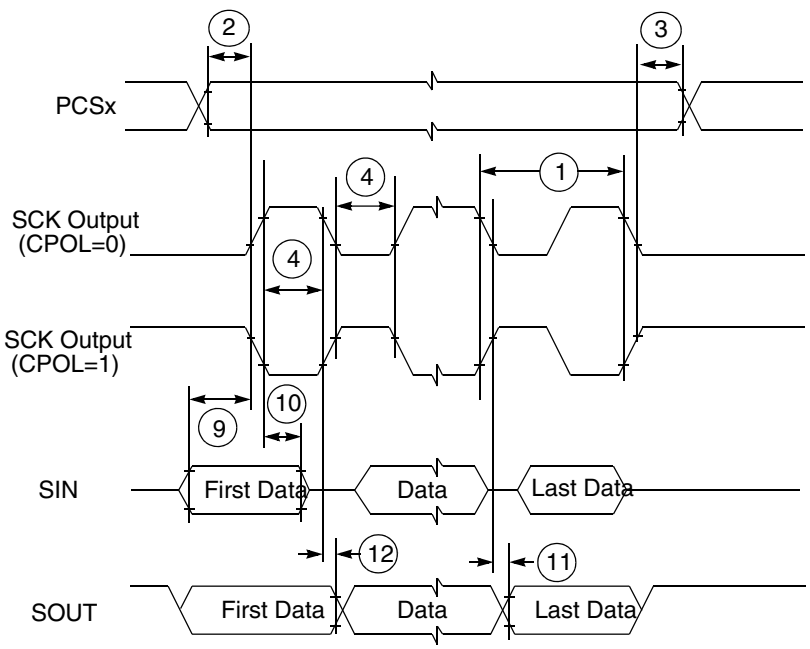



**Figure 21. DSPI classic SPI timing — master, CPHA = 0**

## Table 51. TxEN output characteristics[1]

| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $dCCTxEN_{RISE25}$ | Rise time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{FALL25}$ | Fall time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxEN_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, $T_J$ = –40 °C / 165 °C, TxEN pin load maximum 25 pF

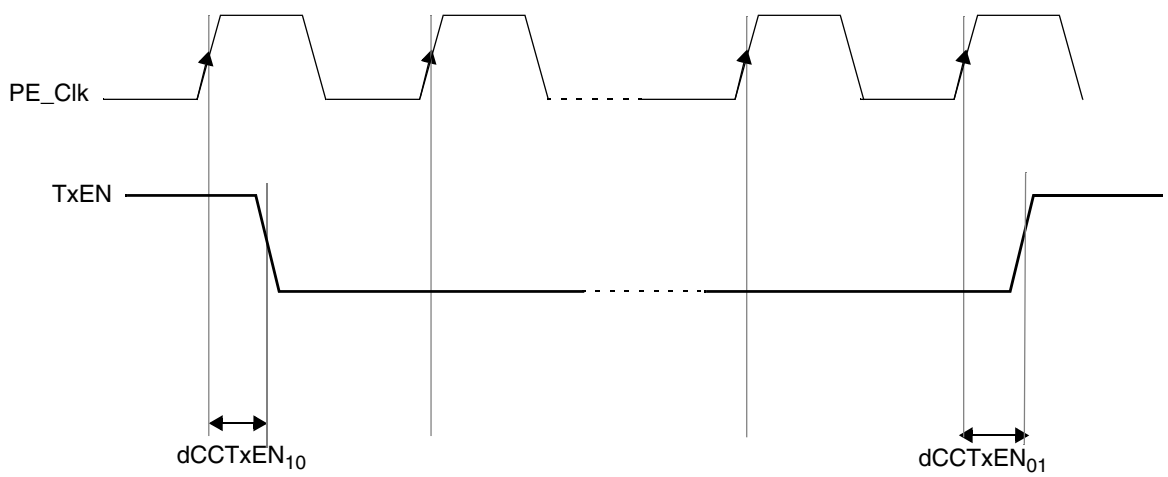



**Figure 34. FlexRay TxEN signal propagation delays**

### 3.19.7.3 TxD

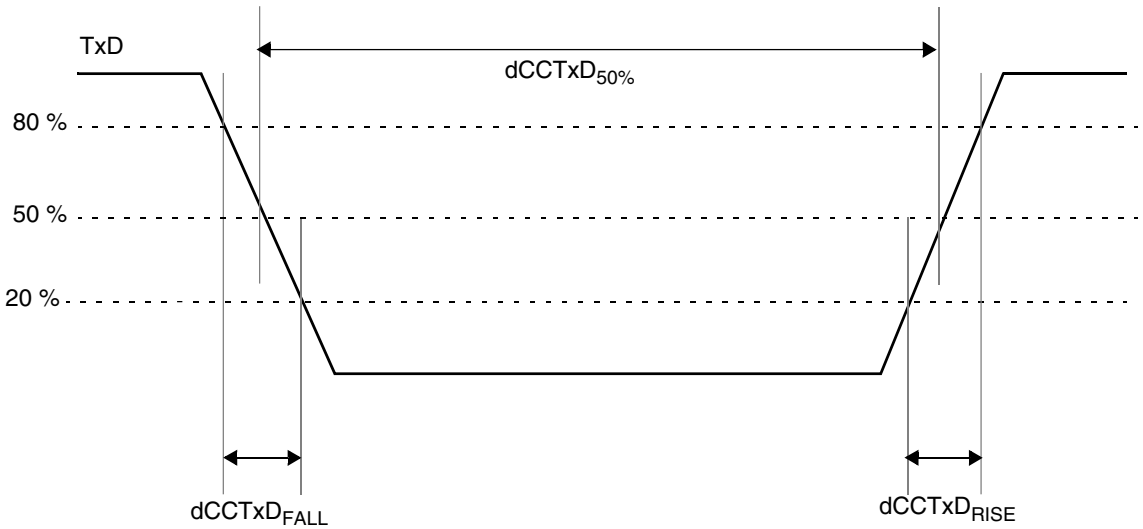
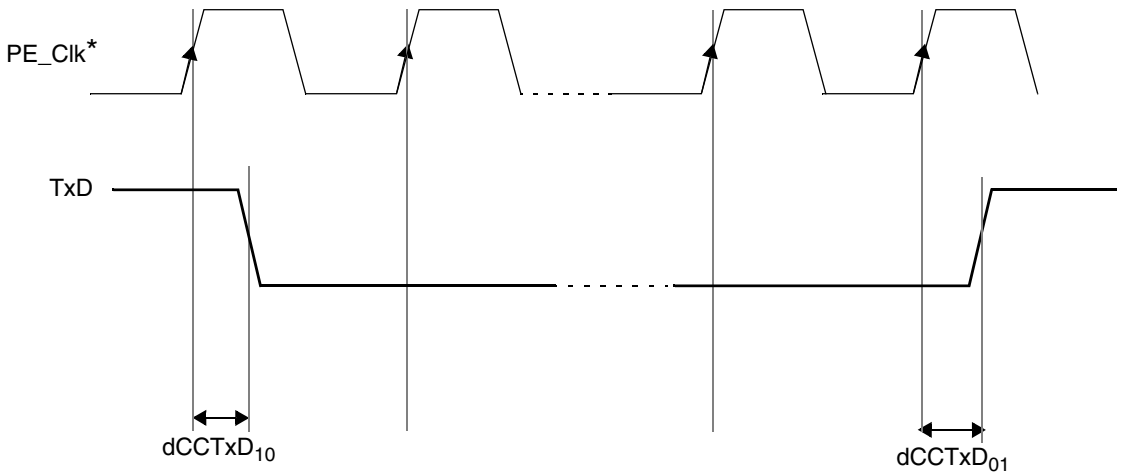



**Figure 35. FlexRay TxD signal**

**Table 52. TxD output characteristics**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| $dCCT_{xAsym}$ | Asymmetry of sending CC @ 25 pF load<br>(=$dCCTxD_{50\%}$ - 100 ns) | –2.45 | 2.45 | ns |
| $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ | Sum of Rise and Fall time of TxD signal at the output | — | 9 | ns |
| $dCCTxD_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxD_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, $T_J$ = –40 °C / 165 °C, TxD pin load maximum 25 pF




*FlexRay Protocol Engine Clock

**Figure 36. FlexRay TxD signal propagation delays**

### 3.19.7.4 RxD

**Table 53. RxD input characteristic**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| C_CCRxD | Input capacitance on RxD pin | — | 7 | pF |
| uCCLogic_1 | Threshold for detecting logic high | 35 | 70 | % |
| uCCLogic_0 | Threshold for detecting logic low | 30 | 65 | % |
| $dCCRxD_{01}$ | Sum of delay from actual input to the D input of the first FF, rising edge | — | 10 | ns |
| $dCCRxD_{10}$ | Sum of delay from actual input to the D input of the first FF, falling edge | — | 10 | ns |

1. All parameters specified for $V_{DD\_HV\_IO}$ = 3.3 V -5%, +10%, $T_J$ = –40 / 165 °C

### 3.19.7.5 Receiver asymmetry

**Table 54. Receiver asymmetry**

| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $dCCRxAsymAccept_{15}$ | Acceptance of asymmetry at receiving CC with 15 pF load (*) | –31.5 | +44.0 | ns |
| $dCCRxAsymAccept_{25}$ | Acceptance of asymmetry at receiving CC with 25 pF load (*) | –30.5 | +43.0 | ns |

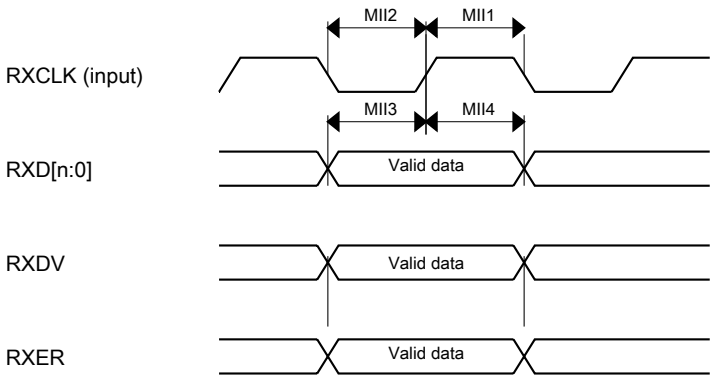



**Figure 38. RMII/MII receive signal timing diagram**

### 3.19.8.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

**Table 56. RMII signal switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| RMII1 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| RMII2 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| RMII3 | RXD[1:0], CRS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| RMII4 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 4 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

# 4 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 144-pin LQFP | 98ASS23177W |
| 257-ball MAPBGA | 98ASA00081D |

## Table 58. Revision history (continued)

| Revision | Date | Description of changes |
|---|---|---|
| | | • Changed Typical from 7 µs plus four system clock periods to 9.4 µs plus four system clock periods<br>• Changed Max from 9.1 µs plus four system clock periods to 11.5 µs plus four system clock periods<br><br>SGEN electrical characteristics<br>• Extensively updated the Table 37<br><br>LFAST interface electrical characteristics<br>• In Table 49 for row set $\lvert\Delta_{VOD\_DRF}\rvert$ deleted the ± from the Max, Typ, and Min values.<br>• In Table 49, removed the row set $V_{HYS\_DRF}$ |
| 6.1 | 10/2017 | • In Voltage regulator electrical characteristics changed the note, from "The device has to.....which drives the EXT_POR" to "When the external regulator.....regulator modes for safety operation". |