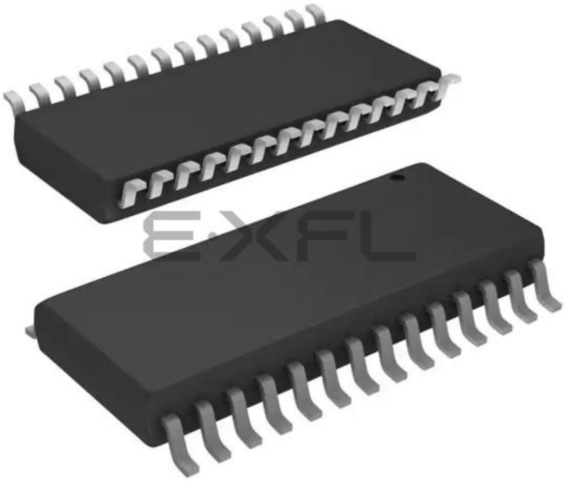
Microchip Technology - PIC18F2423T-I/SO Datasheet



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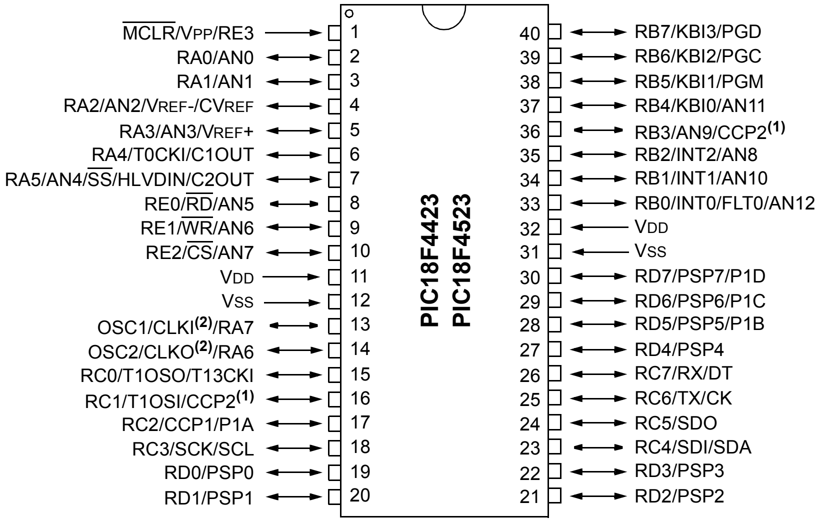
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

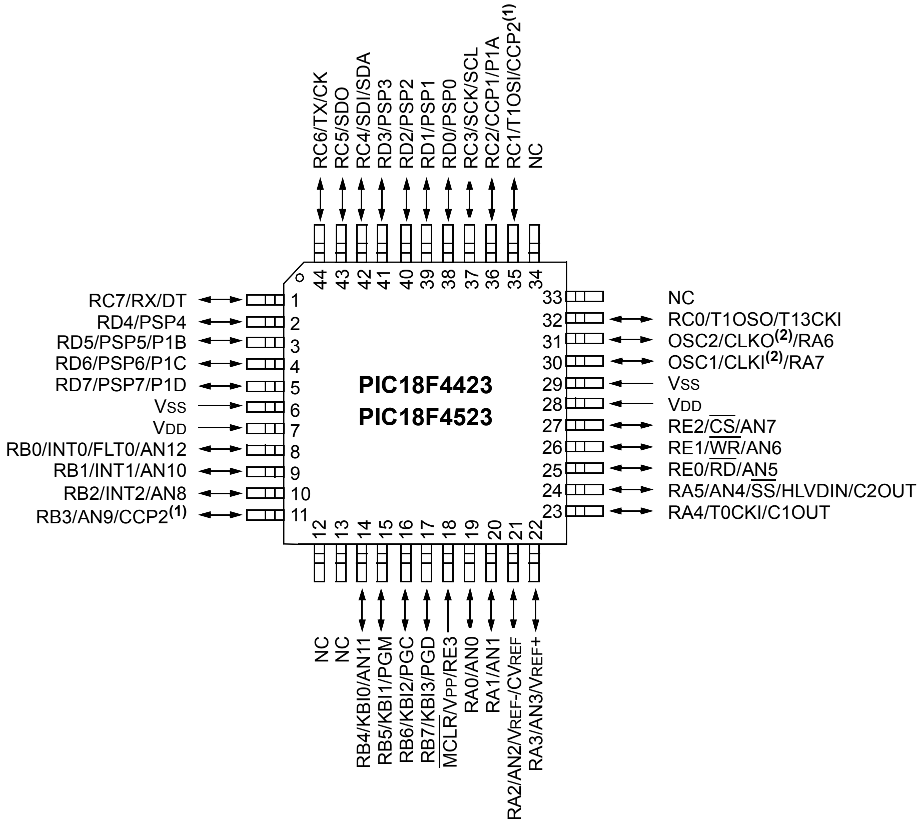
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2423t-i-so

Pin Diagrams (Continued)

40-Pin PDIP



44-Pin TQFP

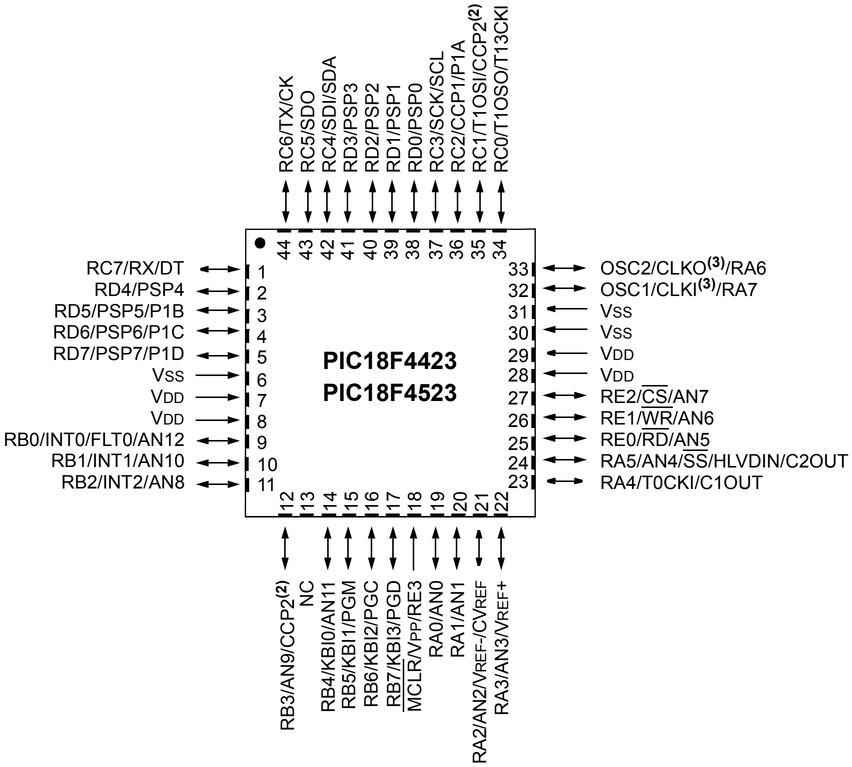


Note 1: RB3 is the alternate pin for CCP2 multiplexing.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 “Oscillator Configurations”** of the *“PIC18F2420/2520/4420/4520 Data Sheet”* (DS39631).

Pin Diagrams (Continued)

44-Pin QFN(1)



Note 1: It is recommended to connect the bottom pad of QFN package parts to VSS.

2: RB3 is the alternate pin for CCP2 multiplexing.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 “Oscillator Configurations”** of the *“PIC18F2420/2520/4420/4520 Data Sheet”* (DS39631).

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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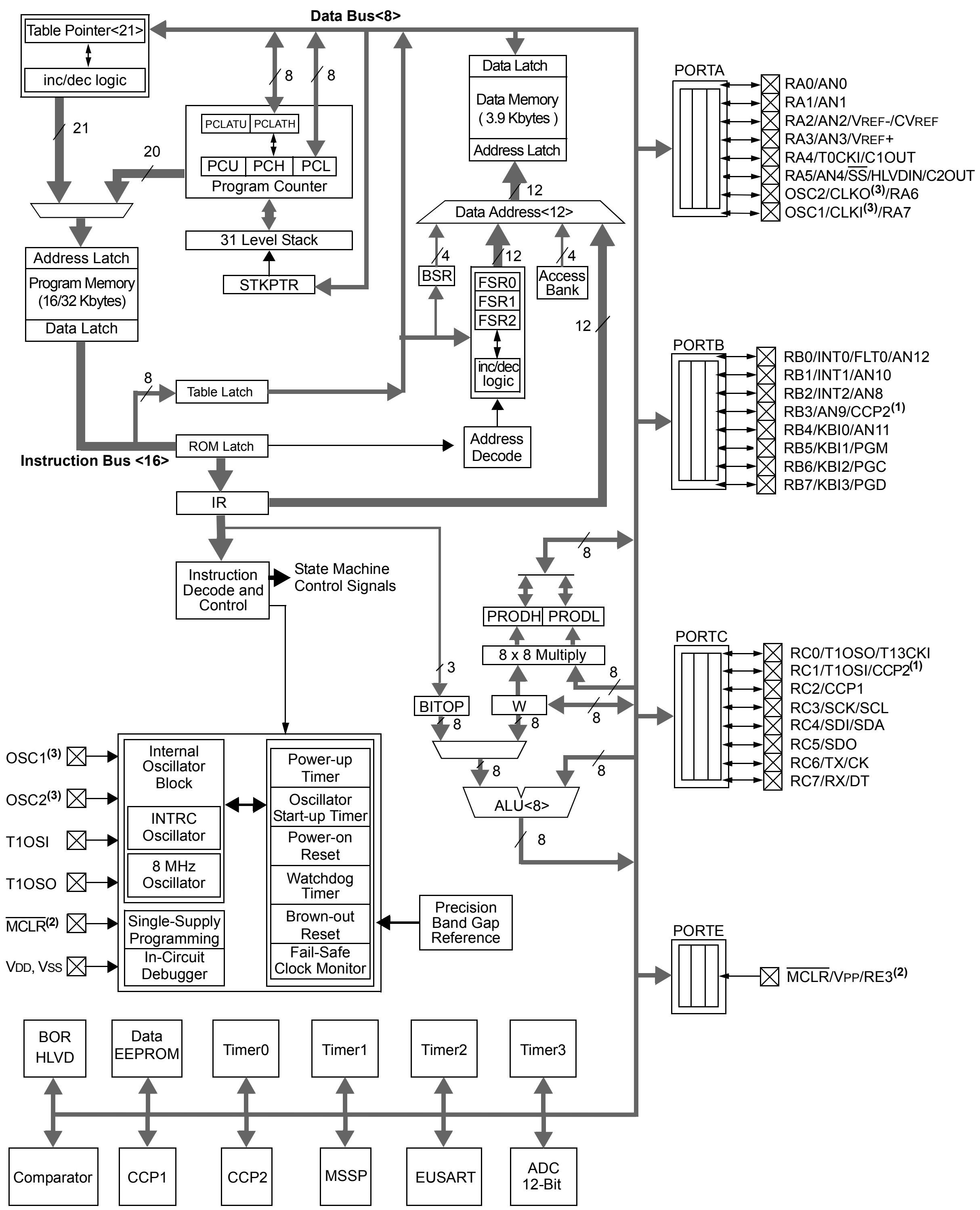
FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM



Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

2: RE3 is only available when MCLR functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
					PORTA is a bidirectional I/O port.
RA0/AN0	2	27			
RA0			I/O	TTL	Digital I/O.
AN0			I	Analog	Analog Input 0.
RA1/AN1	3	28			
RA1			I/O	TTL	Digital I/O.
AN1			I	Analog	Analog Input 1.
RA2/AN2/VREF-/CVREF	4	1			
RA2			I/O	TTL	Digital I/O.
AN2			I	Analog	Analog Input 2.
VREF-			I	Analog	A/D reference voltage (low) input.
CVREF			O	Analog	Comparator reference voltage output.
RA3/AN3/VREF+	5	2			
RA3			I/O	TTL	Digital I/O.
AN3			I	Analog	Analog Input 3.
VREF+			I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT	6	3			
RA4			I/O	ST	Digital I/O.
T0CKI			I	ST	Timer0 external clock input.
C1OUT			O	—	Comparator 1 output.
RA5/AN4/$\overline{SS}$/HLVDIN/ C2OUT	7	4			
RA5			I/O	TTL	Digital I/O.
AN4			I	Analog	Analog Input 4.
$\overline{SS}$			I	TTL	SPI slave select input.
HLVDIN			I	Analog	High/Low-Voltage Detect input.
C2OUT			O	—	Comparator 2 output.
RA6					See the OSC2/CLKO/RA6 pin.
RA7					See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
I^2C = I^2C™/SMBus
CMOS = CMOS compatible input or output
I = Input
P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	11	8			
RC0			I/O	ST	Digital I/O.
T1OSO			O	—	Timer1 oscillator output.
T13CKI			I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	12	9			
RC1			I/O	ST	Digital I/O.
T1OSI			I	Analog	Timer1 oscillator input.
CCP2(2)			I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1	13	10			
RC2			I/O	ST	Digital I/O.
CCP1			I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
RC3/SCK/SCL	14	11			
RC3			I/O	ST	Digital I/O.
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL			I/O	I^{2}C	Synchronous serial clock input/output for I^{2}C™ mode.
RC4/SDI/SDA	15	12			
RC4			I/O	ST	Digital I/O.
SDI			I	ST	SPI data in.
SDA			I/O	I^{2}C	I^{2}C data I/O.
RC5/SDO	16	13			
RC5			I/O	ST	Digital I/O.
SDO			O	—	SPI data out.
RC6/TX/CK	17	14			
RC6			I/O	ST	Digital I/O.
TX			O	—	EUSART asynchronous transmit.
CK			I/O	ST	EUSART synchronous clock (see related RX/DT).
RC7/RX/DT	18	15			
RC7			I/O	ST	Digital I/O.
RX			I	ST	EUSART asynchronous receive.
DT			I/O	ST	EUSART synchronous data (see related TX/CK).
RE3	—	—	—	—	See $\overline{\text{MCLR}}$/VPP/RE3 pin.
VSS	8, 19	5, 16	P	—	Ground reference for logic and I/O pins.
VDD	20	17	P	—	Positive supply for logic and I/O pins.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
I^{2}C = I^{2}C™/SMBus
CMOS = CMOS compatible input or output
I = Input
P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/$\overline{\text{RD}}$/AN5	8	25	25			
RE0				I/O	ST	Digital I/O.
$\overline{\text{RD}}$				I	TTL	Read control for Parallel Slave Port (see also $\overline{\text{WR}}$ and $\overline{\text{CS}}$ pins).
AN5				I	Analog	Analog Input 5.
RE1/$\overline{\text{WR}}$/AN6	9	26	26			
RE1				I/O	ST	Digital I/O.
$\overline{\text{WR}}$				I	TTL	Write control for Parallel Slave Port (see $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins).
AN6				I	Analog	Analog Input 6.
RE2/$\overline{\text{CS}}$/AN7	10	27	27			
RE2				I/O	ST	Digital I/O.
$\overline{\text{CS}}$				I	TTL	Chip select control for Parallel Slave Port (see related $\overline{\text{RD}}$ and $\overline{\text{WR}}$).
AN7				I	Analog	Analog Input 7.
RE3	—	—	—	—	—	See $\overline{\text{MCLR}}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
NC	—	13	12, 13, 33, 34	—	—	No connect.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
I^2C = I^2C™/SMBus
CMOS = CMOS compatible input or output
I = Input
P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

NOTES:

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

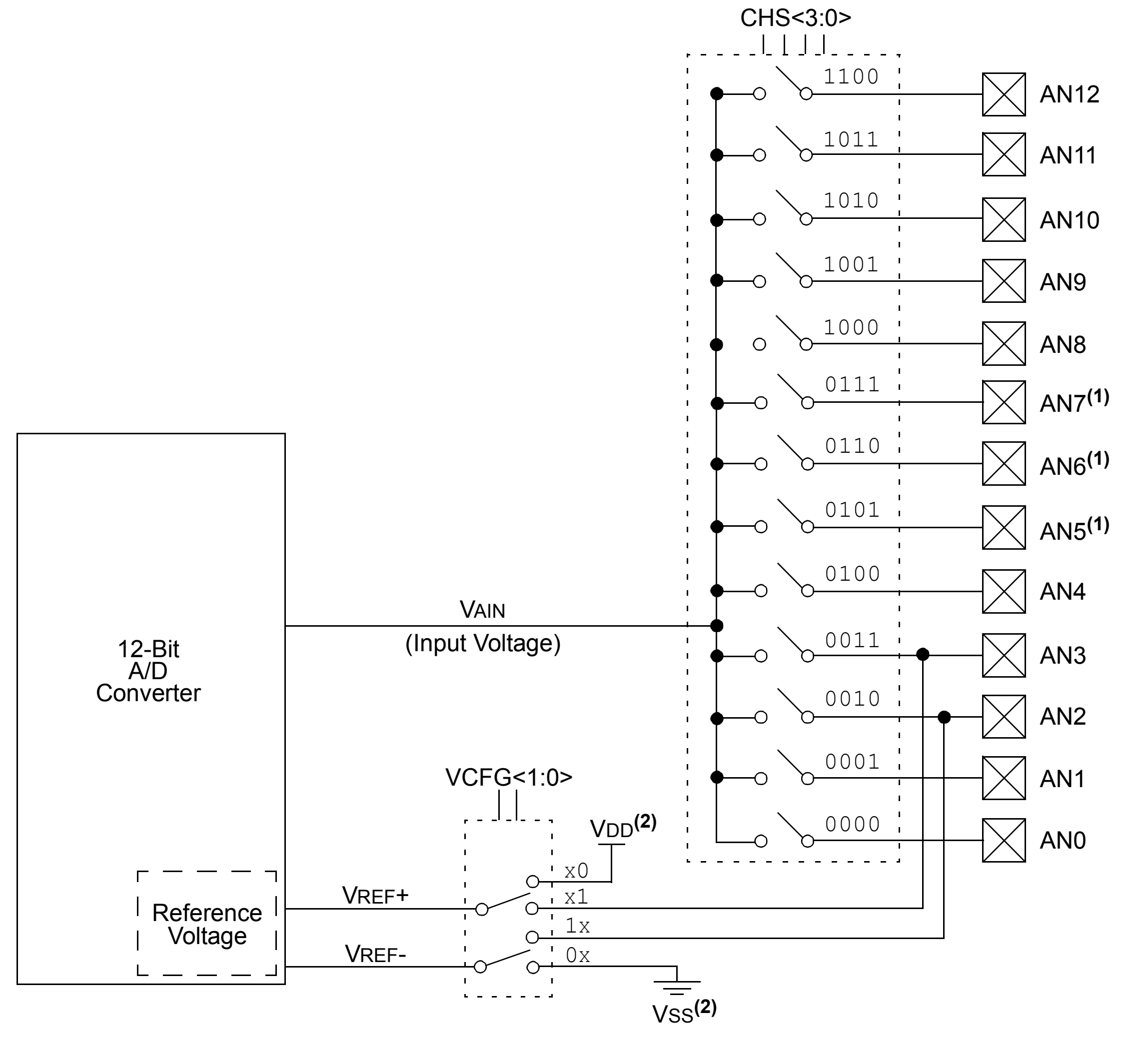
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM



Note 1: Channels, AN5 through AN7, are not available on PIC18F2423/2523 devices.

2: I/O pins have diode protection to VDD and VSS.

The value in the ADRESH:ADRESL registers is unknown following POR and BOR Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**.

After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/$\overline{\text{DONE}}$ bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on the A/D module (ADCON0)
2. Configure the A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>).
5. Wait for the A/D conversion to complete by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR

   - Waiting for the A/D interrupt
6. Read the A/D Result registers (ADRESH:ADRESL) and clear the ADIF bit, if required.
7. For the next conversion, go to step 1 or step 2, as required.

   The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

FIGURE 2-2: A/D TRANSFER FUNCTION

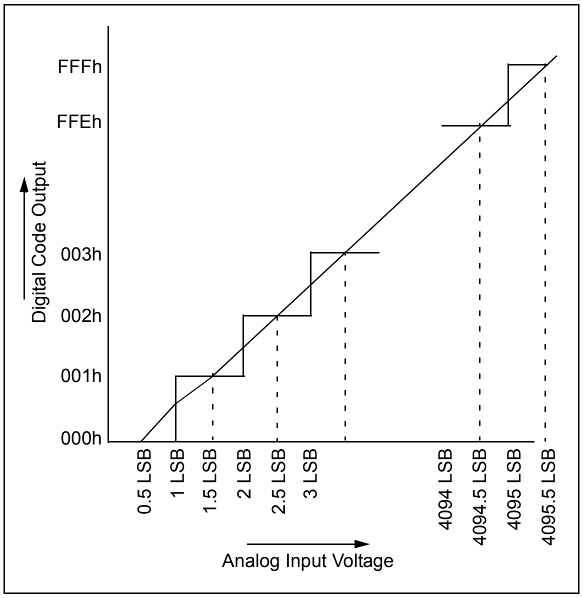
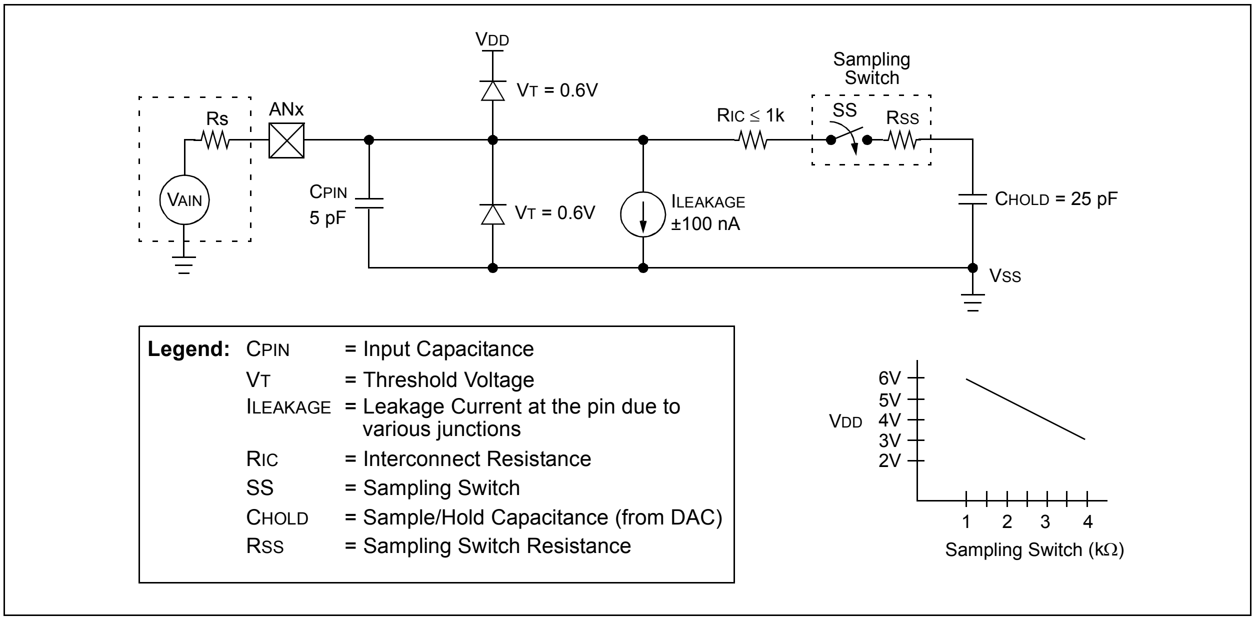


FIGURE 2-3: ANALOG INPUT MODEL



2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS<2:0> bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT<2:0> bits do not need to be adjusted as the ADCS<2:0> bits adjust the T_{AD} time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D F_{RC} clock to be selected. If bits, ACQT<2:0>, are set to '`000`' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

3: The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG<3:0> bits in ADCON1 are reset.

3.0 SPECIAL FEATURES OF THE CPU

Note:	For additional details on the Configuration bits, refer to **Section 23.1 "Configuration Bits" in** the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631). Device ID information presented in this section is for the PIC18F2423/2523/4423/4523 devices only.

3.1 Device ID Registers

The Device ID registers are read-only registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1[(1)]	DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0	`xxxx xxxx`[(2)]
3FFFFFh	DEVID2[(1)]	DEV11	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	`xxxx xxxx`[(2)]

Legend: `x` = unknown, `u` = unchanged, — = unimplemented. Shaded cells are unimplemented, read as '`0`'.

Note 1: DEVID registers are read-only and cannot be programmed by the user.

2: See Register 3-1 and Register 3-2 for DEVID1 and DEVID2 values.

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-4	**DEV<3:0>:** Device ID bits `1101` = PIC18F4423 `1001` = PIC18F4523 `0101` = PIC18F2423 `0001` = PIC18F2523
bit 3-0	**REV<3:0>:** Revision ID bits These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV11(1)	DEV10(1)	DEV9(1)	DEV8(1)	DEV7(1)	DEV6(1)	DEV5(1)	DEV4(1)
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-0 **DEV<11:4>:** Device ID bits(1)

These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number.
`0001 0001` = PIC18F2423/2523 devices
`0001 0000` = PIC18F4423/4523 devices

Note 1: These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.

4.0 ELECTRICAL CHARACTERISTICS

Note:	Other than some basic data, this section documents only the PIC18F2423/2523/4423/4523 devices' specifications that differ from those of the PIC18F2420/2520/4420/4520 devices. For detailed information on the electrical specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

Absolute Maximum Ratings(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS **(Note 2)**	0V to +13.25V
Total power dissipation **(Note 1)**	1.0W
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

Note 1: Power dissipation is calculated as follows:
Pdis = VDD x {IDD – $\sum$ IOH} + $\sum$ {(VDD – VOH) x IOH} + $\sum$(VOL x IOL)

2: Voltage spikes below VSS at the $\overline{\text{MCLR}}$/VPP/RE3 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$/VPP/RE3 pin, rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

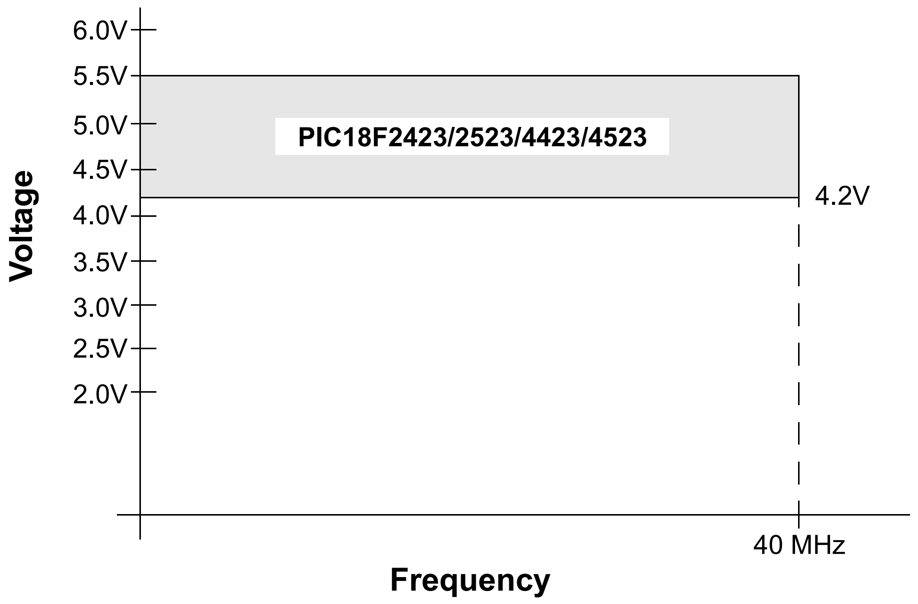


FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)

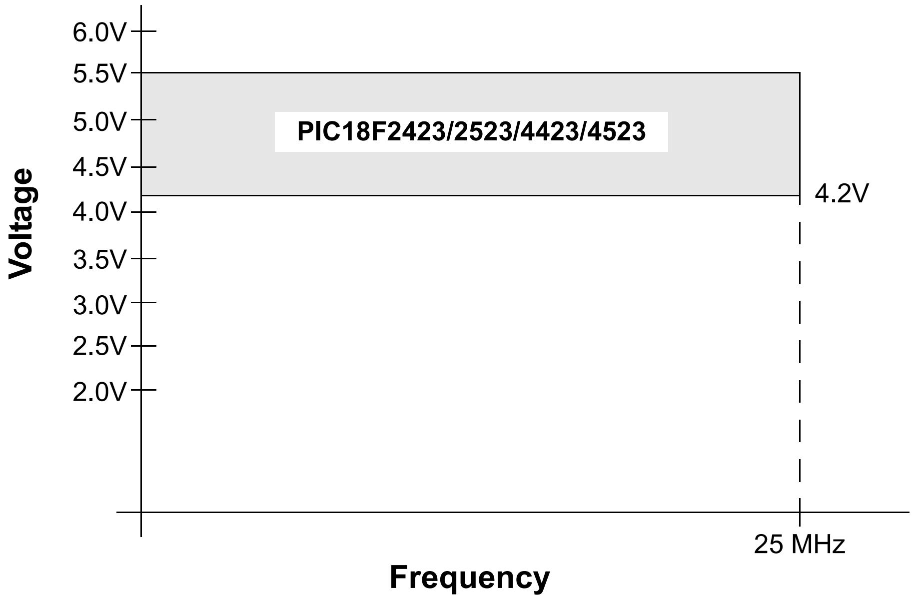
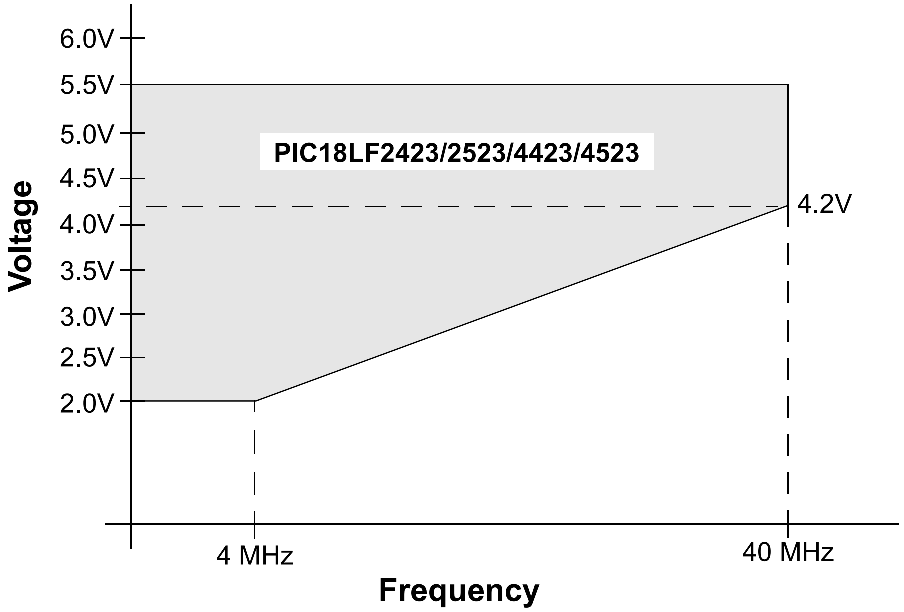


FIGURE 4-3: PIC18LF2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



$F_{MAX} = (16.36 \text{ MHz/V}) (V_{DDAPPMIN} - 2.0V) + 4 \text{ MHz}$

Note: $V_{DDAPPMIN}$ is the minimum voltage of the PIC® device in the application.

TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL)
PIC18LF2423/2523/4423/4523 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		ΔVREF ≥ 3.0V
A03	EIL	Integral Linearity Error	—	<±1	±2.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.0	LSB	VDD = 5.0V	
A04	EDL	Differential Linearity Error	—	<±1	+1.5/-1.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	+1.5/-1.0	LSB	VDD = 5.0V	
A06	EOFF	Offset Error	—	<±1	±5	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±3	LSB	VDD = 5.0V	
A07	EGN	Gain Error	—	<±1	±1.25	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.00	LSB	VDD = 5.0V	
A10	—	Monotonicity	Guaranteed[1]			—		VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V		For 12-bit resolution.
A21	VREFH	Reference Voltage High	VSS + 3.0V	—	VDD + 0.3V	V		For 12-bit resolution.
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	VDD – 3.0V	V		For 12-bit resolution.
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V		
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ		
A50	IREF	VREF Input Current[2]	— —	— —	5 150	μA μA		During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

5.0 PACKAGING INFORMATION

For packaging information, see **Section 28.0 “Packaging Information”** in the *“PIC18F2420/2520/4420/4520 Data Sheet”* (DS39631).

NOTES:

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available