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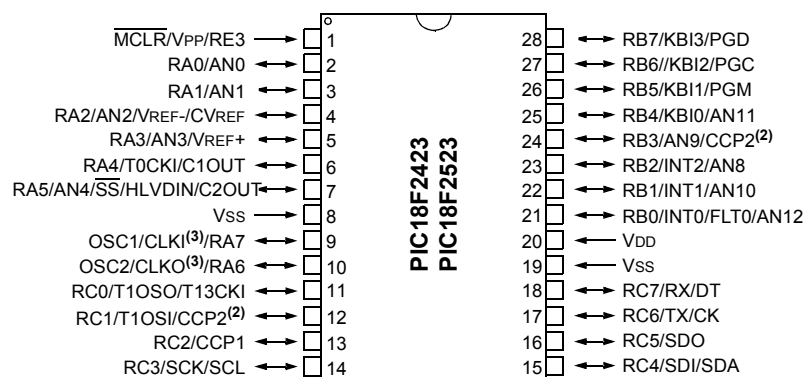
#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f2523-e-sp">https://www.e-xfl.com/product-detail/microchip-technology/pic18f2523-e-sp</a>

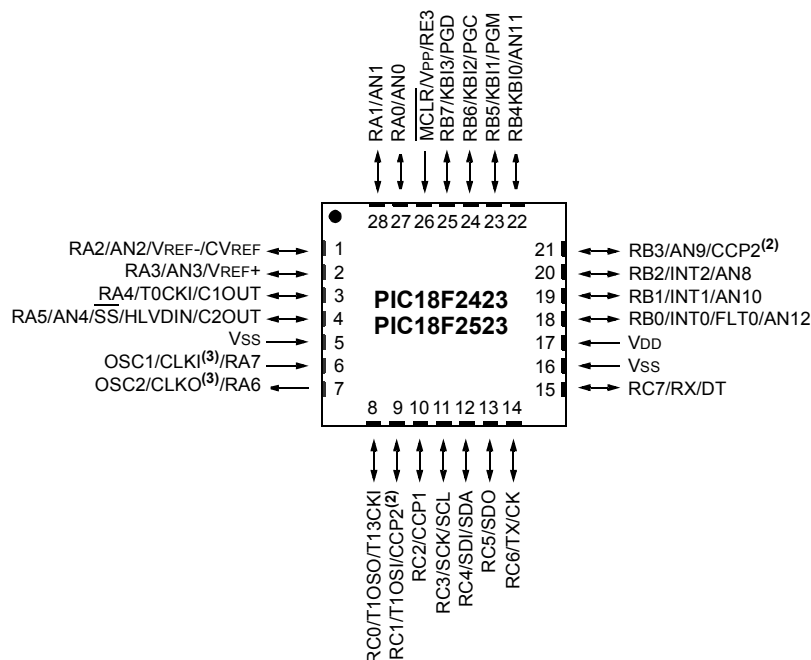
# PIC18F2423/2523/4423/4523

## Pin Diagrams

### 28-Pin PDIP, SOIC



### 28-Pin QFN<sup>(1)</sup>



- Note**
- 1: It is recommended to connect the bottom pad of QFN package parts to Vss.
  - 2: RB3 is the alternate pin for CCP2 multiplexing.
  - 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

## Table of Contents

1.0	Device Overview .....	9
2.0	12-Bit Analog-to-Digital Converter (A/D) Module .....	25
3.0	Special Features of the CPU .....	35
4.0	Electrical Characteristics .....	37
5.0	Packaging Information.....	43
	Appendix A: Revision History.....	45
	Appendix B: Device Differences .....	45
	Appendix C: Conversion Considerations .....	46
	Appendix D: Migration from Baseline to Enhanced Devices.....	46
	Appendix E: Migration from Mid-Range to Enhanced Devices .....	47
	Appendix F: Migration from High-End to Enhanced Devices.....	47
	Index .....	49
	The Microchip Web Site .....	51
	Customer Change Notification Service .....	51
	Customer Support.....	51
	Reader Response .....	52
	Product Identification System .....	53

# PIC18F2423/2523/4423/4523

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## 1.2 Other Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, thereby reducing code overhead.
- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-Programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it is possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18F2423/2523/4423/4523 family introduces an optional extension to the PIC18 instruction set that adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **Enhanced CCP module:** In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown, for disabling PWM outputs on interrupt or other select conditions, and auto-restart, to reactivate outputs once the condition has cleared.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **Extended Watchdog Timer (WDT):** This Enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 4.0 “Electrical Characteristics”** for time-out periods.

## 1.3 Details on Individual Family Members

Devices in the PIC18F2423/2523/4423/4523 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18F2423/4423 devices – 16 Kbytes
  - PIC18F2523/4523 devices – 32 Kbytes
- A/D Channels:
  - PIC18F2423/2523 devices – 10
  - PIC18F4423/4523 devices – 13
- I/O Ports:
  - PIC18F2423/2523 devices – Three bidirectional ports
  - PIC18F4423/4523 devices – Five bidirectional ports
- CCP and Enhanced CCP Implementation:
  - PIC18F2423/2523 devices – Two standard CCP modules
  - PIC18F4423/4523 devices – One standard CCP module and one ECCP module
- Parallel Slave Port – Present only on PIC18F4423/4523 devices

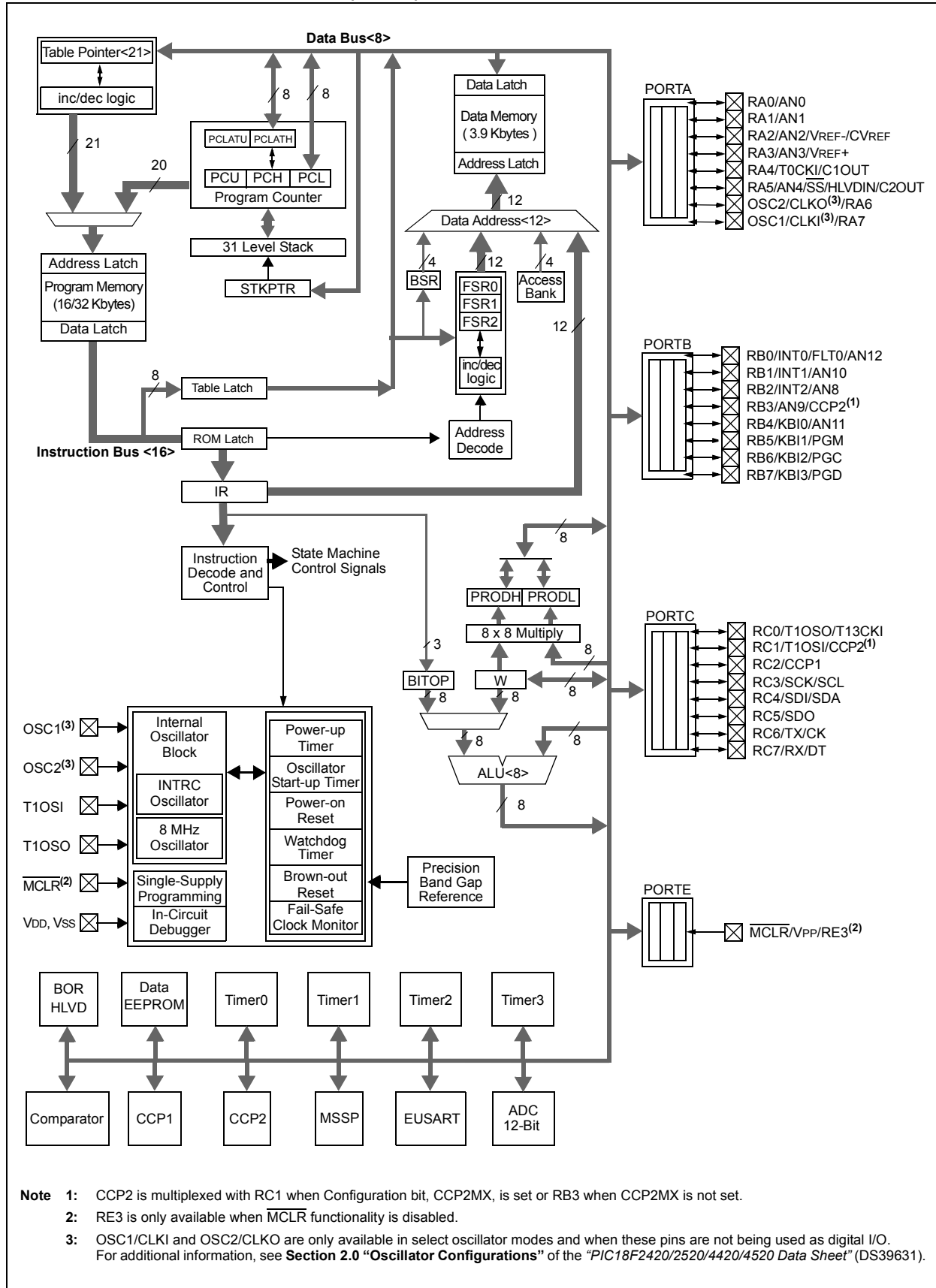
All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F2423/2523/4423/4523 family are available only as low-voltage devices, designated by “LF” (such as PIC18**LF**2423), and function over an extended VDD range of 2.0V to 5.5V.

# PIC18F2423/2523/4423/4523

**FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM**



# PIC18F2423/2523/4423/4523

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RC0/T1OSO/T13CKI	15	34	32	I/O	ST	PORTC is a bidirectional I/O port.  Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC0				O	—	
T1OSO				I	ST	
T13CKI						
RC1/T1OSI/CCP2	16	35	35	I/O	ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.
RC1				I	CMOS	
T1OSI				I/O	ST	
CCP2 <sup>(2)</sup>						
RC2/CCP1/P1A	17	36	36	I/O	ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output. Enhanced CCP1 output.
RC2				I/O	ST	
CCP1				O	—	
P1A						
RC3/SCK/SCL	18	37	37	I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC3				I/O	ST	
SCK				I/O	I <sup>2</sup> C	
SCL						
RC4/SDI/SDA	23	42	42	I/O	ST	Digital I/O. SPI data in. I <sup>2</sup> C data I/O.
RC4				I	ST	
SDI				I/O	I <sup>2</sup> C	
SDA						
RC5/SDO	24	43	43	I/O	ST	Digital I/O. SPI data out.
RC5				O	—	
SDO						
RC6/TX/CK	25	44	44	I/O	ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see related RX/DT).
RC6				O	—	
TX				I/O	ST	
CK						
RC7/RX/DT	26	1	1	I/O	ST	Digital I/O. EUSART asynchronous receive. EUSART synchronous data (see related TX/CK).
RC7				I	ST	
RX				I/O	ST	
DT						

**Legend:** TTL = TTL compatible input  
ST = Schmitt Trigger input with CMOS levels  
O = Output  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus  
CMOS = CMOS compatible input or output  
I = Input  
P = Power

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled.
RD0/PSP0	19	38	38	I/O	ST	Digital I/O.
RD0				I/O	TTL	Parallel Slave Port data.
PSP0						
RD1/PSP1	20	39	39	I/O	ST	Digital I/O.
RD1				I/O	TTL	Parallel Slave Port data.
PSP1						
RD2/PSP2	21	40	40	I/O	ST	Digital I/O.
RD2				I/O	TTL	Parallel Slave Port data.
PSP2						
RD3/PSP3	22	41	41	I/O	ST	Digital I/O.
RD3				I/O	TTL	Parallel Slave Port data.
PSP3						
RD4/PSP4	27	2	2	I/O	ST	Digital I/O.
RD4				I/O	TTL	Parallel Slave Port data.
PSP4						
RD5/PSP5/P1B	28	3	3	I/O	ST	Digital I/O.
RD5				I/O	TTL	Parallel Slave Port data.
PSP5				O	—	Enhanced CCP1 output.
P1B						
RD6/PSP6/P1C	29	4	4	I/O	ST	Digital I/O.
RD6				I/O	TTL	Parallel Slave Port data.
PSP6				O	—	Enhanced CCP1 output.
P1C						
RD7/PSP7/P1D	30	5	5	I/O	ST	Digital I/O.
RD7				I/O	TTL	Parallel Slave Port data.
PSP7				O	—	Enhanced CCP1 output.
P1D						

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

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NOTES:



# PIC18F2423/2523/4423/4523

## REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0 <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (VREF- source)

1 = VREF- (AN2)

0 = VSS

bit 4 **VCFG0:** Voltage Reference Configuration bit (VREF+ source)

1 = VREF+ (AN3)

0 = VDD

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

PCFG<3:0>	AN12	AN11	AN10	AN9	AN8	AN7 <sup>(2)</sup>	AN6 <sup>(2)</sup>	AN5 <sup>(2)</sup>	AN4	AN3	AN2	AN1	AN0
0000 <sup>(1)</sup>	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111 <sup>(1)</sup>	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O

**Note 1:** The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

**2:** AN5 through AN7 are only available on PIC18F4423/4523 devices.

# PIC18F2423/2523/4423/4523

## REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD<sup>(1)</sup>

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the **SLEEP** instruction to be executed before starting a conversion.

# PIC18F2423/2523/4423/4523

The value in the ADRESH:ADRESL registers is unknown following POR and BOR Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. To determine acquisition time, see **Section 2.1 “A/D Acquisition Requirements”**.

After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

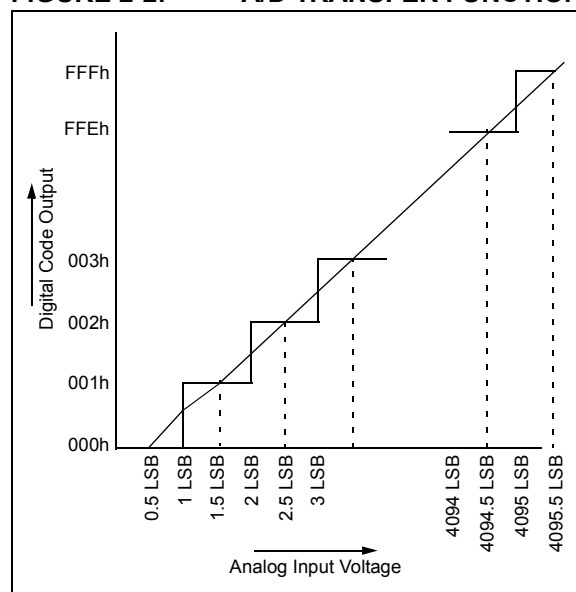
The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
  - Configure analog pins, voltage reference and digital I/O (ADCON1)
  - Select A/D input channel (ADCON0)
  - Select A/D acquisition time (ADCON2)
  - Select A/D conversion clock (ADCON2)
  - Turn on the A/D module (ADCON0)
2. Configure the A/D interrupt (if desired):
  - Clear ADIF bit
  - Set ADIE bit
  - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion by setting the GO/DONE bit (ADCON0<1>).

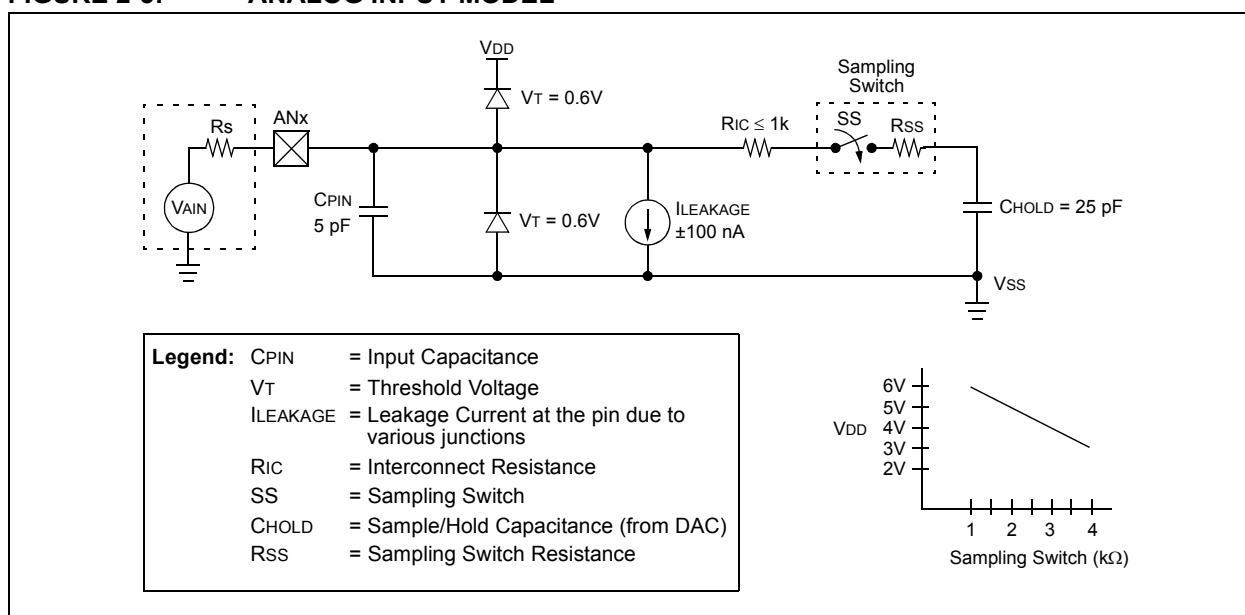
5. Wait for the A/D conversion to complete by either:
  - Polling for the GO/DONE bit to be cleared
 OR
  - Waiting for the A/D interrupt
6. Read the A/D Result registers (ADRESH:ADRESL) and clear the ADIF bit, if required.
7. For the next conversion, go to step 1 or step 2, as required.

The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**



**FIGURE 2-3: ANALOG INPUT MODEL**



## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition time is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-2: TAD vs. DEVICE OPERATING FREQUENCIES**

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 $\mu$ s
Operation	ADCS<2:0>	Maximum Fosc
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	40.00 MHz
RC <sup>(2)</sup>	x11	1.00 MHz <sup>(1)</sup>

**Note 1:** The RC source has a typical TAD time of 2.5  $\mu$ s.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the  $\text{ACQT}<2:0>$  bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set, the  $\text{ACQT}<2:0>$  bits have been set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means, the  $\text{ADRESH:ADRESL}$  registers will continue to contain the value of the last completed conversion (or the last value written to the  $\text{ADRESH:ADRESL}$  registers).

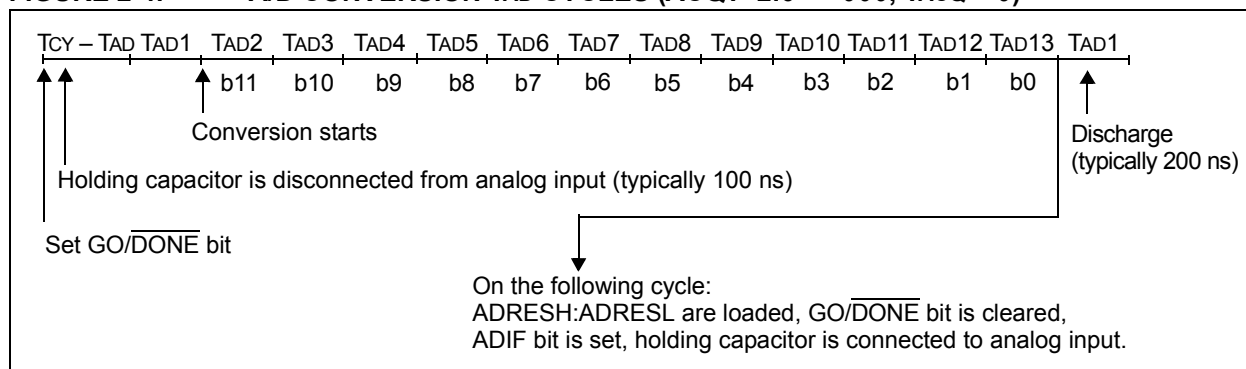
After the A/D conversion is completed or aborted, a 2  $\text{Tcy}$  wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 3 TAD after enabling the A/D before beginning an acquisition and conversion cycle.

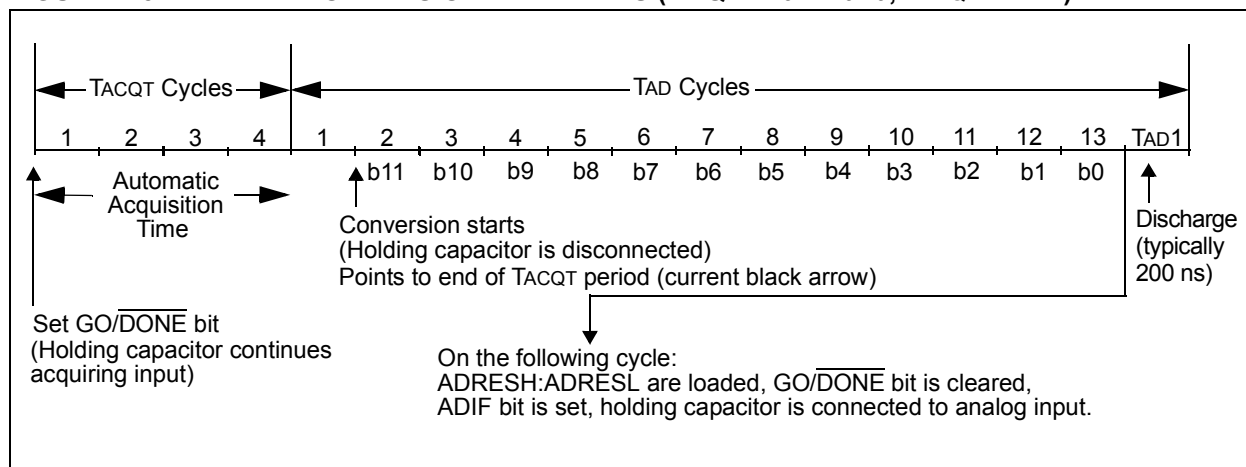
## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity-gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES ( $\text{ACQT}<2:0> = 000$ ,  $\text{Tacq} = 0$ )**



**FIGURE 2-5: A/D CONVERSION TAD CYCLES ( $\text{ACQT}<2:0> = 010$ ,  $\text{Tacq} = 4 \text{ TAD}$ )**



# PIC18F2423/2523/4423/4523

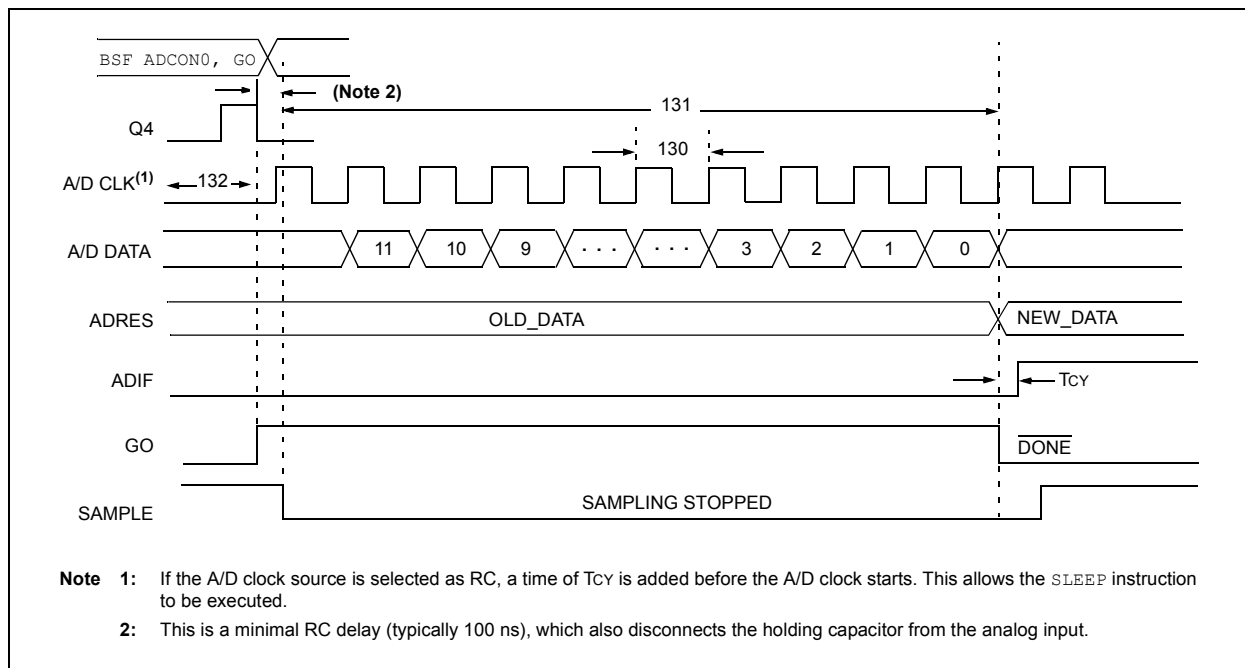
**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL)  
PIC18LF2423/2523/4423/4523 (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	$\pm 2.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.0$	LSB	$V_{DD} = 5.0V$	
A04	EDL	Differential Linearity Error	—	$<\pm 1$	$+1.5/-1.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$+1.5/-1.0$	LSB	$V_{DD} = 5.0V$	
A06	EOFF	Offset Error	—	$<\pm 1$	$\pm 5$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 3$	LSB	$V_{DD} = 5.0V$	
A07	EGN	Gain Error	—	$<\pm 1$	$\pm 1.25$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.00$	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed <sup>(1)</sup>			—		$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	$\Delta V_{REF}$	Reference Voltage Range ( $V_{REFH} - V_{REFL}$ )	3	—	$V_{DD} - V_{SS}$	V		For 12-bit resolution.
A21	$V_{REFH}$	Reference Voltage High	$V_{SS} + 3.0V$	—	$V_{DD} + 0.3V$	V		For 12-bit resolution.
A22	$V_{REFL}$	Reference Voltage Low	$V_{SS} - 0.3V$	—	$V_{DD} - 3.0V$	V		For 12-bit resolution.
A25	$V_{AIN}$	Analog Input Voltage	$V_{REFL}$	—	$V_{REFH}$	V		
A30	$Z_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	2.5	k $\Omega$		
A50	$I_{REF}$	$V_{REF}$ Input Current <sup>(2)</sup>	—	—	5	$\mu A$		During $V_{AIN}$ acquisition. During A/D conversion cycle.
			—	—	150	$\mu A$		

- Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
- Note 2:**  $V_{REFH}$  current is from the RA3/AN3/ $V_{REF+}$  pin or  $V_{DD}$ , whichever is selected as the  $V_{REFH}$  source.  $V_{REFL}$  current is from the RA2/AN2/ $V_{REF-}/CV_{REF}$  pin or  $V_{SS}$ , whichever is selected as the  $V_{REFL}$  source.

# PIC18F2423/2523/4423/4523

**FIGURE 4-4: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	μs	TOSC based, VREF ≥ 3.0V
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	μs	VDD = 3.0V; TOSC based, VREF full range
			PIC18FXXXX	—	1	μs	A/D RC mode
			PIC18LFXXXX	—	3	μs	VDD = 3.0V; A/D RC mode
131	TCNV	Conversion Time (not including acquisition time) <sup>(2)</sup>		13	14	TAD	
132	TACQ	Acquisition Time <sup>(3)</sup>		1.4	—	μs	
135	TSWC	Switching Time from Convert → Sample		—	(Note 4)		
137	TDIS	Discharge Time		0.2	—	μs	

**Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

**Note 2:** ADRES registers may be read on the following T<sub>cy</sub> cycle.

**Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (R<sub>s</sub>) on the input channels is 50Ω.

**Note 4:** On the following cycle of the device clock.

# PIC18F2423/2523/4423/4523

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NOTES:



# PIC18F2423/2523/4423/4523

## APPENDIX A: REVISION HISTORY

### Revision A (June 2006)

Original data sheet for PIC18F2423/2523/4423/4523 devices.

### Revision B (January 2007)

This revision includes updates to the packaging diagrams.

### Revision C (September 2009)

Electrical specifications updated. Preliminary condition status removed. Converted document to the "mini data sheet" format.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Program Memory (Bytes)	16384	32768	16384	32768
Program Memory (Instructions)	8192	16384	8192	16384
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**

# PIC18F2423/2523/4423/4523

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NOTES:

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# PIC18F2423/2523/4423/4523

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device	PIC18F2423 <sup>(1)</sup> , PIC18F2523 <sup>(1)</sup> , PIC18F4423T <sup>(2)</sup> , PIC18F4523T <sup>(2)</sup> ; VDD range 4.2V to 5.5V PIC18F2423 <sup>(1)</sup> , PIC18F2523 <sup>(1)</sup> , PIC18F4423T <sup>(2)</sup> , PIC18F4523T <sup>(2)</sup> ; VDD range 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flat pack) ML = QFN SO = SOIC SP = Skinny Plastic DIP P = PDIP		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

- a) PIC18F4523-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.
- b) PIC18F4523-I/PT = Industrial temp., TQFP package, Extended VDD limits.
- c) PIC18F4523-E/P = Extended temp., PDIP package, normal VDD limits.

**Note 1:** F = Standard Voltage Range  
LF = Wide Voltage Range  
**2:** T = In tape and reel PLCC, and TQFP packages only.