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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
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Pin Diagrams



1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2423 PIC18LF2423
- PIC18F2523 PIC18LF2523
- PIC18F4423 PIC18LF4423
- PIC18F4523 PIC18LF4523
- Note: This data sheet documents only the devices' features and specifications that are in addition to, or different from, the features and specifications of the PIC18F2420/2520/4420/4520 devices. For information on the features and specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. On top of these features, the PIC18F2423/2523/4423/4523 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2423/2523/4423/4523 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- Alternate Run Modes: By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- Multiple Idle Modes: The controller also can run with its CPU core disabled and the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- Low Consumption in Key Modules: The power requirements for both Timer1 and the Watchdog Timer are minimized. See Section 4.0 "Electrical Characteristics" for values.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2423/2523/4423/4523 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- Two External RC Oscillator modes with the same pin options as the External Clock modes.
- An internal oscillator block that offers eight clock frequencies: an 8 MHz clock and an INTRC source (approximately 31 kHz), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and Internal Oscillator modes, allowing clock speeds of up to 40 MHz from the HS clock source. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz, all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- Fail-Safe Clock Monitor: Constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** Allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.



FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM

Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

2: RE3 is only available when MCLR functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see Section 2.0 "Oscillator Configurations" of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

TABLE 1-2:	PIC18F2423/2523 PINOUT I/O DESCRIPTIONS
------------	---

	Pin N	umber	Din	Duffer						
Pin Name	PDIP, SOIC	QFN	Туре	Туре	Description					
MCLR/VPP/RE3	1	26		0.7	Master Clear (input) or programming voltage (input).					
MCLR			I	SI	Master Clear (Reset) input. This pin is an active-low Reset to the device.					
VPP			Р		Programming voltage input.					
RE3			Ι	ST	Digital input.					
OSC1/CLKI/RA7	9	6			Oscillator crystal or external clock input.					
OSC1			I	ST	Oscillator crystal input or external clock source input.					
				01400	ST buffer when configured in RC mode; CMOS otherwise.					
CLKI				CIMOS	S External clock source input. Always associated with pin function_OSC1 (See related OSC1/CLKL_OSC2/CLKO)					
					pins.)					
RA7			I/O	TTL	General purpose I/O pin.					
OSC2/CLKO/RA6	10	7			Oscillator crystal or clock output.					
OSC2			0	—	Oscillator crystal output. Connects to crystal or					
			~		resonator in Crystal Oscillator mode.					
CLKO			0		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the					
RA6			1/0	тті	General purpose I/O pin.					
	omnatih	lo input			CMOS = CMOS compatible input or output					
ST = Schm	itt Trigg	ar input	with C							
	t nyy	si input	with C		$D = D_{OWOP}$					
2° = 2°										

 $I^2C = I^2C^{TM}/SMBus$

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

	Pin Number		Din	Buffor					
Pin Name	PDIP, SOIC	QFN	Туре	Туре	Description				
					PORTC is a bidirectional I/O port.				
RC0/T1OSO/T13CKI RC0 T1OSO T13CKI	11	8	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.				
RC1/T1OSI/CCP2	12	9							
RC1 T1OSI CCP2 ⁽²⁾			1/O 1 1/O	ST Analog ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.				
RC2/CCP1 RC2	13	10	I/O	ST					
CCP1			I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.				
RC3/SCK/SCL RC3 SCK SCL	14	11	I/O I/O I/O	ST ST I ² C	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode.				
RC4/SDI/SDA RC4	15	12	I/O	ST	Digital I/O.				
SDI SDA			I I/O	ST I ² C	SPI data in. I ² C data I/O.				
RC5/SDO RC5	16	13	I/O	ST	Digital I/O.				
SDO			0	—	SPI data out.				
RC6/TX/CK RC6 TX CK	17	14	I/O O I/O	ST — ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see related RX/DT).				
RC7/RX/DT RC7	18	15	I/O	ST	Digital I/O.				
RX DT			I I/O	ST ST	EUSART asynchronous receive. EUSART synchronous data (see related TX/CK).				
RE3	_	—	—	—	See MCLR/VPP/RE3 pin.				
Vss	8, 19	5, 16	Р	—	Ground reference for logic and I/O pins.				
VDD	20	17	Ρ	—	Positive supply for logic and I/O pins.				
Legend: TTL = TTL co ST = Schmi	ompatib tt Trigge	le input er input	: with C	MOS le	vels CMOS = CMOS compatible input or output I = Input				

Р

= Power

TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS ((CONTINUED)
--	-------------

O = Output I^2C = $I^2C^{TM}/SMBus$ Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

Pin Namo	Pi	n Numt	ber	Pin	Buffer	Description		
	PDIP	QFN	TQFP	Туре	Туре	Description		
						PORTA is a bidirectional I/O port.		
RA0/AN0 RA0 AN0	2	19	19	I/O I	TTL Analog	Digital I/O. Analog Input 0.		
RA1/AN1 RA1 AN1	3	20	20	I/O I	TTL Analog	Digital I/O. Analog Input 1.		
RA2/AN2/VREF-/CVREF RA2 AN2 VREF- CVREF	4	21	21	I/O I I O	TTL Analog Analog Analog	Digital I/O. Analog Input 2. A/D reference voltage (low) input. Comparator reference voltage output.		
RA3/AN3/VREF+ RA3 AN3 VREF+	5	22	22	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 3. A/D reference voltage (high) input.		
RA4/T0CKI/C1OUT RA4 T0CKI C1OUT	6	23	23	I/O I O	ST ST	Digital I/O. Timer0 external clock input. Comparator 1 output.		
RA5/AN4/SS/HLVDIN/ C2OUT RA5 AN4	7	24	24	I/O I	TTL Analog	Digital I/O. Analog Input 4.		
SS HLVDIN C2OUT			ITTLSPI slave select input.IAnalogHigh/Low-Voltage DetO—Comparator 2 output.		TTL Analog —	SPI slave select input. High/Low-Voltage Detect input. Comparator 2 output.		
RA6						See the OSC2/CLKO/RA6 pin.		
Legend: TTI - TTI	compat	ihle inn	l ut			See the USC I/ULNI/KA7 pin.		
Legend: TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels O = Output $I^2C = I^2C^{TM}(SMBus)$ CMOS = CMOS compatible input or output I = Input P = Power								

TABLE 1-3:	PIC18F4423/4523 PINOUT I/O DESCRIPTIONS ((CONTINUED)	1

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

Din Nama	Pi	n Numb	ber	Pin	Buffer	Description
	PDIP	QFN	TQFP	Туре	Туре	Description
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/FLT0/AN12 RB0 INT0 FLT0 AN12	33	9	8	I/O I I	TTL ST ST Analog	Digital I/O. External Interrupt 0. PWM Fault input for Enhanced CCP1. Analog Input 12.
RB1/INT1/AN10 RB1 INT1 AN10	34	10	9	I/O I I	TTL ST Analog	Digital I/O. External Interrupt 1. Analog Input 10.
RB2/INT2/AN8 RB2 INT2 AN8	35	11	10	I/O I I	TTL ST Analog	Digital I/O. External Interrupt 2. Analog Input 8.
RB3/AN9/CCP2 RB3 AN9 CCP2 ⁽¹⁾	36	12	11	I/O I I/O	TTL Analog ST	Digital I/O. Analog Input 9. Capture 2 input/Compare 2 output/PWM2 output.
RB4/KBI0/AN11 RB4 KBI0 AN11	37	14	14	I/O I I	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. Analog Input 11.
RB5/KBI1/PGM RB5 KBI1 PGM	38	15	15	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC RB6 KBI2 PGC	39	16	16	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	40	17	17	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.
Legend:TTL = TTL compatible inputCMOS = CMOS compatible input or outputST = Schmitt Trigger input with CMOS levelsI= InputO = OutputP= Power I^2C = $I^2C^{TM}/SMBus$ P= Power						

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

NOTES:

2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the PIC18F2423/2523 devices and 13 for the PIC18F4423/4523 devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

REGISTER 2-1:

Of the ADCONx registers:

- ADCON0 (shown in Register 2-1) Controls the module's operation
- ADCON1 (Register 2-2) Configures the functions of the port pins
- ADCON2 (Register 2-3) Configures the A/D clock source, programmed acquisition time and justification

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

ADCON0: A/D CONTROL REGISTER 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 7-6 Unimplemented: Read as '0'

bit 5-2	CHS<3:0>: Analog Channel Select bits
	0000 = Channel 0 (AN0)
	0001 = Channel 1 (AN1)
	0010 = Channel 2 (AN2)
	0011 = Channel 3 (AN3)
	0100 = Channel 4 (AN4)
	0101 = Channel 5 (AN5) ^(1,2)
	0110 = Channel 6 (AN6) ^(1,2)
	0111 = Channel 7 (AN7) ^(1,2)
	1000 = Channel 8 (AN8)
	1001 = Channel 9 (AN9)
	1010 = Channel 10 (AN10)
	1011 = Channel 11 (AN11)
	1100 = Channel 12 (AN12
	1101 = Unimplemented ⁽²⁾
	1110 = Unimplemented ⁽²⁾
	1111 = Unimplemented ⁽²⁾
bit 1	GO/DONE: A/D Conversion Status bit
	When ADON = 1:
	1 = A/D conversion in progress
	0 = A/D Idle
bit 0	ADON: A/D On bit
	1 = A/D Converter module is enabled
	0 = A/D Converter module is disabled
Note 1:	These channels are not implemented on PIC18F2423/2523 devices.
•	

2: Performing a conversion on unimplemented channels will return a floating input measurement.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss), or the voltage level on the RA3/AN3/ VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is <u>loaded</u> into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

The block diagram of the A/D module is shown in Figure 2-1.



FIGURE 2-1: A/D BLOCK DIAGRAM

Device ID Registers

The Device ID registers are read-only registers. They identify the device type and revision for device pro-

grammers and can be read by firmware using table

3.0 SPECIAL FEATURES OF THE CPU

Note: For additional details on the Configuration bits, refer to Section 23.1 "Configuration Bits" in the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631). Device ID information presented in this section is for the PIC18F2423/2523/4423/4523 devices only.

TABLE 3-1: DEVICE IDs

Default/ File Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Unprogrammed Value ×××× ×××××××××(2) DEVID1⁽¹⁾ 3FFFFEh DEV3 DEV2 DEV1 DEV0 REV3 REV2 REV1 REV0 XXXX XXXX(2) 3FFFFFh DEVID2⁽¹⁾ DEV11 DEV10 DEV8 DEV7 DEV6 DEV5 DEV4 DEV9

3.1

reads.

x = unknown, u = unchanged, — = unimplemented. Shaded cells are unimplemented, read as '0'. Legend:

Note 1: DEVID registers are read-only and cannot be programmed by the user.

2: See Register 3-1 and Register 3-2 for DEVID1 and DEVID2 values.

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0
bit 7	•		•				bit 0

Legend:				
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'		
-n = Value when device is unp	programmed	u = Unchanged from programmed state		

bit 7-4	DEV<3:0>: Device ID bits
	1101 = PIC18F4423
	1001 = PIC18F4523
	0101 = PIC18F2423
	0001 = PIC18F2523
bit 3-0	REV<3:0>: Revision ID bits
	These bits are used to indicate the device revision

PIC18F2423/2523/4423/4523

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV11 ⁽¹⁾	DEV10 ⁽¹⁾	DEV9 ⁽¹⁾	DEV8 ⁽¹⁾	DEV7 ⁽¹⁾	DEV6 ⁽¹⁾	DEV5 ⁽¹⁾	DEV4 ⁽¹⁾
bit 7							bit 0
Legend:							
R = Read-only bit P = Programmable bit		U = Unimplemented bit, read as '0'					
-n = Value when device is unprogrammed			u = Unchanged from programmed state				

bit 7-0 **DEV<11:4>:** Device ID bits⁽¹⁾ These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number. 0001 0001 = PIC18F2423/2523 devices 0001 0000 = PIC18F4423/4523 devices

Note 1: These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.



PIC18F2423/2523/4423/4523



Param No.	Symbol	Characte	Min	Мах	Units	Conditions	
130	Tad	A/D Clock Period	PIC18FXXXX	0.8	12.5 ⁽¹⁾	μS	Tosc based, VREF \geq 3.0V
			PIC18 LF XXXX	1.4	25.0 ⁽¹⁾	μS	VDD = 3.0V; Tosc based, VREF full range
			PIC18FXXXX	_	1	μS	A/D RC mode
			PIC18LFXXXX	_	3	μS	VDD = 3.0V; A/D RC mode
131	TCNV	Conversion Time (not including acquisition	on time) ⁽²⁾	13	14	Tad	
132	TACQ	Acquisition Time ⁽³⁾		1.4	—	μS	
135	Tswc	Switching Time from C	_	(Note 4)			
137	TDIS	Discharge Time	0.2	—	μS		

TABLE 4-2: A/D CONVERSION REQUIREMENT

Note 1: The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

2: ADRES registers may be read on the following TCY cycle.

3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to Vss or Vss to VDD). The source impedance (Rs) on the input channels is 50Ω.

4: On the following cycle of the device clock.

NOTES:

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

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