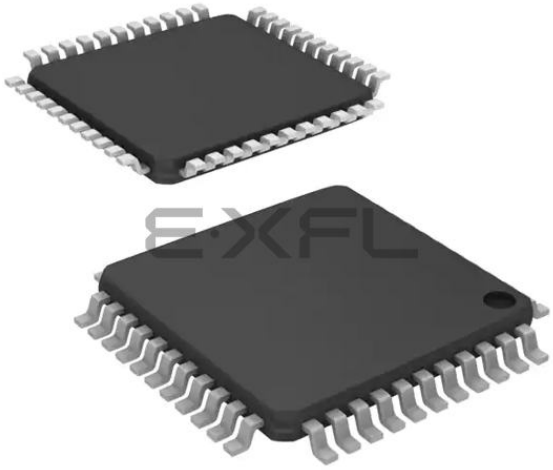

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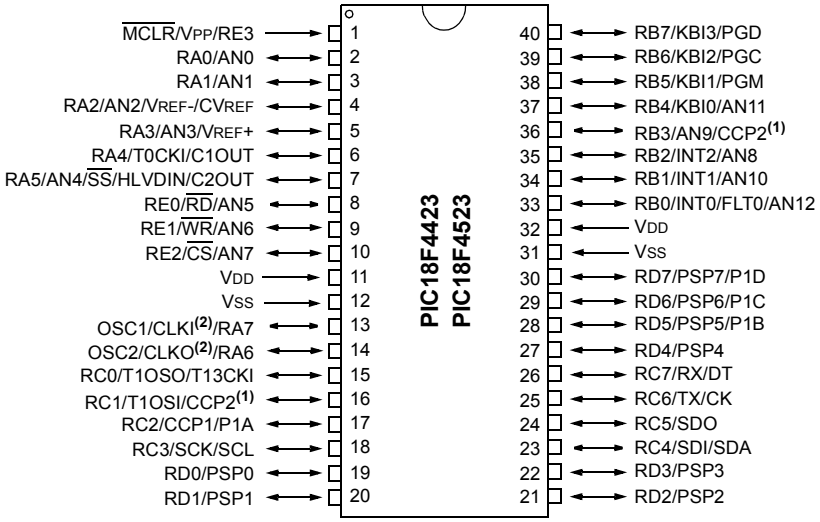
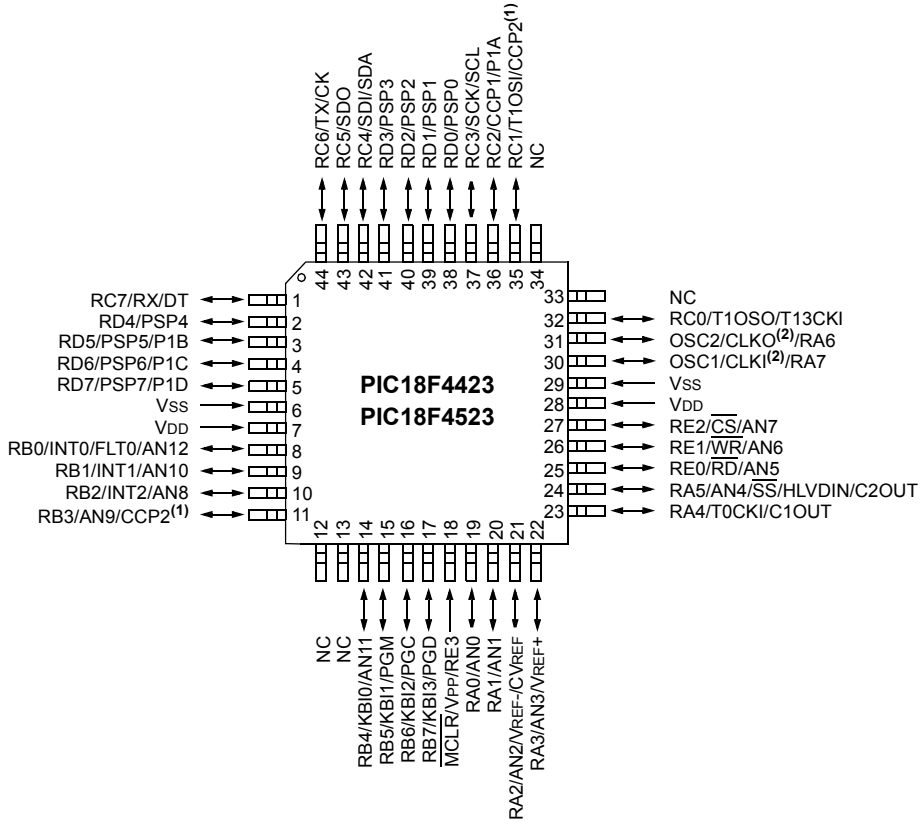
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4523-e-pt

Pin Diagrams (Continued)

40-Pin PDIP



44-Pin TQFP

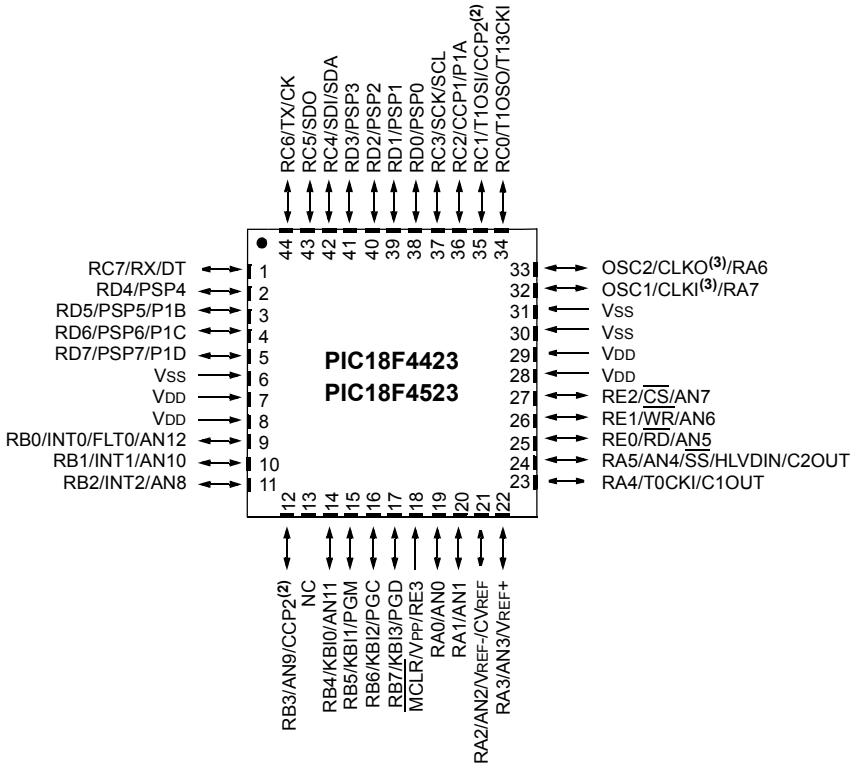


Note 1: RB3 is the alternate pin for CCP2 multiplexing.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

Pin Diagrams (Continued)

44-Pin QFN(1)



Note 1: It is recommended to connect the bottom pad of QFN package parts to VSS.

2: RB3 is the alternate pin for CCP2 multiplexing.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

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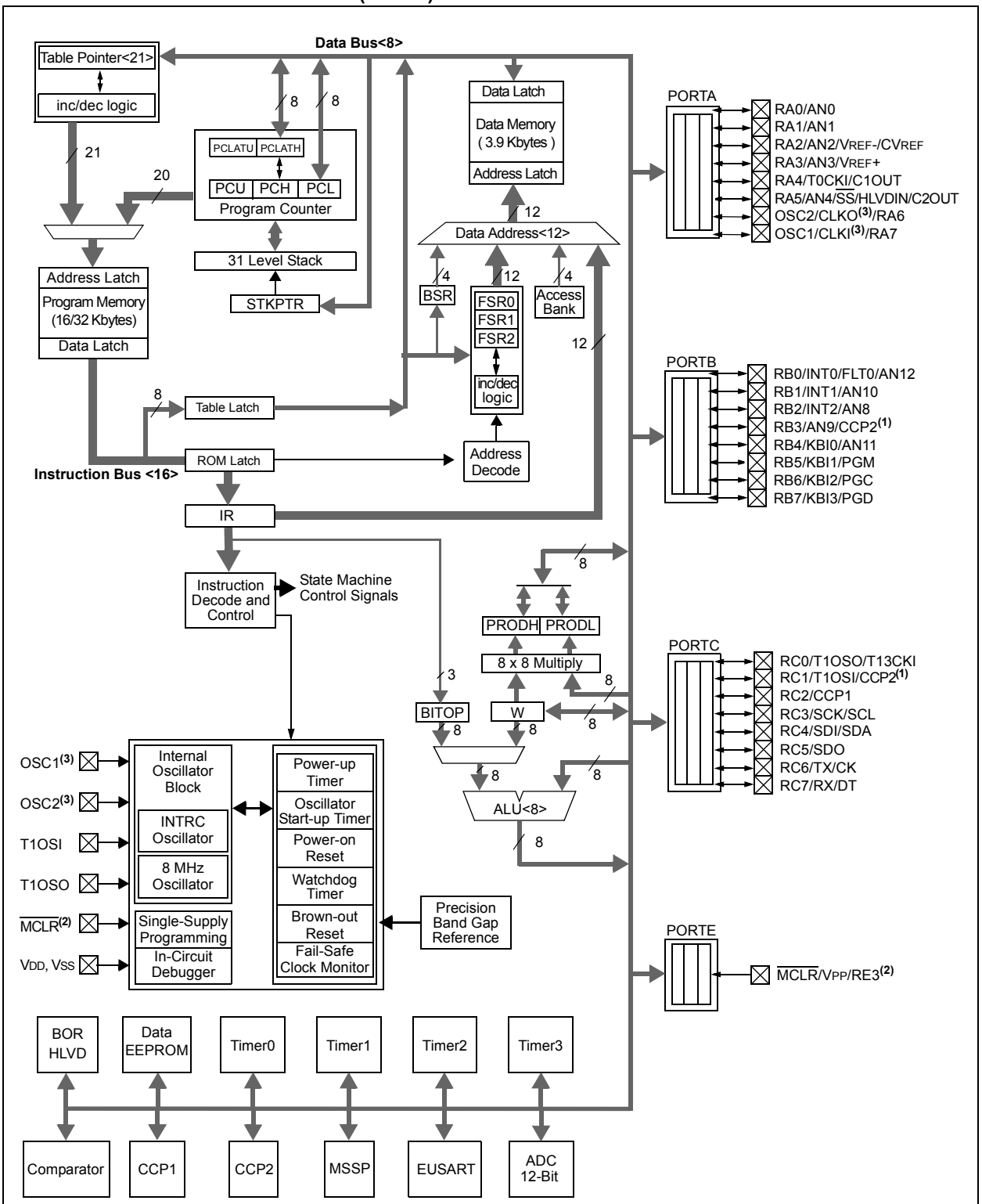
FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM



Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

2: RE3 is only available when MCLR functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
MCLR/VPP/RE3	1	26			Master Clear (input) or programming voltage (input).
MCLR			I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP			P		Programming voltage input.
RE3			I	ST	Digital input.
OSC1/CLKI/RA7	9	6			Oscillator crystal or external clock input.
OSC1			I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI			I	CMOS	External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7			I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	10	7			Oscillator crystal or clock output.
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6			I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; I^2C = I^2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

PCFG<3:0>	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are only available on PIC18F4423/4523 devices.

REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (V_{DD} and V_{SS}), or the voltage level on the RA3/AN3/V_{REF}+ and RA2/AN2/V_{REF}-/CV_{REF} pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

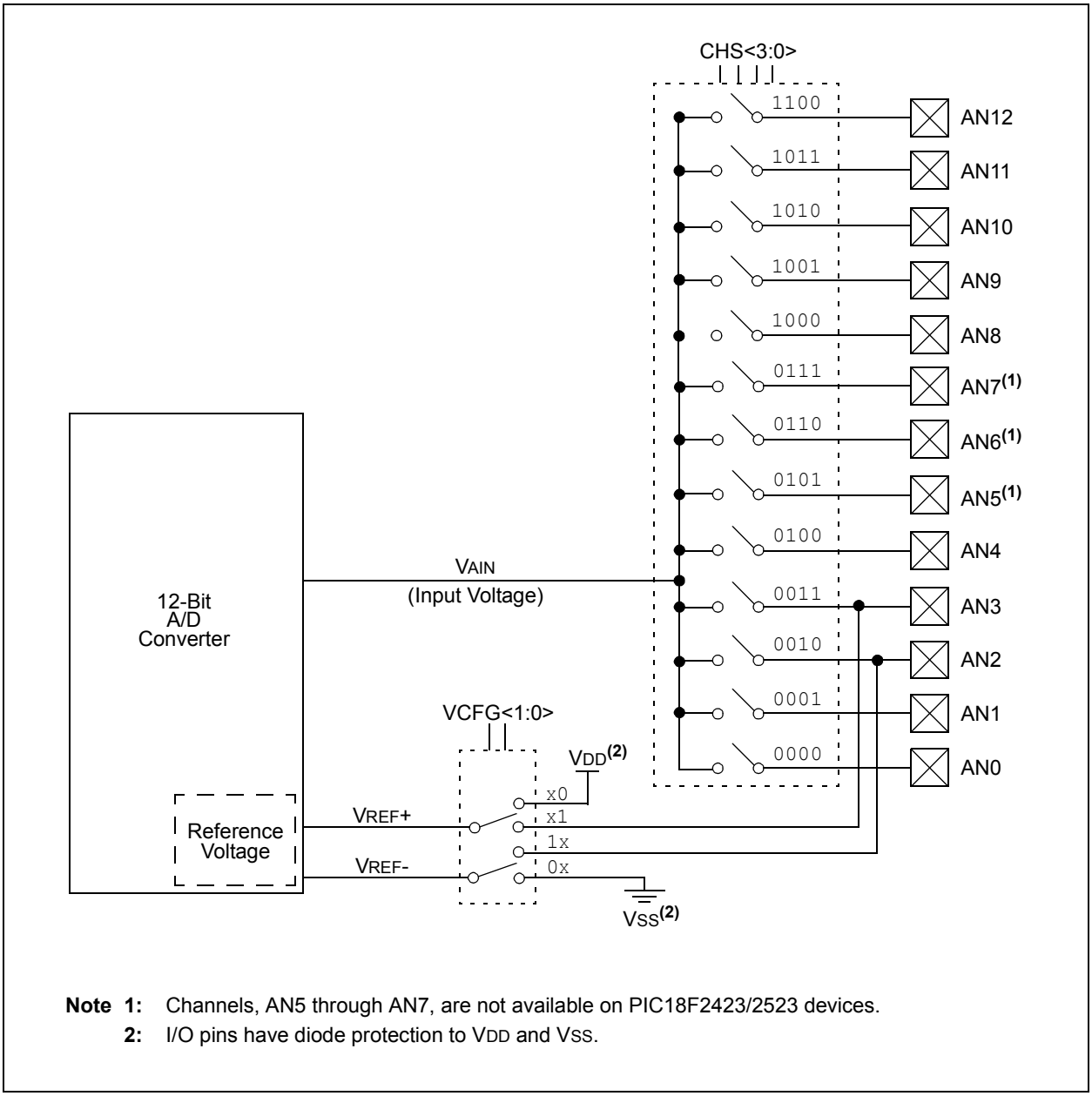
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM



Note 1: Channels, AN5 through AN7, are not available on PIC18F2423/2523 devices.

2: I/O pins have diode protection to V_{DD} and V_{SS}.

2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3.

The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.**

After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note:	When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the application system assumptions shown in Table 2-1:

TABLE 2-1: TACQ ASSUMPTIONS

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system maximum)

EQUATION 2-1: ACQUISITION TIME

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \bullet (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ln(1/4096)$$

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$
$$T_{AMP} = 0.2\ \mu s$$
$$T_{COFF} = (\text{Temp} - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, T_{COFF} = 0 ms.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ln(1/4095)\ \mu s$$
$$-(25\ pF)(1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega)\ln(0.0004883)\ \mu s$$
$$1.56\ \mu s$$
$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$

2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition time is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-2: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 μs
Operation	**ADCS<2:0>**	**Maximum FOSC**
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	40.00 MHz
RC(2)	x11	1.00 MHz(1)

Note 1: The RC source has a typical TAD time of 2.5 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS<2:0> bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT<2:0> bits do not need to be adjusted as the ADCS<2:0> bits adjust the TAD time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits, ACQT<2:0>, are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

Note 1:	When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.
2:	Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.
3:	The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG<3:0> bits in ADCON1 are reset.

2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

TABLE 2-3: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	**(Note 4)**
PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	**(Note 4)**
PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	**(Note 4)**
IPR1	PSPIP(1)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	**(Note 4)**
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	**(Note 4)**
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	**(Note 4)**
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	**(Note 4)**
ADRESH	A/D Result Register High Byte								**(Note 4)**
ADRESL	A/D Result Register Low Byte								**(Note 4)**
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	**(Note 4)**
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	**(Note 4)**
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	**(Note 4)**
PORTA	RA7(2)	RA6(2)	RA5	RA4	RA3	RA2	RA1	RA0	**(Note 4)**
TRISA	TRISA7(2)	TRISA6(2)	PORTA Data Direction Control Register						**(Note 4)**
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	**(Note 4)**
TRISB	PORTB Data Direction Control Register								**(Note 4)**
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								**(Note 4)**
PORTE(1)	—	—	—	—	RE3(3)	RE2	RE1	RE0	**(Note 4)**
TRISE(1)	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	**(Note 4)**
LATE(1)	—	—	—	—	—	PORTE Data Latch Register			**(Note 4)**

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These registers and/or bits are not implemented on PIC18F2423/2523 devices and are read as '0'.

2: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

3: RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

4: For these Reset values, see **Section 4.0 "Reset"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

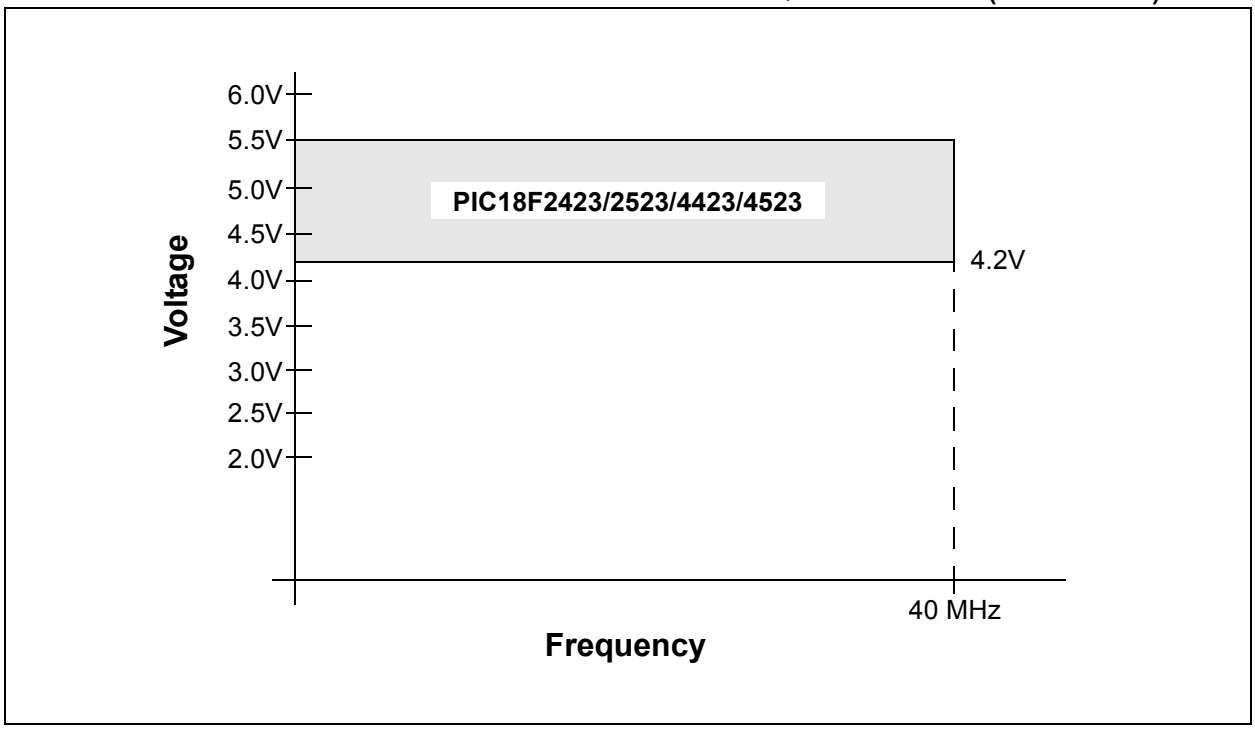


FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)

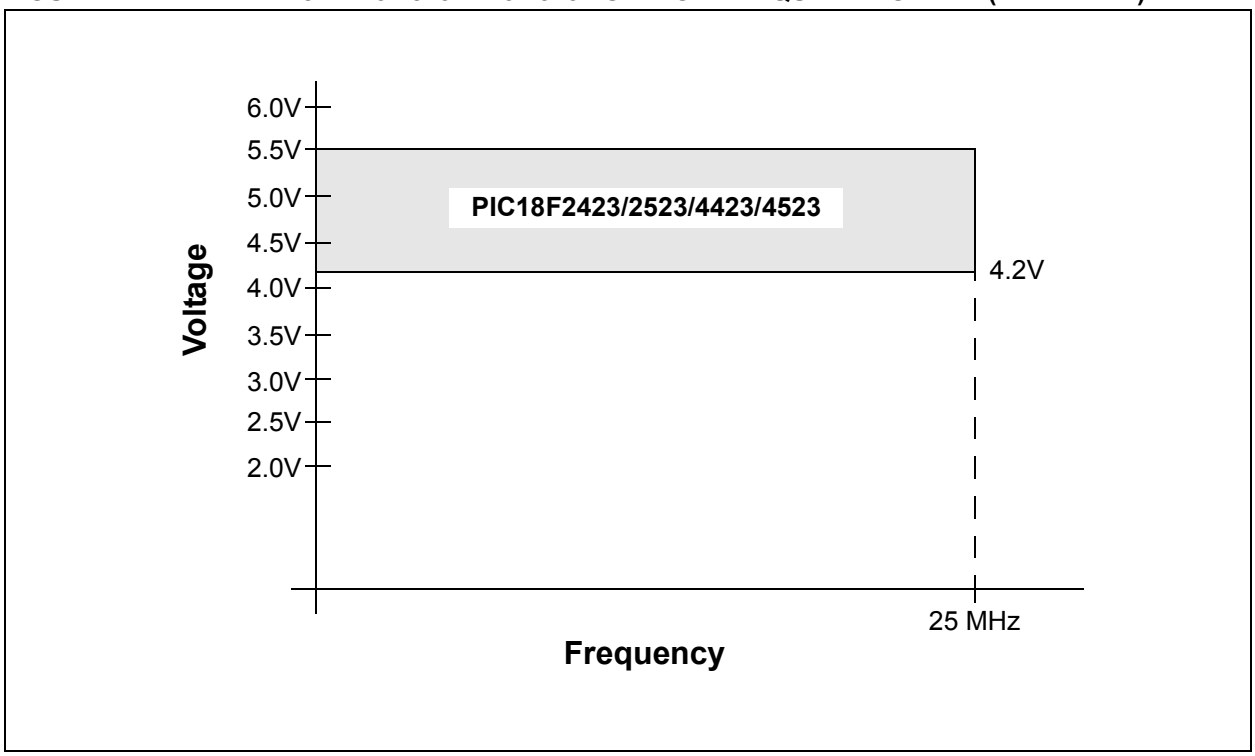


TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL) PIC18LF2423/2523/4423/4523 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		ΔVREF ≥ 3.0V
A03	EIL	Integral Linearity Error	—	<±1	±2.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.0	LSB	VDD = 5.0V	
A04	EDL	Differential Linearity Error	—	<±1	+1.5/-1.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	+1.5/-1.0	LSB	VDD = 5.0V	
A06	EOFF	Offset Error	—	<±1	±5	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±3	LSB	VDD = 5.0V	
A07	EGN	Gain Error	—	<±1	±1.25	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.00	LSB	VDD = 5.0V	
A10	—	Monotonicity	Guaranteed(1)			—		VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V		For 12-bit resolution.
A21	VREFH	Reference Voltage High	VSS + 3.0V	—	VDD + 0.3V	V		For 12-bit resolution.
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	VDD – 3.0V	V		For 12-bit resolution.
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V		
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ		
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA		During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

NOTES:

5.0 PACKAGING INFORMATION

For packaging information, see **Section 28.0 "Packaging Information"** in the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

NOTES:

APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442"*. The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration*". This Application Note is available as Literature Number DS00726.

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