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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f4523-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic18f4523-i-pt</a>

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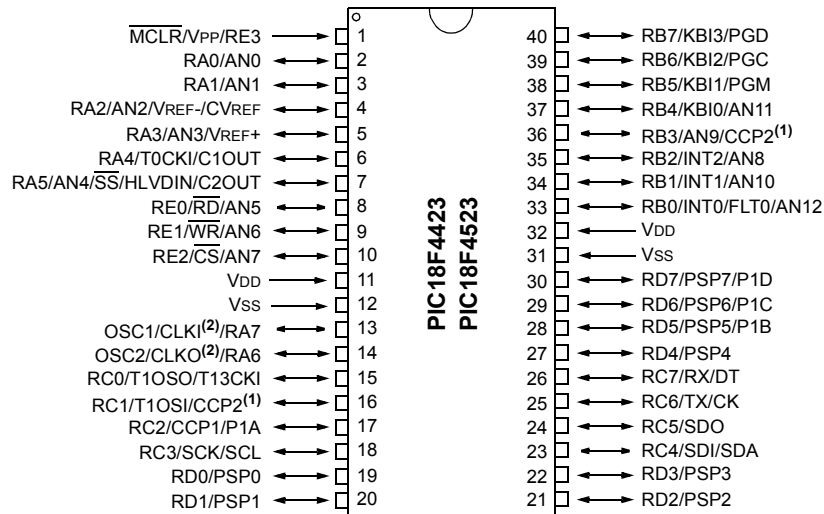
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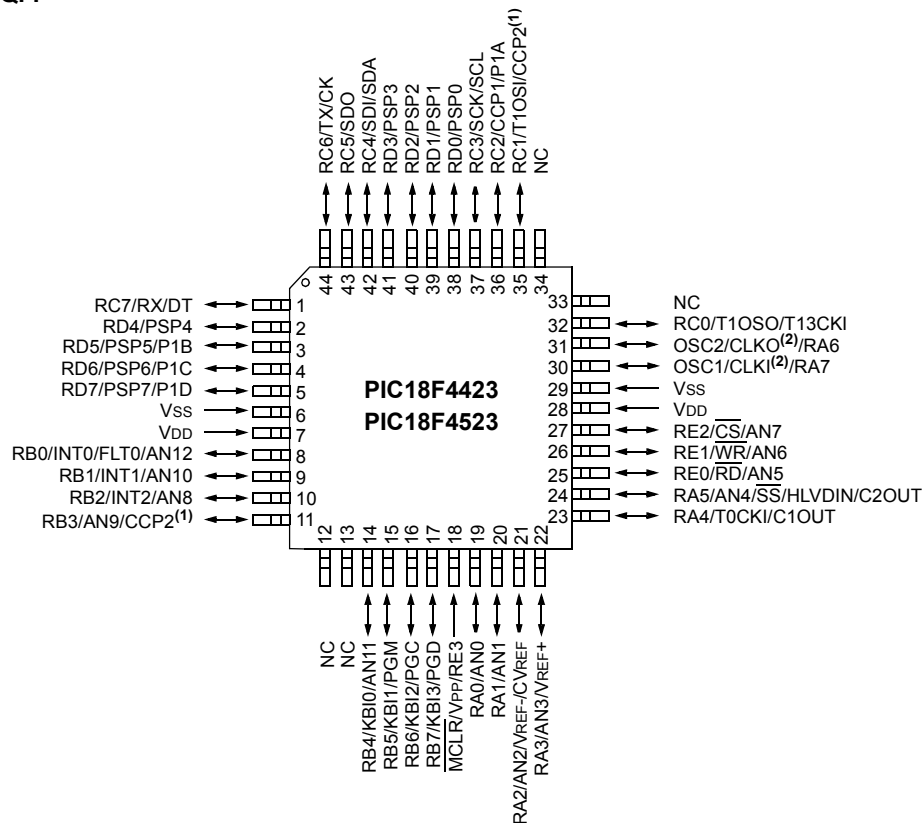
# PIC18F2423/2523/4423/4523

## Pin Diagrams (Continued)

### 40-Pin PDIP



### 44-Pin TQFP

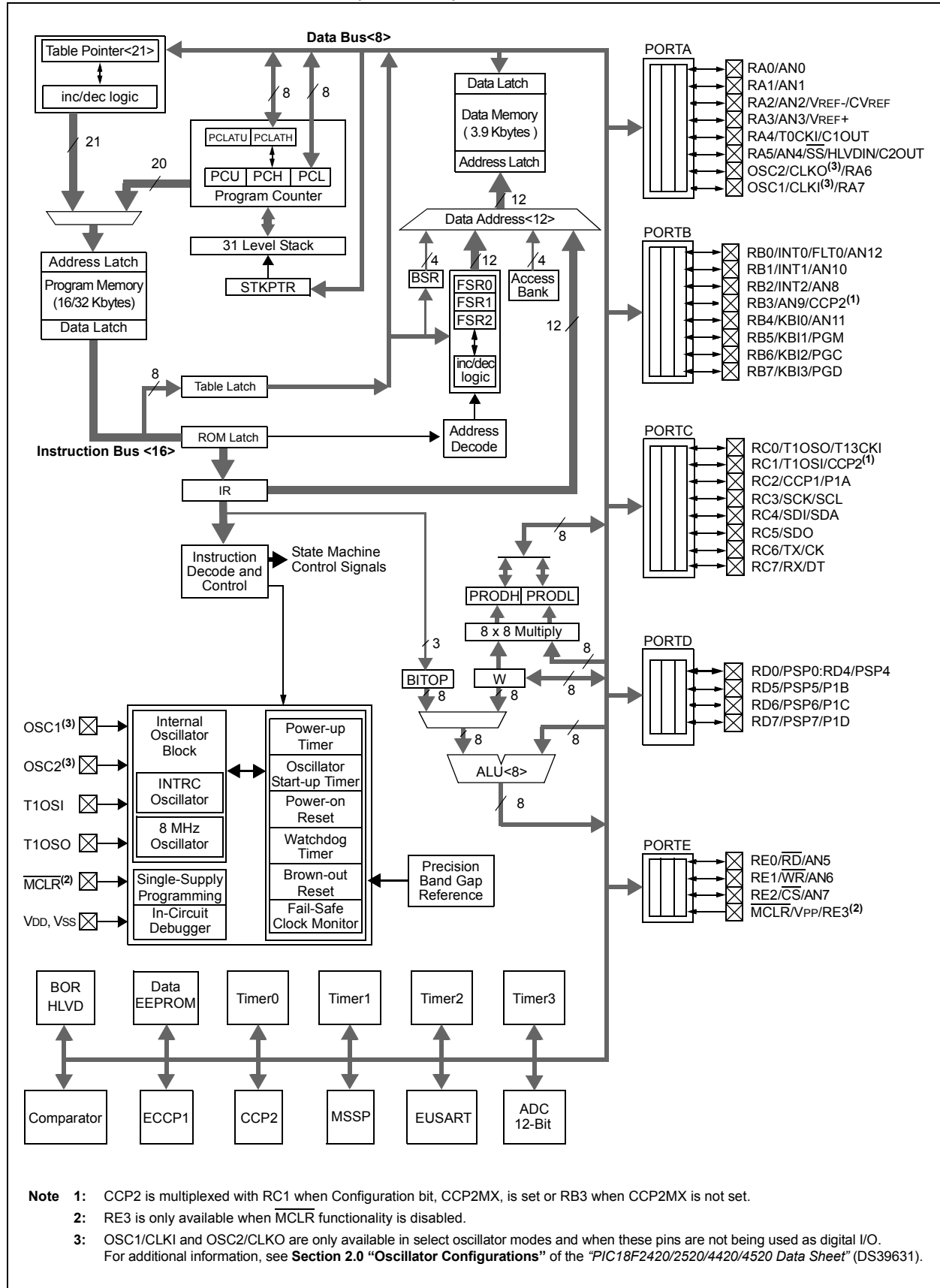


**Note 1:** RB3 is the alternate pin for CCP2 multiplexing.

**Note 2:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

# PIC18F2423/2523/4423/4523

**FIGURE 1-2: PIC18F4423/4523 (40/44-PIN) BLOCK DIAGRAM**



# PIC18F2423/2523/4423/4523

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RC0/T1OSO/T13CKI RC0 T1OSO T13CKI	15	34	32	I/O O I	ST — ST	PORTC is a bidirectional I/O port.  Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 <sup>(2)</sup>	16	35	35	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/P1A RC2 CCP1 P1A	17	36	36	I/O I/O O	ST ST —	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output. Enhanced CCP1 output.
RC3/SCK/SCL RC3 SCK  SCL	18	37	37	I/O I/O I/O	ST ST I <sup>2</sup> C	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC4/SDI/SDA RC4 SDI SDA	23	42	42	I/O I I/O	ST ST I <sup>2</sup> C	Digital I/O. SPI data in. I <sup>2</sup> C data I/O.
RC5/SDO RC5 SDO	24	43	43	I/O O	ST —	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	44	44	I/O O I/O	ST — ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see related RX/DT).
RC7/RX/DT RC7 RX DT	26	1	1	I/O I I/O	ST ST ST	Digital I/O. EUSART asynchronous receive. EUSART synchronous data (see related TX/CK).

**Legend:** TTL = TTL compatible input  
ST = Schmitt Trigger input with CMOS levels  
O = Output  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus  
CMOS = CMOS compatible input or output  
I = Input  
P = Power

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

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NOTES:

# PIC18F2423/2523/4423/4523

## REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0 <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (VREF- source)

1 = VREF- (AN2)

0 = VSS

bit 4 **VCFG0:** Voltage Reference Configuration bit (VREF+ source)

1 = VREF+ (AN3)

0 = VDD

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

PCFG<3:0>	AN12	AN11	AN10	AN9	AN8	AN7 <sup>(2)</sup>	AN6 <sup>(2)</sup>	AN5 <sup>(2)</sup>	AN4	AN3	AN2	AN1	AN0
0000 <sup>(1)</sup>	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111 <sup>(1)</sup>	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O

**Note 1:** The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

**2:** AN5 through AN7 are only available on PIC18F4423/4523 devices.

# PIC18F2423/2523/4423/4523

## REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD<sup>(1)</sup>

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the **SLEEP** instruction to be executed before starting a conversion.



# PIC18F2423/2523/4423/4523

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

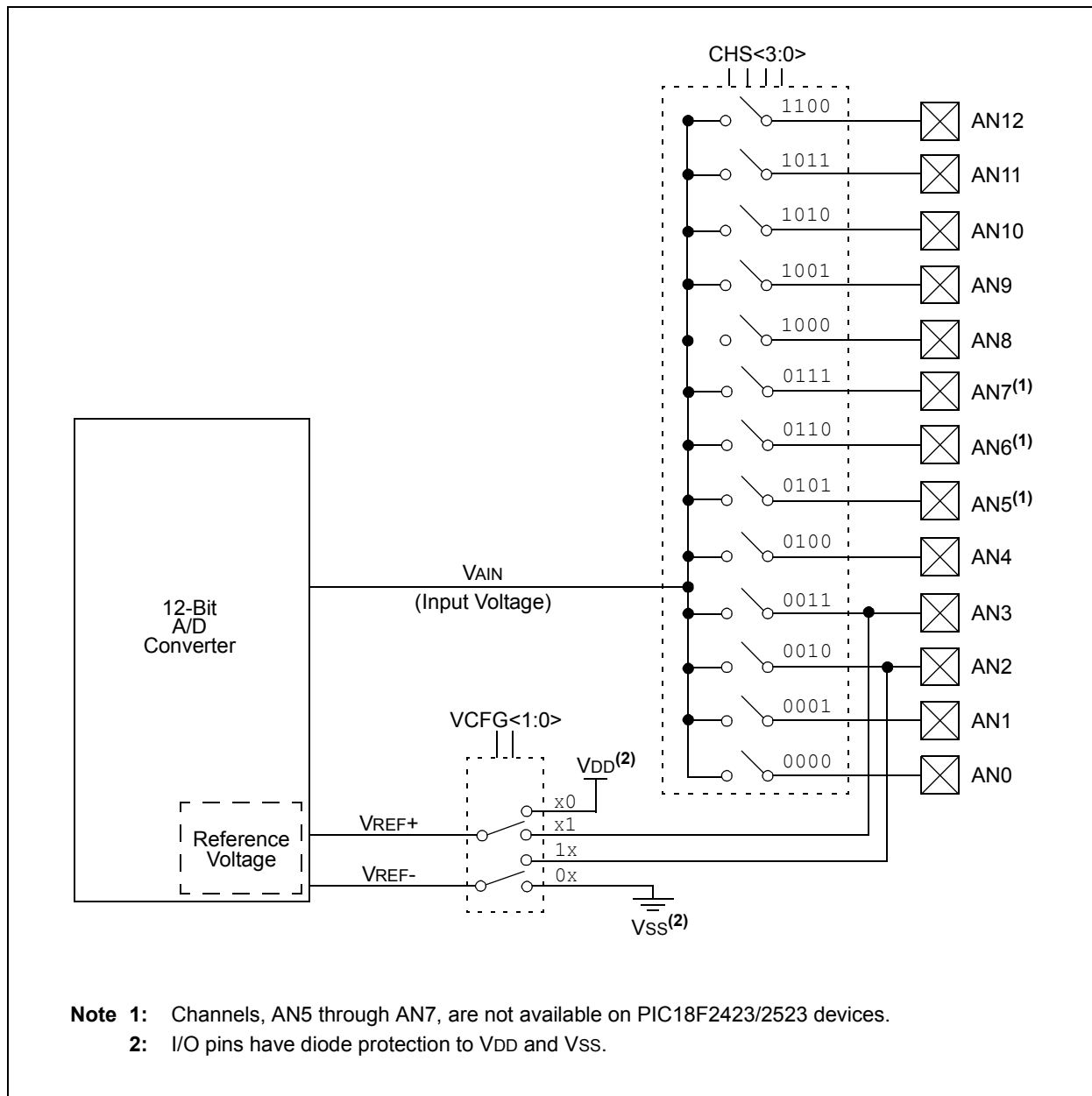
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**



# PIC18F2423/2523/4423/4523

## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3.

The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.**

After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

**Note:** When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the application system assumptions shown in Table 2-1:

**TABLE 2-1: TAcQ ASSUMPTIONS**

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system maximum)

### EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= \text{TAMP} + \text{TC} + \text{TCOFF} \end{aligned}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} \text{VHOLD} &= (\text{VREF} - (\text{VREF}/4096)) \cdot (1 - e^{-(\text{TC}/\text{CHOLD}(\text{RIC} + \text{RSS} + \text{RS})))} \\ \text{or} \\ \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \end{aligned}$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{TAMP} + \text{TC} + \text{TCOFF} \\ \text{TAMP} &= 0.2 \mu\text{s} \\ \text{TCOFF} &= (\text{Temp} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad 1.2 \mu\text{s} \end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 ms.

$$\begin{aligned} \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \mu\text{s} \\ &\quad -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0004883) \mu\text{s} \\ &\quad 1.56 \mu\text{s} \\ \text{TACQ} &= 0.2 \mu\text{s} + 1.56 \mu\text{s} + 1.2 \mu\text{s} \\ &\quad 2.96 \mu\text{s} \end{aligned}$$

# PIC18F2423/2523/4423/4523

## 2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location).

The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-3: REGISTERS ASSOCIATED WITH A/D OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(Note 4)
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	(Note 4)
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	(Note 4)
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	(Note 4)
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	(Note 4)
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	(Note 4)
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	(Note 4)
ADRESH	A/D Result Register High Byte								(Note 4)
ADRESL	A/D Result Register Low Byte								(Note 4)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	(Note 4)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(Note 4)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(Note 4)
PORTA	RA7 <sup>(2)</sup>	RA6 <sup>(2)</sup>	RA5	RA4	RA3	RA2	RA1	RA0	(Note 4)
TRISA	TRISA7 <sup>(2)</sup>	TRISA6 <sup>(2)</sup>	PORTA Data Direction Control Register						(Note 4)
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	(Note 4)
TRISB	PORTB Data Direction Control Register								(Note 4)
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								(Note 4)
PORTE <sup>(1)</sup>	—	—	—	—	RE3 <sup>(3)</sup>	RE2	RE1	RE0	(Note 4)
TRISE <sup>(1)</sup>	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	(Note 4)
LATE <sup>(1)</sup>	—	—	—	—	—	PORTE Data Latch Register			(Note 4)

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** These registers and/or bits are not implemented on PIC18F2423/2523 devices and are read as '0'.

**2:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**3:** RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

**4:** For these Reset values, see **Section 4.0 "Reset"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

# PIC18F2423/2523/4423/4523

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV11 <sup>(1)</sup>	DEV10 <sup>(1)</sup>	DEV9 <sup>(1)</sup>	DEV8 <sup>(1)</sup>	DEV7 <sup>(1)</sup>	DEV6 <sup>(1)</sup>	DEV5 <sup>(1)</sup>	DEV4 <sup>(1)</sup>
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-0      **DEV<11:4>**: Device ID bits<sup>(1)</sup>

These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number.

0001 0001 = PIC18F2423/2523 devices

0001 0000 = PIC18F4423/4523 devices

**Note 1:** These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.

# PIC18F2423/2523/4423/4523

FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

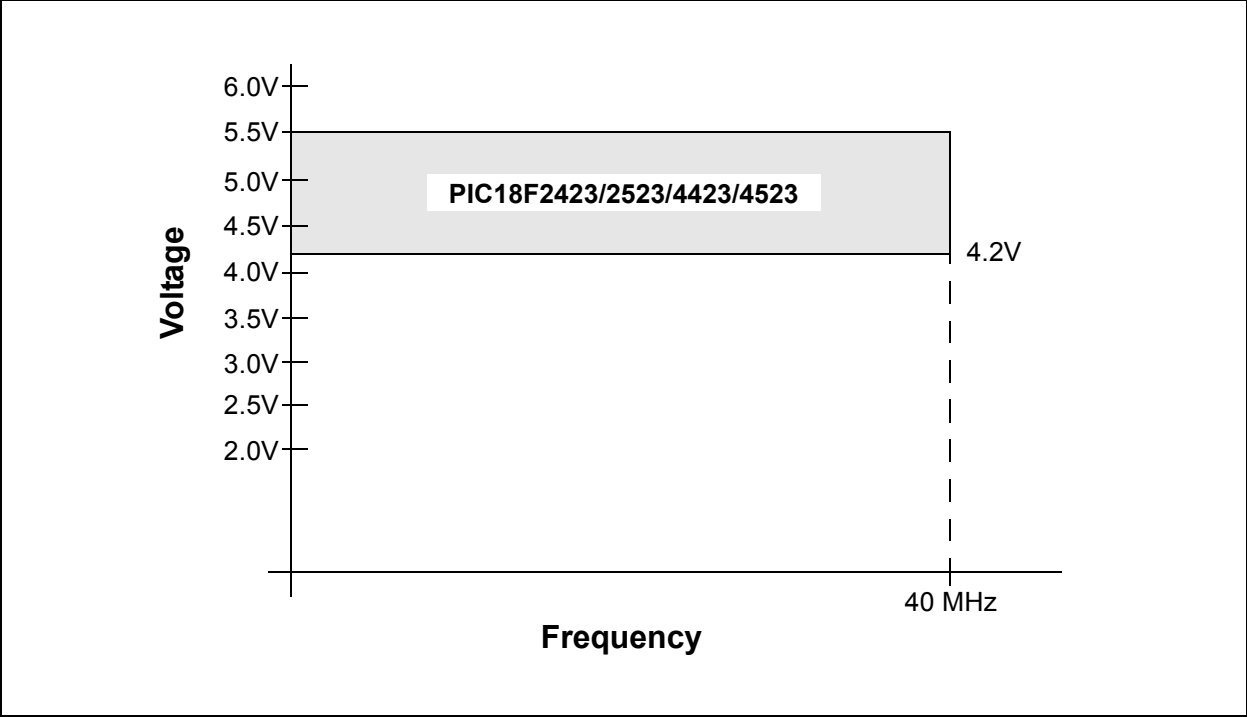
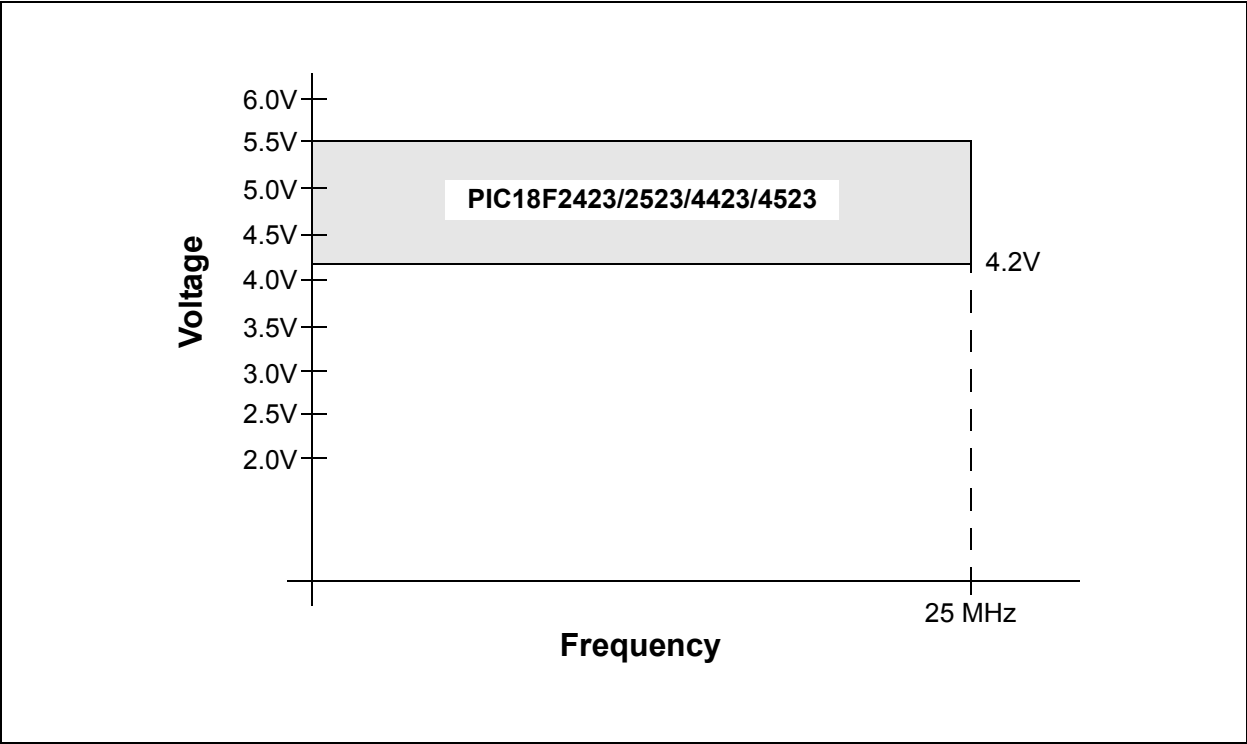
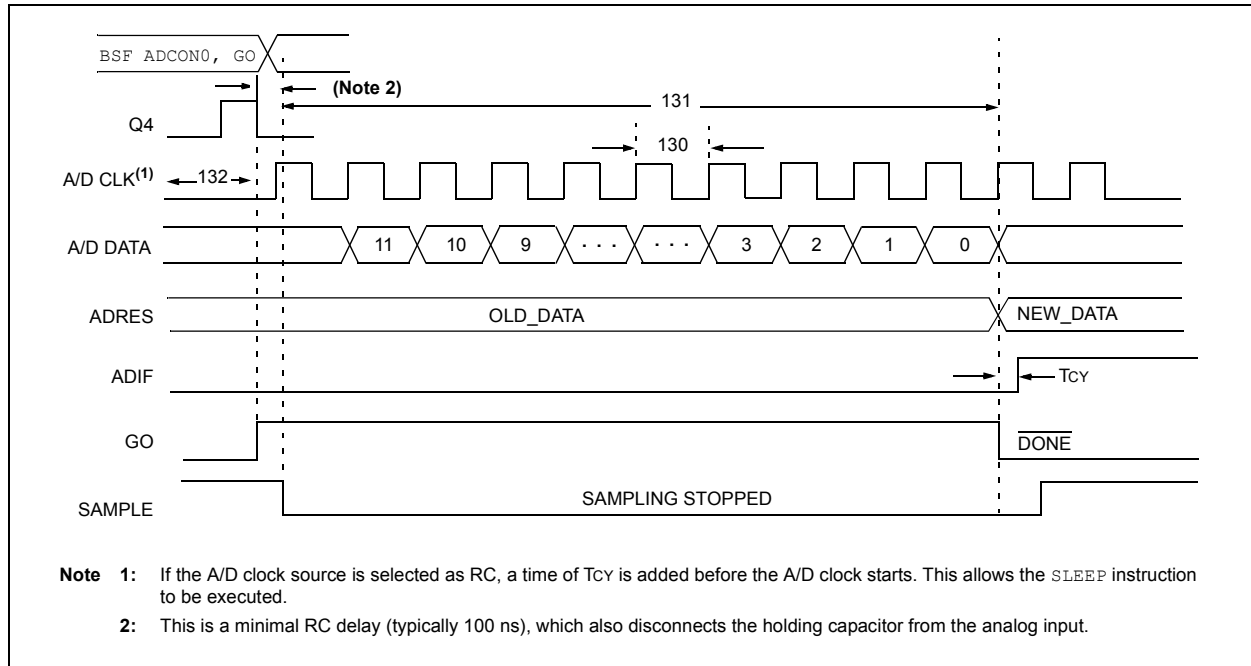


FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



# PIC18F2423/2523/4423/4523

**FIGURE 4-4: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	μs	TOSC based, VREF ≥ 3.0V
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	μs	VDD = 3.0V; TOSC based, VREF full range
			PIC18FXXXX	—	1	μs	A/D RC mode
			PIC18LFXXXX	—	3	μs	VDD = 3.0V; A/D RC mode
131	TCNV	Conversion Time (not including acquisition time) <sup>(2)</sup>		13	14	TAD	
132	TACQ	Acquisition Time <sup>(3)</sup>		1.4	—	μs	
135	TSWC	Switching Time from Convert → Sample		—	(Note 4)		
137	TDIS	Discharge Time		0.2	—	μs	

**Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

**Note 2:** ADRES registers may be read on the following  $T_{CY}$  cycle.

**Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion ( $V_{DD}$  to  $V_{SS}$  or  $V_{SS}$  to  $V_{DD}$ ). The source impedance ( $R_s$ ) on the input channels is  $50\Omega$ .

**Note 4:** On the following cycle of the device clock.

# PIC18F2423/2523/4423/4523

## APPENDIX A: REVISION HISTORY

### Revision A (June 2006)

Original data sheet for PIC18F2423/2523/4423/4523 devices.

### Revision B (January 2007)

This revision includes updates to the packaging diagrams.

### Revision C (September 2009)

Electrical specifications updated. Preliminary condition status removed. Converted document to the "mini data sheet" format.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Program Memory (Bytes)	16384	32768	16384	32768
Program Memory (Instructions)	8192	16384	8192	16384
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**



## **APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES**

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, *"Migrating Designs from PIC16C74A/74B to PIC18C442"*. The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

## **APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES**

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN726, *"PIC17CXXX to PIC18CXXX Migration"*. This Application Note is available as Literature Number DS00726.

# PIC18F2423/2523/4423/4523

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# PIC18F2423/2523/4423/4523

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# PIC18F2423/2523/4423/4523

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device	PIC18F2423 <sup>(1)</sup> , PIC18F2523 <sup>(1)</sup> , PIC18F4423T <sup>(2)</sup> , PIC18F4523T <sup>(2)</sup> ; VDD range 4.2V to 5.5V PIC18F2423 <sup>(1)</sup> , PIC18F2523 <sup>(1)</sup> , PIC18F4423T <sup>(2)</sup> , PIC18F4523T <sup>(2)</sup> ; VDD range 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flat pack) ML = QFN SO = SOIC SP = Skinny Plastic DIP P = PDIP		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

- a) PIC18F4523-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.
- b) PIC18F4523-I/PT = Industrial temp., TQFP package, Extended VDD limits.
- c) PIC18F4523-E/P = Extended temp., PDIP package, normal VDD limits.

  
**Note 1:** F = Standard Voltage Range  
LF = Wide Voltage Range  
**2:** T = In tape and reel PLCC, and TQFP packages only.



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