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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf2423t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



PIC18F2423/2523/4423/4523

28/40/44-Pin, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

Power Management Features:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- · Sleep: CPU off, Peripherals off
- Ultra Low 50 nA Input Leakage
- Run mode Currents Down to 11 μA Typical
- Idle mode Currents Down to 2.5 μA Typical
- Sleep mode Current Down to 100 μA Typical
- Timer1 Oscillator: 900 nA, 32 kHz, 2V
- Watchdog Timer: 1.4 μA, 2V Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL) Available for Crystal and Internal Oscillators
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
- Fast wake from Sleep and Idle, 1 µs typical
- 8 user-selectable frequencies, from 31 kHz to 8 MHz
- Provides a complete range of clock speeds, from 31 kHz to 32 MHz, when used with PLL
 User-tunable to Compensate for Frequency Drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock stops

Peripheral Highlights:

- 12-Bit, Up to 13-Channel Analog-to-Digital Converter module (A/D):
 - Auto-acquisition capability
 - Conversion available during Sleep mode
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Three Programmable External Interrupts
- Four Input Change Interrupts
- Up to Two Capture/Compare/PWM (CCP)
- modules, One with Auto-Shutdown (28-pin devices) • Enhanced Capture/Compare/PWM (ECCP) module
- (40/44-pin devices only):
- One, two or four PWM outputs
- Selectable polarity
- Programmable dead time
- Auto-shutdown and auto-restart

Peripheral Highlights (Continued):

- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all four modes) and I²C[™] Master and Slave modes
- Enhanced USART module:
- Support for RS-485, RS-232 and LIN/J2602RS-232 operation using internal oscillator
- RS-232 operation using internal osc block (no external crystal required)
- Auto-wake-up on Start bit
- Auto-Baud Detect (ABD)

Special Microcontroller Features:

- C Compiler Optimized Architecture: Optional Extended Instruction Set Designed to Optimize Re-Entrant Code
- 100,000 Erase/Write Cycle, Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle, Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT): Programmable Period, from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Operating Voltage Range: 2.0V to 5.5V
- Programmable, 16-Level High/Low-Voltage Detection (HLVD) module: Supports Interrupt on High/Low-Voltage Detection
- Programmable Brown-out Reset (BOR): With Software-Enable Option

Note:	This d	ocumer	nt is	supplem	ented	by	the
	"PIC18	F2420/	2520/	4420/452	20 Data	a Sh	eet"
	(DS396	531). 3	See	Section	1.0 '	'De\	/ice
	Overvi	ew".					

	Program Memory		Data Memory			40 51	CCP/	MS	SSP	RT		-
Device	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)	I/O	12-Bit A/D (ch)	ECCP (PWM)	SPI	Master I ² C™	EUSA	Comp.	8/16-Bit
PIC18F2423	16K	8192	768	256	25	10	2/0	Y	Y	1	2	1/3
PIC18F2523	32K	16384	1536	256	25	10	2/0	Y	Y	1	2	1/3
PIC18F4423	16K	8192	768	256	36	13	1/1	Y	Y	1	2	1/3
PIC18F4523	32K	16384	1536	256	36	13	1/1	Y	Y	1	2	1/3

Pin Diagrams (Continued)



1.2 Other Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, thereby reducing code overhead.
- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- Self-Programmability: These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it is possible to create an application that can update itself in the field.
- Extended Instruction Set: The PIC18F2423/ 2523/4423/4523 family introduces an optional extension to the PIC18 instruction set that adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- Enhanced CCP module: In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown, for disabling PWM outputs on interrupt or other select conditions, and auto-restart, to reactivate outputs once the condition has cleared.
- Enhanced Addressable USART: This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- Extended Watchdog Timer (WDT): This Enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See Section 4.0 "Electrical Characteristics" for time-out periods.

1.3 Details on Individual Family Members

Devices in the PIC18F2423/2523/4423/4523 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
 - PIC18F2423/4423 devices 16 Kbytes
 - PIC18F2523/4523 devices 32 Kbytes
- A/D Channels:
 - PIC18F2423/2523 devices 10
 - PIC18F4423/4523 devices 13
- I/O Ports:
 - PIC18F2423/2523 devices Three bidirectional ports
 - PIC18F4423/4523 devices Five bidirectional ports
- CCP and Enhanced CCP Implementation:
 - PIC18F2423/2523 devices Two standard CCP modules
 - PIC18F4423/4523 devices One standard CCP module and one ECCP module
- Parallel Slave Port Present only on PIC18F4423/4523 devices

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F2423/2523/4423/4523 family are available only as low-voltage devices, designated by "LF" (such as PIC18**LF**2423), and function over an extended VDD range of 2.0V to 5.5V.



FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM

Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

2: RE3 is only available when MCLR functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see Section 2.0 "Oscillator Configurations" of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).



- **2:** RE3 is only available when MCLR functionality is disabled.
- 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see Section 2.0 "Oscillator Configurations" of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

Din Nomo	Pin Number			Pin	Buffer	Description
Pin Name	PDIP	QFN	TQFP	Туре	Туре	Description
MCLR/VPP/RE3 MCLR	1	18	18	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.
Vpp				Р		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI/RA7 OSC1	13	32	30	I	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode;
CLKI				Ι	CMOS	analog otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7				I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6 OSC2	14	33	31	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				0	_	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cvcle rate.
RA6				I/O	TTL	General purpose I/O pin.
Legend: TTL = TTL ST = Sch O = Out I^2C = I^2C^3	compat mitt Trig out ™/SMBเ	ible inp ger inpi is	ut ut with C	CMOS = CMOS compatible input or output I = Input P = Power		

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

Din Namo	Pi	n Numb	ber	Pin	Buffer	Description	
	PDIP	QFN	TQFP	Туре	Туре	Description	
						PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled.	
RD0/PSP0 RD0 PSP0	19	38	38	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD1/PSP1 RD1 PSP1	20	39	39	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD2/PSP2 RD2 PSP2	21	40	40	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD3/PSP3 RD3 PSP3	22	41	41	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD4/PSP4 RD4 PSP4	27	2	2	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD5/PSP5/P1B RD5 PSP5 P1B	28	3	3	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. Enhanced CCP1 output.	
RD6/PSP6/P1C RD6 PSP6 P1C	29	4	4	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. Enhanced CCP1 output.	
RD7/PSP7/P1D RD7 PSP7 P1D	30	5	5	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. Enhanced CCP1 output.	
Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels I = Input O = Output P = Power							

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

O = Output $I^{2}C = I^{2}C^{TM}/SMBus$

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

The value in the ADRESH:ADRESL registers is unknown following POR and BOR Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**.

After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

- 1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on the A/D module (ADCON0)
- 2. Configure the A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
- 3. Wait the required acquisition time (if required).
- Start conversion by setting the GO/DONE bit (ADCON0<1>).

- 5. Wait for the A/D conversion to complete by either:
 - Polling for the GO/DONE bit to be cleared
 OR

· Waiting for the A/D interrupt

- 6. Read the A/D Result registers (ADRESH:ADRESL) and clear the ADIF bit, if required.
- 7. For the next conversion, go to step 1 or step 2, as required.

The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

FIGURE 2-2: A/D TRANSFER FUNCTION





FIGURE 2-3: ANALOG INPUT MODEL

2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition time is <u>selected</u> when ACQT<2:0> = 0.00. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 Tosc
- 32 Tosc
 64 Tosc
- 4 Tosc
- Internal RC Oscillator
- 8 Tosc 16 Tosc
 -)SC

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

A/D Clock So	urce (TAD)	Assumes TAD Min. = 0.8 μ s
Operation	ADCS<2:0>	Maximum Fosc
2 Tosc	000	2.50 MHz
4 Tosc	100	5.00 MHz
8 Tosc	001	10.00 MHz
16 Tosc	101	20.00 MHz
32 Tosc	010	40.00 MHz
64 Tosc	110	40.00 MHz
RC ⁽²⁾	x11	1.00 MHz ⁽¹⁾

TABLE 2-2:TAD vs. DEVICE OPERATING FREQUENCIES

Note 1: The RC source has a typical TAD time of 2.5 μ s.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT<2:0> bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/DONE bit has been set, the ACQT<2:0> bits have been set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is completed or aborted, a 2 TcY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note:	The GO/DONE bit should NOT be set in
	the same instruction that turns on the A/D.
	Code should wait at least 3 TAD after
	enabling the A/D before beginning an
	acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unitygain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.





FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)





TABLE 4-1:A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL)PIC18LF2423/2523/4423/4523 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Тур	Мах	Units		Conditions
A01	NR	Resolution	—	_	12	bit		$\Delta V \text{REF} \geq 3.0 V$
A03	EIL	Integral Linearity Error	—	<±1	±2.0	LSB	VDD = 3.0V	$\Delta \text{VREF} \geq 3.0 \text{V}$
			—	—	±2.0	LSB	VDD = 5.0V	
A04	Edl	Differential Linearity Error	—	<±1	+1.5/-1.0	LSB	VDD = 3.0V	$\Delta \text{VREF} \geq 3.0 \text{V}$
			—	_	+1.5/-1.0	LSB	VDD = 5.0V	
A06	EOFF	Offset Error	—	<±1	±5	LSB	VDD = 3.0V	$\Delta VREF \ge 3.0V$
			—	_	±3	LSB	VDD = 5.0V	
A07	Egn	Gain Error	—	<±1	±1.25	LSB	VDD = 3.0V	$\Delta \text{VREF} \geq 3.0 \text{V}$
			—	—	±2.00	LSB	VDD = 5.0V	
A10	_	Monotonicity	Gu	arantee	d ⁽¹⁾	_		$VSS \leq VAIN \leq VREF$
A20	$\Delta VREF$	Reference Voltage Range (VREFH – VREFL)	3	—	Vdd - Vss	V		For 12-bit resolution.
A21	Vrefh	Reference Voltage High	Vss + 3.0V	_	VDD + 0.3V	V		For 12-bit resolution.
A22	Vrefl	Reference Voltage Low	Vss – 0.3V	_	Vdd - 3.0V	V		For 12-bit resolution.
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V		
A30	Zain	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ		
A50	IREF	VREF Input Current ⁽²⁾	—	_	5 150	μΑ μΑ		During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

NOTES:

5.0 PACKAGING INFORMATION

For packaging information, see **Section 28.0 "Packaging Information"** in the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2006)

Original data sheet for PIC18F2423/2523/4423/4523 devices.

Revision B (January 2007)

This revision includes updates to the packaging diagrams.

Revision C (September 2009)

Electrical specifications updated. Preliminary condition status removed. Converted document to the "mini data sheet" format.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Program Memory (Bytes)	16384	32768	16384	32768
Program Memory (Instructions)	8192	16384	8192	16384
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

TABLE B-1:DEVICE DIFFERENCES

R

Reader Response	. 52
Registers	
ADCON0 (A/D Control 0)	. 25
ADCON1 (A/D Control 1)	. 26
ADCON2 (A/D Control 2)	. 27
DEVID1 (Device ID 1)	. 35
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PRODUCT IDENTIFICATION SYSTEM

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PART NO.	X Temperature	/XX Package	XXX Pattern	Exa a)	ample PIC ⁻	95: 18F452	:3-I/P 301 = Industrial temp., PDIP	
Device	Range PIC18F2423 ⁽¹⁾ , P PIC18F4523T ⁽²⁾ ; VDD range 4.21 PIC18F2423 ⁽¹⁾ , P PIC18F4232T ⁽²⁾ ; VDD range 2.0V	PIC18F2523 ⁽¹⁾ V to 5.5V IC18F2523 ⁽¹⁾ V to 5.5V	⁾ , PIC18F4423T ⁽²⁾ , ⁾ , PIC18F4423T ⁽²⁾ ,	b) c)	pack #30 ⁻ PIC pack PIC pack	package, Extended VDD limits, QTP pattern #301. PIC18F4523-I/PT = Industrial temp., TQFP package, Extended VDD limits. PIC18F4523-E/P = Extended temp., PDIP package, normal VDD limits.		
Temperature Range	$ \begin{array}{rcl} I & = -40^{\circ}C \\ E & = -40^{\circ}C \end{array} $	to +85°C to +125°C	(Industrial) (Extended)					
Package	PT = TQF ML = QFN SO = SOI(SP = Skini P = PDIF	P (Thin Quad C ny Plastic DIF	l Flat pack)	Not	e 1: 2:	F = LF = T =	 Standard Voltage Range Wide Voltage Range In tape and reel PLCC, and TQFP packages only. 	
Pattern	QTP, SQTP, Code (blank otherwise)	e or Special F	Requirements					



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