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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18lf2523t-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic18lf2523t-i-ml</a>

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**MICROCHIP****PIC18F2423/2523/4423/4523**

## 28/40/44-Pin, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

**Power Management Features:**

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Ultra Low 50 nA Input Leakage
- Run mode Currents Down to 11  $\mu$ A Typical
- Idle mode Currents Down to 2.5  $\mu$ A Typical
- Sleep mode Current Down to 100  $\mu$ A Typical
- Timer1 Oscillator: 900 nA, 32 kHz, 2V
- Watchdog Timer: 1.4  $\mu$ A, 2V Typical
- Two-Speed Oscillator Start-up

**Flexible Oscillator Structure:**

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL) – Available for Crystal and Internal Oscillators
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
  - Fast wake from Sleep and Idle, 1  $\mu$ s typical
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds, from 31 kHz to 32 MHz, when used with PLL
  - User-tunable to Compensate for Frequency Drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops

**Peripheral Highlights:**

- 12-Bit, Up to 13-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep mode
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Three Programmable External Interrupts
- Four Input Change Interrupts
- Up to Two Capture/Compare/PWM (CCP) modules, One with Auto-Shutdown (28-pin devices)
- Enhanced Capture/Compare/PWM (ECCP) module (40/44-pin devices only):
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart

**Peripheral Highlights (Continued):**

- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all four modes) and I<sup>2</sup>C™ Master and Slave modes
- Enhanced USART module:
  - Support for RS-485, RS-232 and LIN/J2602
  - RS-232 operation using internal oscillator block (no external crystal required)
  - Auto-wake-up on Start bit
  - Auto-Baud Detect (ABD)

**Special Microcontroller Features:**

- C Compiler Optimized Architecture: Optional Extended Instruction Set Designed to Optimize Re-Entrant Code
- 100,000 Erase/Write Cycle, Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle, Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT): Programmable Period, from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Operating Voltage Range: 2.0V to 5.5V
- Programmable, 16-Level High/Low-Voltage Detection (HLVD) module: Supports Interrupt on High/Low-Voltage Detection
- Programmable Brown-out Reset (BOR): With Software-Enable Option

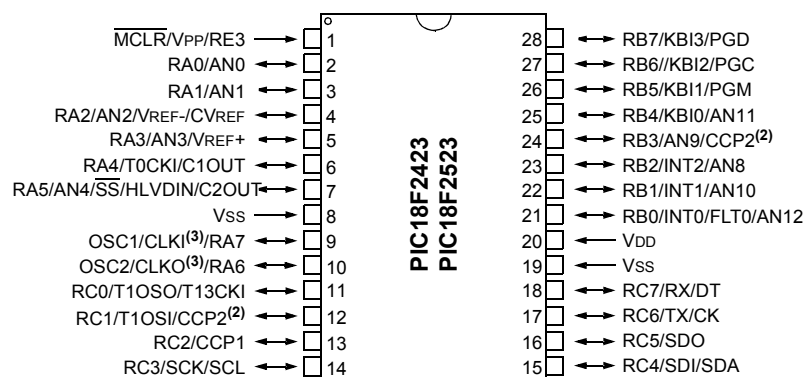
**Note:** This document is supplemented by the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631). See **Section 1.0 "Device Overview"**.

Device	Program Memory		Data Memory		I/O	12-Bit A/D (ch)	CCP/ ECCP (PWM)	MSSP		EUSART	Comp.	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I <sup>2</sup> C™			
PIC18F2423	16K	8192	768	256	25	10	2/0	Y	Y	1	2	1/3
PIC18F2523	32K	16384	1536	256	25	10	2/0	Y	Y	1	2	1/3
PIC18F4423	16K	8192	768	256	36	13	1/1	Y	Y	1	2	1/3
PIC18F4523	32K	16384	1536	256	36	13	1/1	Y	Y	1	2	1/3

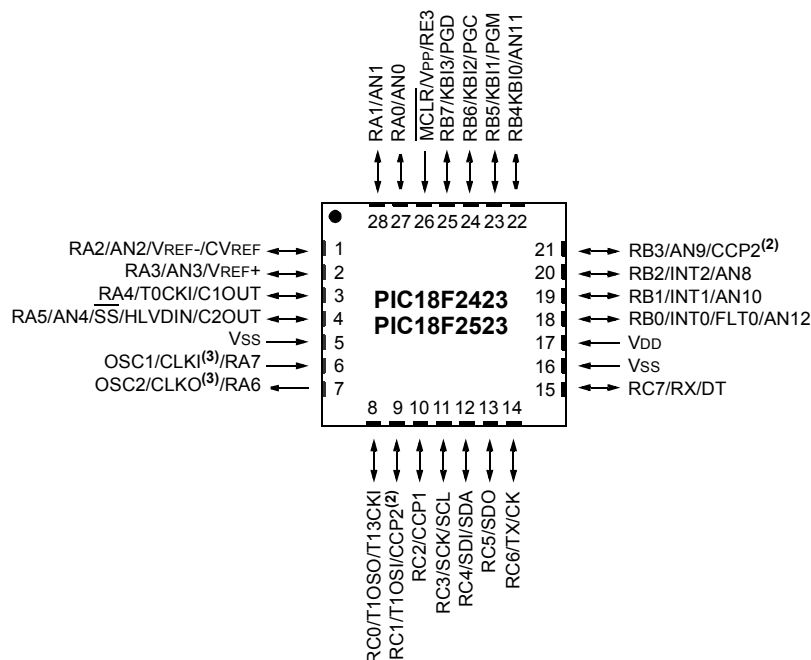
# PIC18F2423/2523/4423/4523

## Pin Diagrams

### 28-Pin PDIP, SOIC



### 28-Pin QFN<sup>(1)</sup>



- Note**
- 1: It is recommended to connect the bottom pad of QFN package parts to Vss.
  - 2: RB3 is the alternate pin for CCP2 multiplexing.
  - 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

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# PIC18F2423/2523/4423/4523

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## 1.2 Other Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, thereby reducing code overhead.
- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-Programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it is possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18F2423/2523/4423/4523 family introduces an optional extension to the PIC18 instruction set that adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **Enhanced CCP module:** In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown, for disabling PWM outputs on interrupt or other select conditions, and auto-restart, to reactivate outputs once the condition has cleared.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **Extended Watchdog Timer (WDT):** This Enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 4.0 “Electrical Characteristics”** for time-out periods.

## 1.3 Details on Individual Family Members

Devices in the PIC18F2423/2523/4423/4523 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18F2423/4423 devices – 16 Kbytes
  - PIC18F2523/4523 devices – 32 Kbytes
- A/D Channels:
  - PIC18F2423/2523 devices – 10
  - PIC18F4423/4523 devices – 13
- I/O Ports:
  - PIC18F2423/2523 devices – Three bidirectional ports
  - PIC18F4423/4523 devices – Five bidirectional ports
- CCP and Enhanced CCP Implementation:
  - PIC18F2423/2523 devices – Two standard CCP modules
  - PIC18F4423/4523 devices – One standard CCP module and one ECCP module
- Parallel Slave Port – Present only on PIC18F4423/4523 devices

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F2423/2523/4423/4523 family are available only as low-voltage devices, designated by “LF” (such as PIC18**LF**2423), and function over an extended VDD range of 2.0V to 5.5V.

# PIC18F2423/2523/4423/4523

**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
RA0/AN0	2	27	I/O	TTL	PORTA is a bidirectional I/O port.
RA0			I	Analog	Digital I/O.
AN0					Analog Input 0.
RA1/AN1	3	28	I/O	TTL	Digital I/O.
RA1			I	Analog	Analog Input 1.
AN1					
RA2/AN2/VREF-/CVREF	4	1	I/O	TTL	Digital I/O.
RA2			I	Analog	Analog Input 2.
AN2			I	Analog	A/D reference voltage (low) input.
VREF-					
CVREF			O	Analog	Comparator reference voltage output.
RA3/AN3/VREF+	5	2	I/O	TTL	Digital I/O.
RA3			I	Analog	Analog Input 3.
AN3			I	Analog	A/D reference voltage (high) input.
VREF+					
RA4/T0CKI/C1OUT	6	3	I/O	ST	Digital I/O.
RA4			I	ST	Timer0 external clock input.
T0CKI					
C1OUT			O	—	Comparator 1 output.
RA5/AN4/ $\overline{SS}$ /HLVDIN/C2OUT	7	4	I/O	TTL	Digital I/O.
RA5			I	Analog	Analog Input 4.
AN4			I	TTL	SPI slave select input.
$\overline{SS}$			I	Analog	High/Low-Voltage Detect input.
HLVDIN					
C2OUT			O	—	Comparator 2 output.
RA6					See the OSC2/CLKO/RA6 pin.
RA7					See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.



# PIC18F2423/2523/4423/4523

**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
RB0/INT0/FLT0/AN12	21	18	I/O I I I	TTL ST ST Analog	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.  Digital I/O. External Interrupt 0. PWM Fault input for CCP1. Analog Input 12.
RB1/INT1/AN10	22	19	I/O I I	TTL ST Analog	Digital I/O. External Interrupt 1. Analog Input 10.
RB2/INT2/AN8	23	20	I/O I I	TTL ST Analog	Digital I/O. External Interrupt 2. Analog Input 8.
RB3/AN9/CCP2	24	21	I/O I I/O	TTL Analog ST	Digital I/O. Analog Input 9. Capture 2 input/Compare 2 output/PWM2 output.
RB4/KBI0/AN11	25	22	I/O I I	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. Analog Input 11.
RB5/KBI1/PGM	26	23	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	27	24	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28	25	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/VPP/RE3 MCLR  VPP RE3	1	18	18	I  P I	ST   ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI/RA7 OSC1  CLKI  RA7	13	32	30	I  I I/O	ST  CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; analog otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2  CLKO  RA6	14	33	31	O  O I/O	—  — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

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NOTES:

# PIC18F2423/2523/4423/4523

## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the PIC18F2423/2523 devices and 13 for the PIC18F4423/4523 devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

Of the ADCONx registers:

- ADCON0 (shown in Register 2-1) – Controls the module's operation
- ADCON1 (Register 2-2) – Configures the functions of the port pins
- ADCON2 (Register 2-3) – Configures the A/D clock source, programmed acquisition time and justification

### REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS<3:0>:** Analog Channel Select bits

0000 = Channel 0 (AN0)  
 0001 = Channel 1 (AN1)  
 0010 = Channel 2 (AN2)  
 0011 = Channel 3 (AN3)  
 0100 = Channel 4 (AN4)  
 0101 = Channel 5 (AN5)<sup>(1,2)</sup>  
 0110 = Channel 6 (AN6)<sup>(1,2)</sup>  
 0111 = Channel 7 (AN7)<sup>(1,2)</sup>  
 1000 = Channel 8 (AN8)  
 1001 = Channel 9 (AN9)  
 1010 = Channel 10 (AN10)  
 1011 = Channel 11 (AN11)  
 1100 = Channel 12 (AN12)  
 1101 = Unimplemented<sup>(2)</sup>  
 1110 = Unimplemented<sup>(2)</sup>  
 1111 = Unimplemented<sup>(2)</sup>

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on PIC18F2423/2523 devices.

**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition time is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-2: TAD vs. DEVICE OPERATING FREQUENCIES**

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 $\mu$ s
Operation	ADCS<2:0>	Maximum Fosc
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	40.00 MHz
RC <sup>(2)</sup>	x11	1.00 MHz <sup>(1)</sup>

**Note 1:** The RC source has a typical TAD time of 2.5  $\mu$ s.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the  $ADCS<2:0>$  bits in  $ADCON2$  should be updated in accordance with the clock source to be used. The  $ACQT<2:0>$  bits do not need to be adjusted as the  $ADCS<2:0>$  bits adjust the  $TAD$  time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits,  $ACQT<2:0>$ , are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The  $IDLEN$  bit ( $OSCCON<7>$ ) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The  $ADCON1$ ,  $TRISA$ ,  $TRISB$  and  $TRISE$  registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding  $TRIS$  bits set (input). If the  $TRIS$  bit is cleared (output), the digital output level ( $V_{OH}$  or  $V_{OL}$ ) will be converted.

The A/D operation is independent of the state of the  $CHS<3:0>$  bits and the  $TRIS$  bits.

- Note 1:** When reading the  $PORT$  register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

**3:** The  $PBADEN$  bit in Configuration Register 3H configures  $PORTB$  pins to reset as analog or digital pins by controlling how the  $PCFG<3:0>$  bits in  $ADCON1$  are reset.

# PIC18F2423/2523/4423/4523

## 2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location).

The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-3: REGISTERS ASSOCIATED WITH A/D OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(Note 4)
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	(Note 4)
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	(Note 4)
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	(Note 4)
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	(Note 4)
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	(Note 4)
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	(Note 4)
ADRESH	A/D Result Register High Byte								(Note 4)
ADRESL	A/D Result Register Low Byte								(Note 4)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	(Note 4)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(Note 4)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(Note 4)
PORTA	RA7 <sup>(2)</sup>	RA6 <sup>(2)</sup>	RA5	RA4	RA3	RA2	RA1	RA0	(Note 4)
TRISA	TRISA7 <sup>(2)</sup>	TRISA6 <sup>(2)</sup>	PORTA Data Direction Control Register						(Note 4)
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	(Note 4)
TRISB	PORTB Data Direction Control Register								(Note 4)
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								(Note 4)
PORTE <sup>(1)</sup>	—	—	—	—	RE3 <sup>(3)</sup>	RE2	RE1	RE0	(Note 4)
TRISE <sup>(1)</sup>	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	(Note 4)
LATE <sup>(1)</sup>	—	—	—	—	—	PORTE Data Latch Register			(Note 4)

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** These registers and/or bits are not implemented on PIC18F2423/2523 devices and are read as '0'.

**2:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**3:** RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

**4:** For these Reset values, see **Section 4.0 "Reset"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

# PIC18F2423/2523/4423/4523

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV11 <sup>(1)</sup>	DEV10 <sup>(1)</sup>	DEV9 <sup>(1)</sup>	DEV8 <sup>(1)</sup>	DEV7 <sup>(1)</sup>	DEV6 <sup>(1)</sup>	DEV5 <sup>(1)</sup>	DEV4 <sup>(1)</sup>
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-0      **DEV<11:4>**: Device ID bits<sup>(1)</sup>

These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number.

0001 0001 = PIC18F2423/2523 devices

0001 0000 = PIC18F4423/4523 devices

**Note 1:** These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.



# PIC18F2423/2523/4423/4523

FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

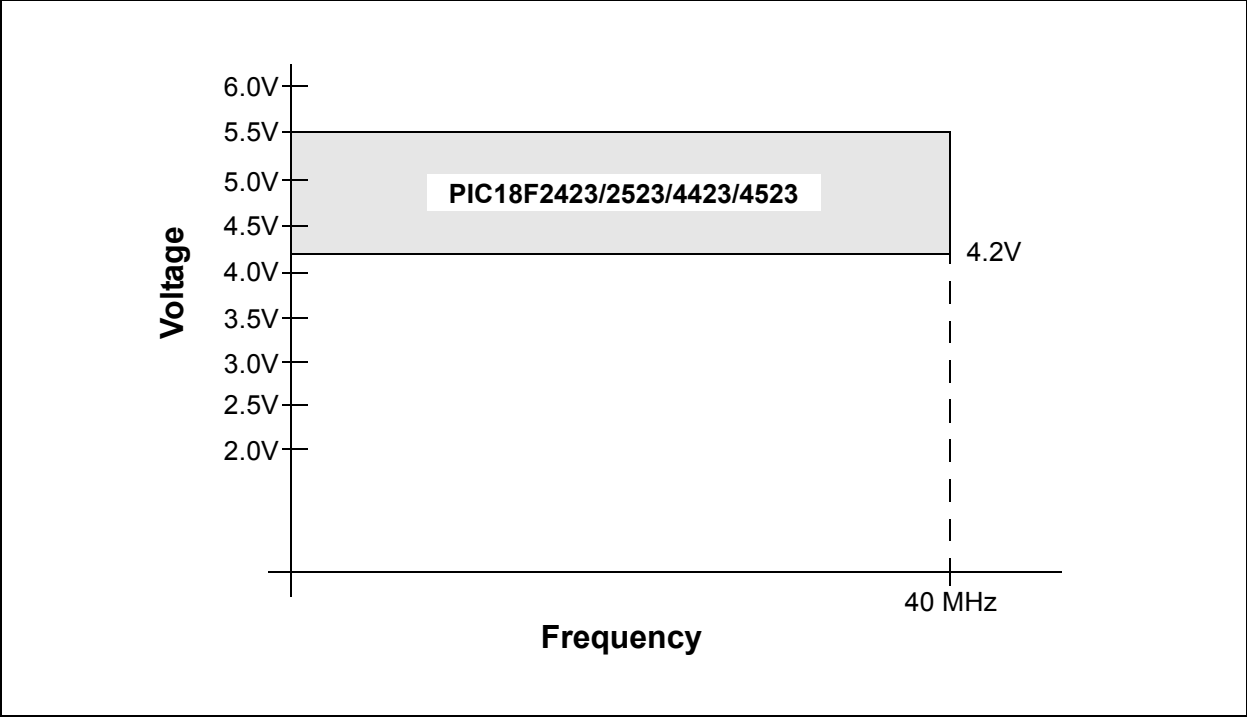
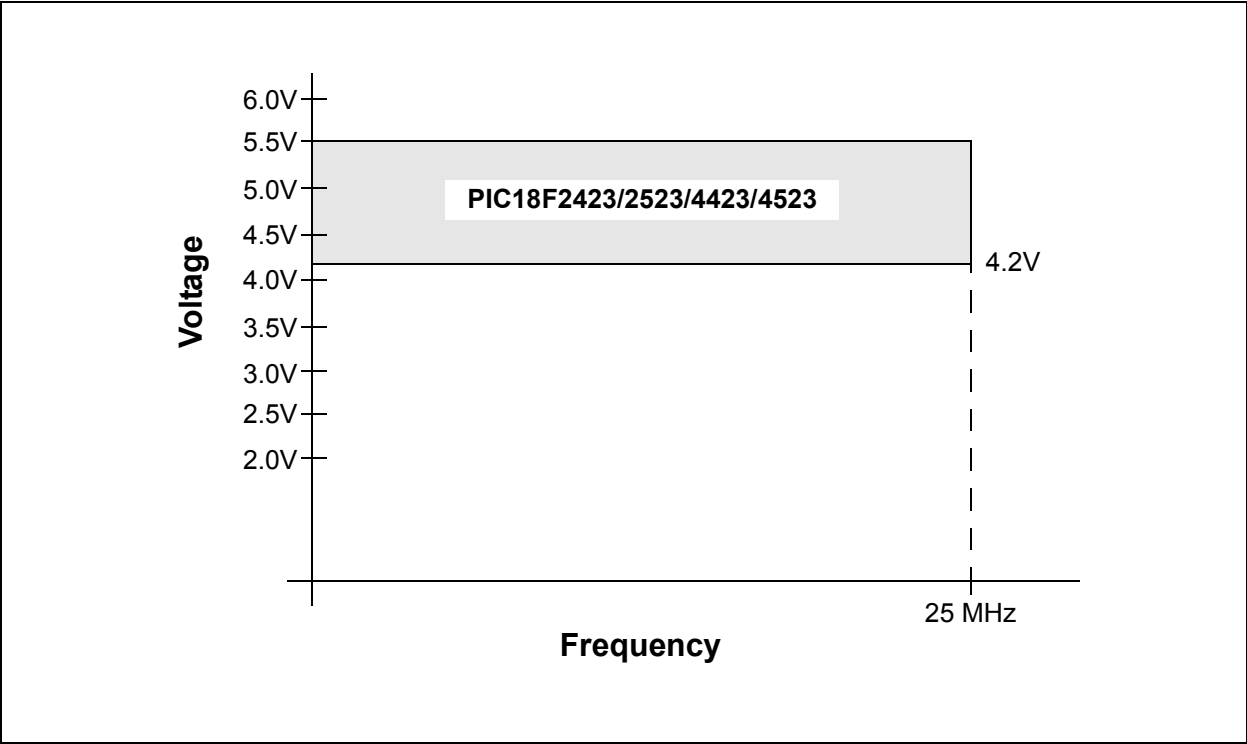
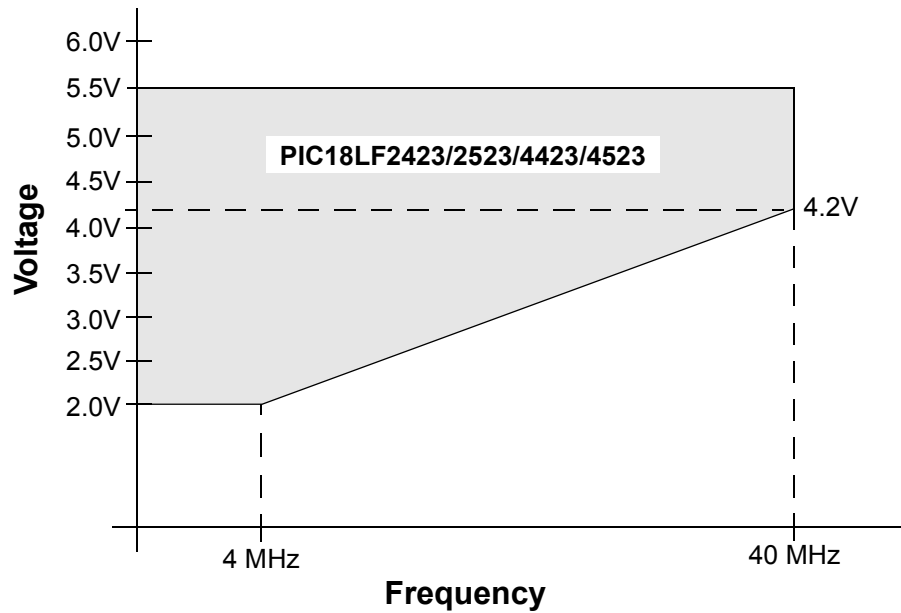


FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



# PIC18F2423/2523/4423/4523

FIGURE 4-3: PIC18LF2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



$$F_{MAX} = (16.36 \text{ MHz/V}) (V_{DDAPP\text{MIN}} - 2.0\text{V}) + 4 \text{ MHz}$$

**Note:**  $V_{DDAPP\text{MIN}}$  is the minimum voltage of the PIC<sup>®</sup> device in the application.

# PIC18F2423/2523/4423/4523

**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL)  
PIC18LF2423/2523/4423/4523 (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	$\pm 2.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.0$	LSB	$V_{DD} = 5.0V$	
A04	EDL	Differential Linearity Error	—	$<\pm 1$	$+1.5/-1.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$+1.5/-1.0$	LSB	$V_{DD} = 5.0V$	
A06	EOFF	Offset Error	—	$<\pm 1$	$\pm 5$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 3$	LSB	$V_{DD} = 5.0V$	
A07	EGN	Gain Error	—	$<\pm 1$	$\pm 1.25$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.00$	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed <sup>(1)</sup>			—		$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	$\Delta V_{REF}$	Reference Voltage Range ( $V_{REFH} - V_{REFL}$ )	3	—	$V_{DD} - V_{SS}$	V		For 12-bit resolution.
A21	$V_{REFH}$	Reference Voltage High	$V_{SS} + 3.0V$	—	$V_{DD} + 0.3V$	V		For 12-bit resolution.
A22	$V_{REFL}$	Reference Voltage Low	$V_{SS} - 0.3V$	—	$V_{DD} - 3.0V$	V		For 12-bit resolution.
A25	$V_{AIN}$	Analog Input Voltage	$V_{REFL}$	—	$V_{REFH}$	V		
A30	$Z_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	2.5	k $\Omega$		
A50	$I_{REF}$	$V_{REF}$ Input Current <sup>(2)</sup>	—	—	5	$\mu A$		During $V_{AIN}$ acquisition. During A/D conversion cycle.
			—	—	150	$\mu A$		

- Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
- Note 2:**  $V_{REFH}$  current is from the RA3/AN3/ $V_{REF+}$  pin or  $V_{DD}$ , whichever is selected as the  $V_{REFH}$  source.  $V_{REFL}$  current is from the RA2/AN2/ $V_{REF-}/CV_{REF}$  pin or  $V_{SS}$ , whichever is selected as the  $V_{REFL}$  source.

# PIC18F2423/2523/4423/4523

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NOTES:

# PIC18F2423/2523/4423/4523

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device	PIC18F2423 <sup>(1)</sup> , PIC18F2523 <sup>(1)</sup> , PIC18F4423T <sup>(2)</sup> , PIC18F4523T <sup>(2)</sup> ; VDD range 4.2V to 5.5V PIC18F2423 <sup>(1)</sup> , PIC18F2523 <sup>(1)</sup> , PIC18F4423T <sup>(2)</sup> , PIC18F4523T <sup>(2)</sup> ; VDD range 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flat pack) ML = QFN SO = SOIC SP = Skinny Plastic DIP P = PDIP		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

- a) PIC18F4523-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.
- b) PIC18F4523-I/PT = Industrial temp., TQFP package, Extended VDD limits.
- c) PIC18F4523-E/P = Extended temp., PDIP package, normal VDD limits.

**Note 1:** F = Standard Voltage Range  
LF = Wide Voltage Range  
**2:** T = In tape and reel PLCC, and TQFP packages only.