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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4423-i-ml

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Pin Diagrams (Continued)

44-Pin QFN[(1)]
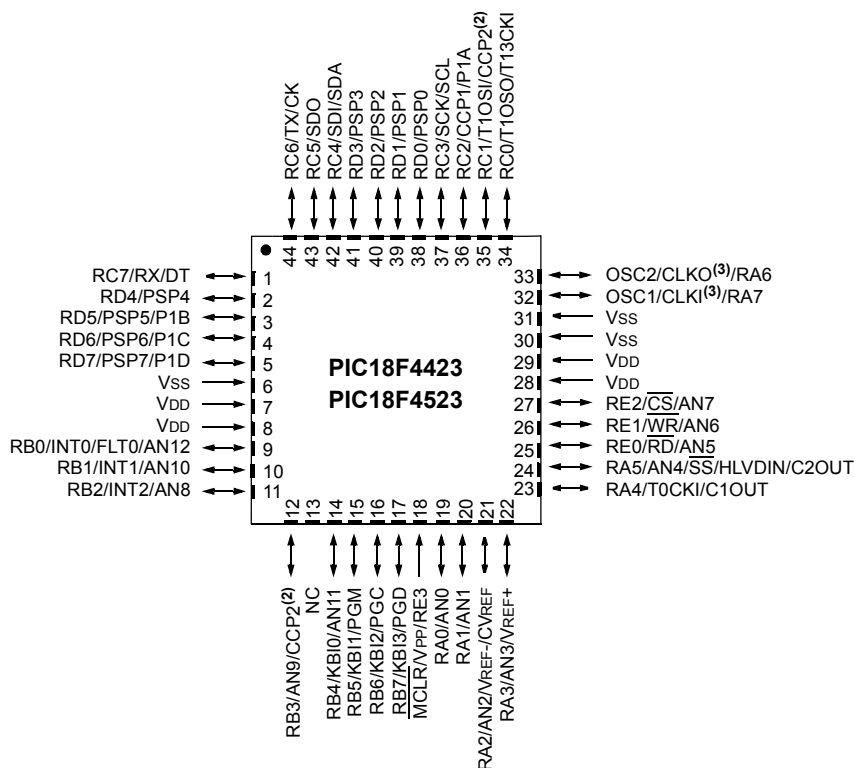
Note 1: It is recommended to connect the bottom pad of QFN package parts to Vss.

2: RB3 is the alternate pin for CCP2 multiplexing.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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1.0   DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2423
- PIC18F2523
- PIC18F4423
- PIC18F4523

- PIC18LF2423
- PIC18LF2523
- PIC18LF4423
- PIC18LF4523

> **Note:** This data sheet documents only the devices' features and specifications that are in addition to, or different from, the features and specifications of the PIC18F2420/2520/4420/4520 devices. For information on the features and specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. On top of these features, the PIC18F2423/2523/4423/4523 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1   New Core Features

1.1.1   nanoWatt TECHNOLOGY

All of the devices in the PIC18F2423/2523/4423/4523 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller also can run with its CPU core disabled and the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 4.0 "Electrical Characteristics"** for values.

1.1.2   MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2423/2523/4423/4523 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- Two External RC Oscillator modes with the same pin options as the External Clock modes.
- An internal oscillator block that offers eight clock frequencies: an 8 MHz clock and an INTRC source (approximately 31 kHz), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and Internal Oscillator modes, allowing clock speeds of up to 40 MHz from the HS clock source. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz, all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** Constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** Allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	16,384	32,768	16,384	32,768
Program Memory (Instructions)	8,192	16,384	8,192	16,384
Data Memory (Bytes)	768	1,536	768	1,536
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin QFN 44-Pin TQFP	40-Pin PDIP 44-Pin QFN 44-Pin TQFP

PIC18F2423/2523/4423/4523

TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
MCLR/VPP/RE3	1	26			Master Clear (input) or programming voltage (input).
MCLR			I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP			P		Programming voltage input.
RE3			I	ST	Digital input.
OSC1/CLKI/RA7	9	6			Oscillator crystal or external clock input.
OSC1			I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI			I	CMOS	External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7			I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	10	7			Oscillator crystal or clock output.
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6			I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
       ST = Schmitt Trigger input with CMOS levels   I = Input
       O = Output   P = Power
       I^2C = I^2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

     2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

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TABLE 1-2:   PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
RA0/AN0	2	27			PORTA is a bidirectional I/O port.
RA0			I/O	TTL	Digital I/O.
AN0			I	Analog	Analog Input 0.
RA1/AN1	3	28			
RA1			I/O	TTL	Digital I/O.
AN1			I	Analog	Analog Input 1.
RA2/AN2/VREF-/CVREF	4	1			
RA2			I/O	TTL	Digital I/O.
AN2			I	Analog	Analog Input 2.
VREF-			I	Analog	A/D reference voltage (low) input.
CVREF			O	Analog	Comparator reference voltage output.
RA3/AN3/VREF+	5	2			
RA3			I/O	TTL	Digital I/O.
AN3			I	Analog	Analog Input 3.
VREF+			I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT	6	3			
RA4			I/O	ST	Digital I/O.
T0CKI			I	ST	Timer0 external clock input.
C1OUT			O	—	Comparator 1 output.
RA5/AN4/$\overline{SS}$/HLVDIN/ C2OUT	7	4			
RA5			I/O	TTL	Digital I/O.
AN4			I	Analog	Analog Input 4.
$\overline{SS}$			I	TTL	SPI slave select input.
HLVDIN			I	Analog	High/Low-Voltage Detect input.
C2OUT			O	—	Comparator 2 output.
RA6					See the OSC2/CLKO/RA6 pin.
RA7					See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
                ST   = Schmitt Trigger input with CMOS levels   I   = Input
                O   = Output   P   = Power
                I2C = I2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog Input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog Input 1.
RA2/AN2/VREF-/CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog Input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Comparator reference voltage output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog Input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RA5/AN4/$\overline{SS}$/HLVDIN/ C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog Input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6						See the OSC2/CLKO/RA6 pin.
RA7						See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I = Input
O = Output   P = Power
I2C = I2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
     2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2[2]				I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A				O	—	Enhanced CCP1 output.
RC3/SCK/SCL	18	37	37			
RC3				I/O	ST	Digital I/O.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	I^{2}C	Synchronous serial clock input/output for I^{2}C™ mode.
RC4/SDI/SDA	23	42	42			
RC4				I/O	ST	Digital I/O.
SDI				I	ST	SPI data in.
SDA				I/O	I^{2}C	I^{2}C data I/O.
RC5/SDO	24	43	43			
RC5				I/O	ST	Digital I/O.
SDO				O	—	SPI data out.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see related RX/DT).
RC7/RX/DT	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see related TX/CK).

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I = Input
O = Output   P = Power
I^{2}C = I^{2}C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

NOTES:

2.0   12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the PIC18F2423/2523 devices and 13 for the PIC18F4423/4523 devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

• A/D Result High Register (ADRESH)
• A/D Result Low Register (ADRESL)
• A/D Control Register 0 (ADCON0)
• A/D Control Register 1 (ADCON1)
• A/D Control Register 2 (ADCON2)

Of the ADCONx registers:

• ADCON0 (shown in Register 2-1) – Controls the module's operation
• ADCON1 (Register 2-2) – Configures the functions of the port pins
• ADCON2 (Register 2-3) – Configures the A/D clock source, programmed acquisition time and justification

REGISTER 2-1:   ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5-2   **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)[1,2]
0110 = Channel 6 (AN6)[1,2]
0111 = Channel 7 (AN7)[1,2]
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12
1101 = Unimplemented[2]
1110 = Unimplemented[2]
1111 = Unimplemented[2]

bit 1   **GO/$\overline{DONE}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0   **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

Note 1:   These channels are not implemented on PIC18F2423/2523 devices.
   2:   Performing a conversion on unimplemented channels will return a floating input measurement.

FIGURE 4-1: **PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**
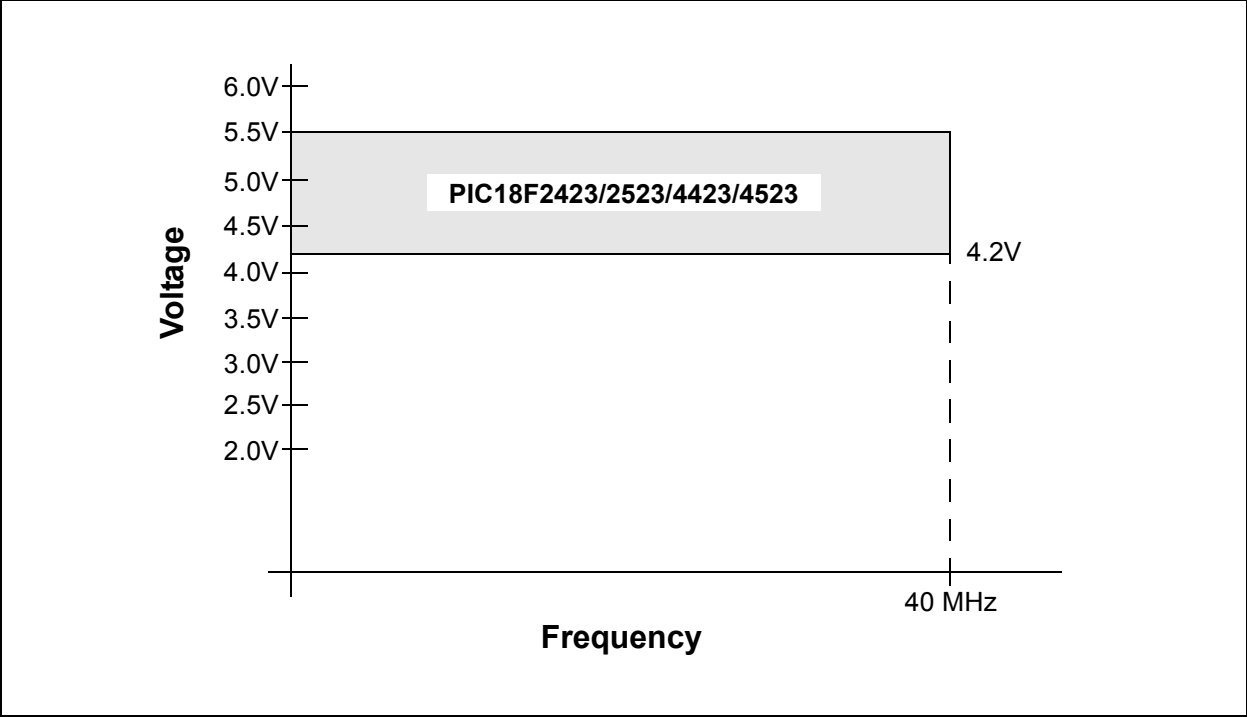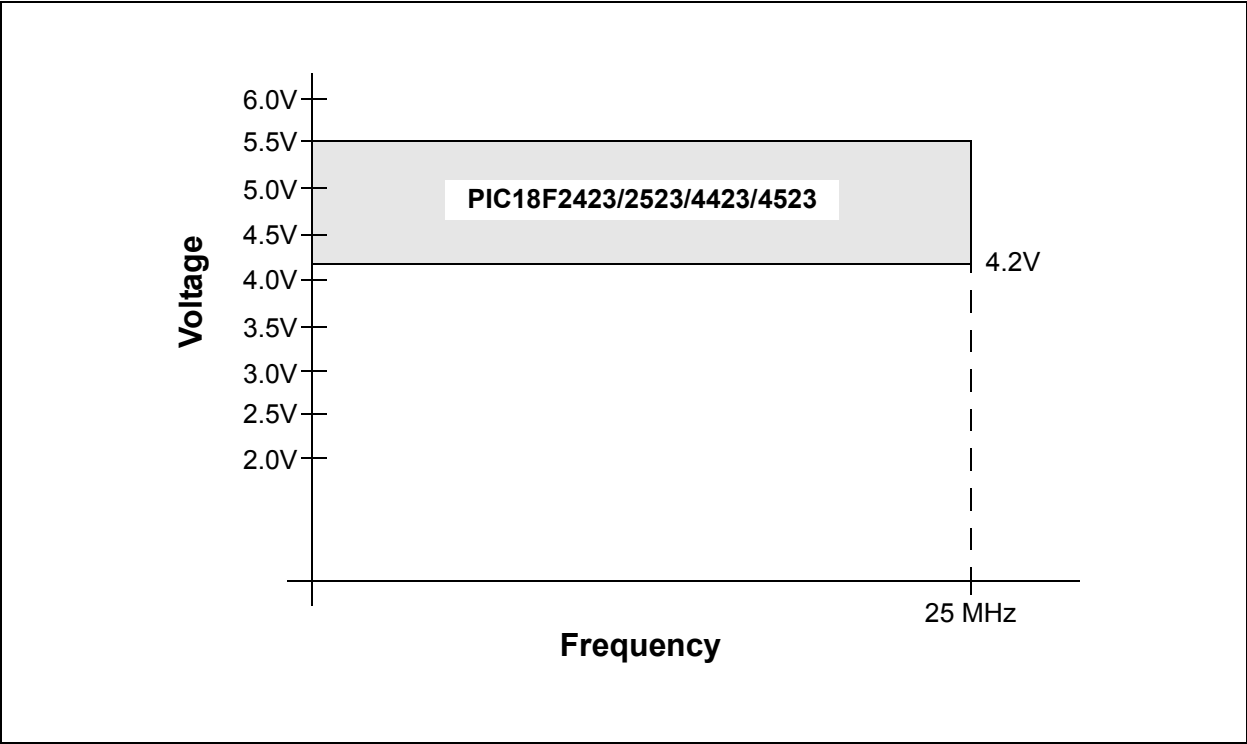

FIGURE 4-2: **PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)**

PIC18F2423/2523/4423/4523

TABLE 4-1: **A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL)**
PIC18LF2423/2523/4423/4523 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	N_R	Resolution	—	—	12	bit		$\Delta V_{REF} \geq 3.0V$
A03	E_{IL}	Integral Linearity Error	—	$<\pm 1$	± 2.0	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	± 2.0	LSB	$V_{DD} = 5.0V$	
A04	E_{DL}	Differential Linearity Error	—	$<\pm 1$	+1.5/-1.0	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	+1.5/-1.0	LSB	$V_{DD} = 5.0V$	
A06	E_{OFF}	Offset Error	—	$<\pm 1$	± 5	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	± 3	LSB	$V_{DD} = 5.0V$	
A07	E_{GN}	Gain Error	—	$<\pm 1$	± 1.25	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	± 2.00	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed[1]			—		$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range ($V_{REFH} - V_{REFL}$)	3	—	$V_{DD} - V_{SS}$	V		For 12-bit resolution.
A21	V_{REFH}	Reference Voltage High	$V_{SS} + 3.0V$	—	$V_{DD} + 0.3V$	V		For 12-bit resolution.
A22	V_{REFL}	Reference Voltage Low	$V_{SS} - 0.3V$	—	$V_{DD} - 3.0V$	V		For 12-bit resolution.
A25	V_{AIN}	Analog Input Voltage	V_{REFL}	—	V_{REFH}	V		
A30	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ		
A50	I_{REF}	V_{REF} Input Current[2]	—	—	5	μA		During V_{AIN} acquisition. During A/D conversion cycle.
			—	—	150	μA		

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: V_{REFH} current is from the RA3/AN3/V_{REF}+ pin or V_{DD}, whichever is selected as the V_{REFH} source. V_{REFL} current is from the RA2/AN2/V_{REF}-/CV_{REF} pin or V_{SS}, whichever is selected as the V_{REFL} source.

NOTES:

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

PIC18F2423/2523/4423/4523

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Application (optional):

Would you like a reply? ____Y ____N

Device: PIC18F2423/2523/4423/4523   Literature Number: DS39755C

Questions:

1. What are the best features of this document?

      _____

      _____

2. How does this document meet your hardware and software development needs?

      _____

      _____

3. Do you find the organization of this document easy to follow? If not, why?

      _____

      _____

4. What additions to the document do you think would enhance the structure and subject?

      _____

      _____

5. What deletions from the document could be made without affecting the overall usefulness?

      _____

      _____

6. Is there any incorrect or misleading information (what and where)?

      _____

      _____

7. How would you improve this document?

      _____

      _____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC18F2423[1], PIC18F2523[1], PIC18F4423T[2], PIC18F4523T[2];
	  V_DD range 4.2V to 5.5V
	PIC18F2423[1], PIC18F2523[1], PIC18F4423T[2], PIC18F4523T[2];
	  V_DD range 2.0V to 5.5V

Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package	PT = TQFP (Thin Quad Flat pack) ML = QFN SO = SOIC SP = Skinny Plastic DIP P = PDIP
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F4523-I/P 301 = Industrial temp., PDIP package, Extended V_DD limits, QTP pattern #301.

b) PIC18F4523-I/PT = Industrial temp., TQFP package, Extended V_DD limits.

c) PIC18F4523-E/P = Extended temp., PDIP package, normal V_DD limits.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = In tape and reel PLCC, and TQFP packages only.

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Fax: 248-538-2260

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