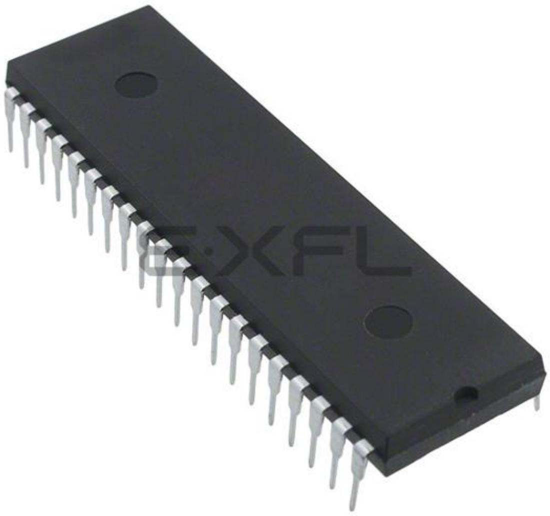
Microchip Technology - PIC18LF4423-I/P Datasheet



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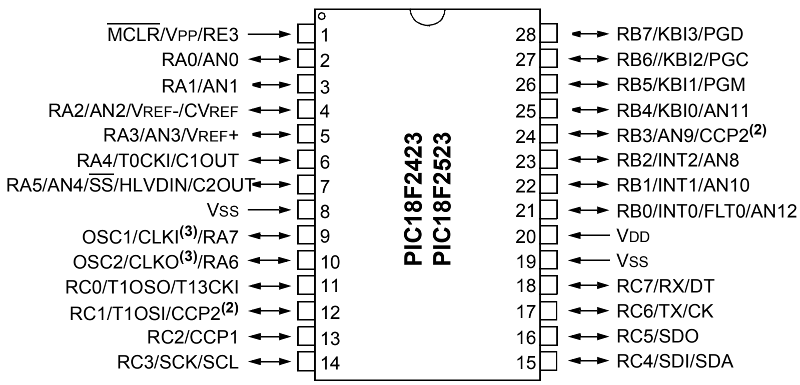
Applications of "Embedded - Microcontrollers"

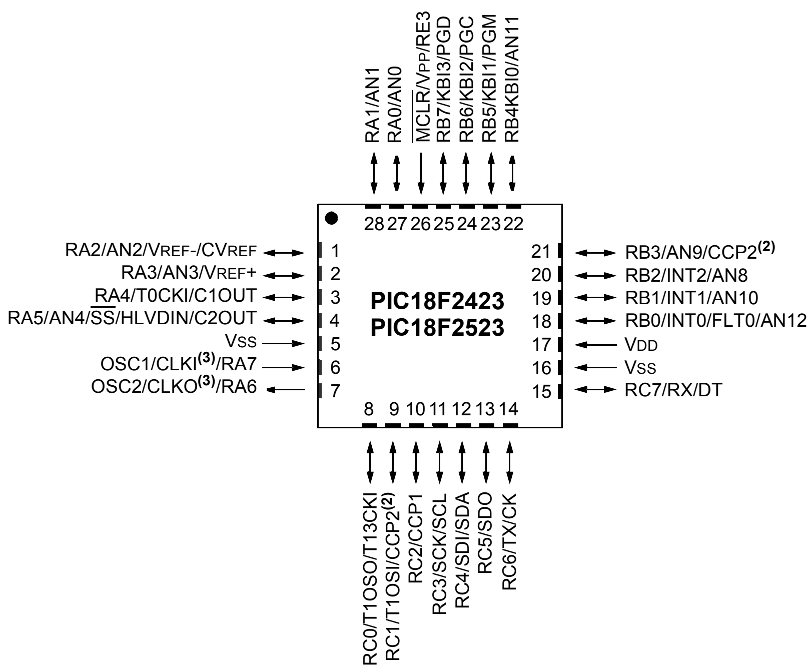
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4423-i-p

Pin Diagrams

28-Pin PDIP, SOIC



28-Pin QFN(1)



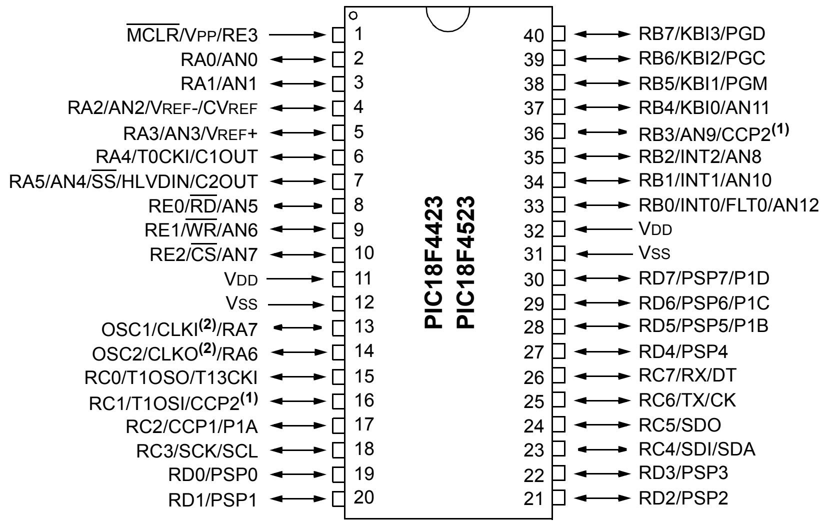
Note 1: It is recommended to connect the bottom pad of QFN package parts to VSS.

2: RB3 is the alternate pin for CCP2 multiplexing.

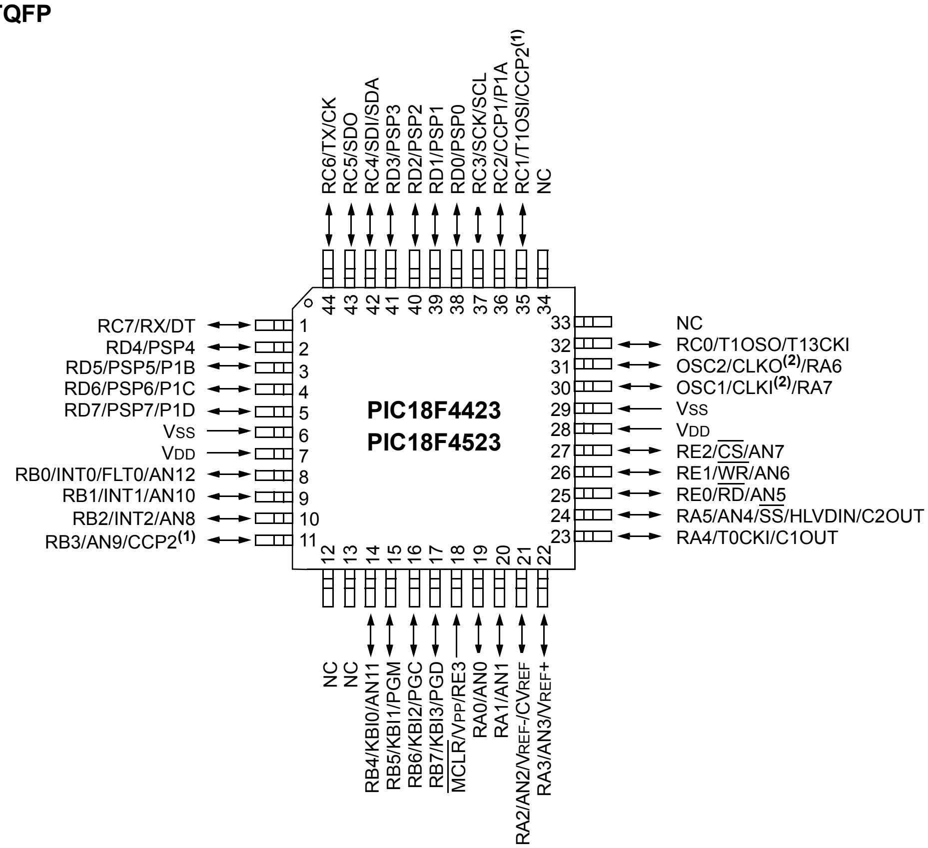
3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

Pin Diagrams (Continued)

40-Pin PDIP



44-Pin TQFP



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2423
- PIC18F2523
- PIC18F4423
- PIC18F4523
- PIC18LF2423
- PIC18LF2523
- PIC18LF4423
- PIC18LF4523

> **Note:** This data sheet documents only the devices' features and specifications that are in addition to, or different from, the features and specifications of the PIC18F2420/2520/4420/4520 devices. For information on the features and specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. On top of these features, the PIC18F2423/2523/4423/4523 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2423/2523/4423/4523 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller also can run with its CPU core disabled and the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 4.0 "Electrical Characteristics"** for values.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

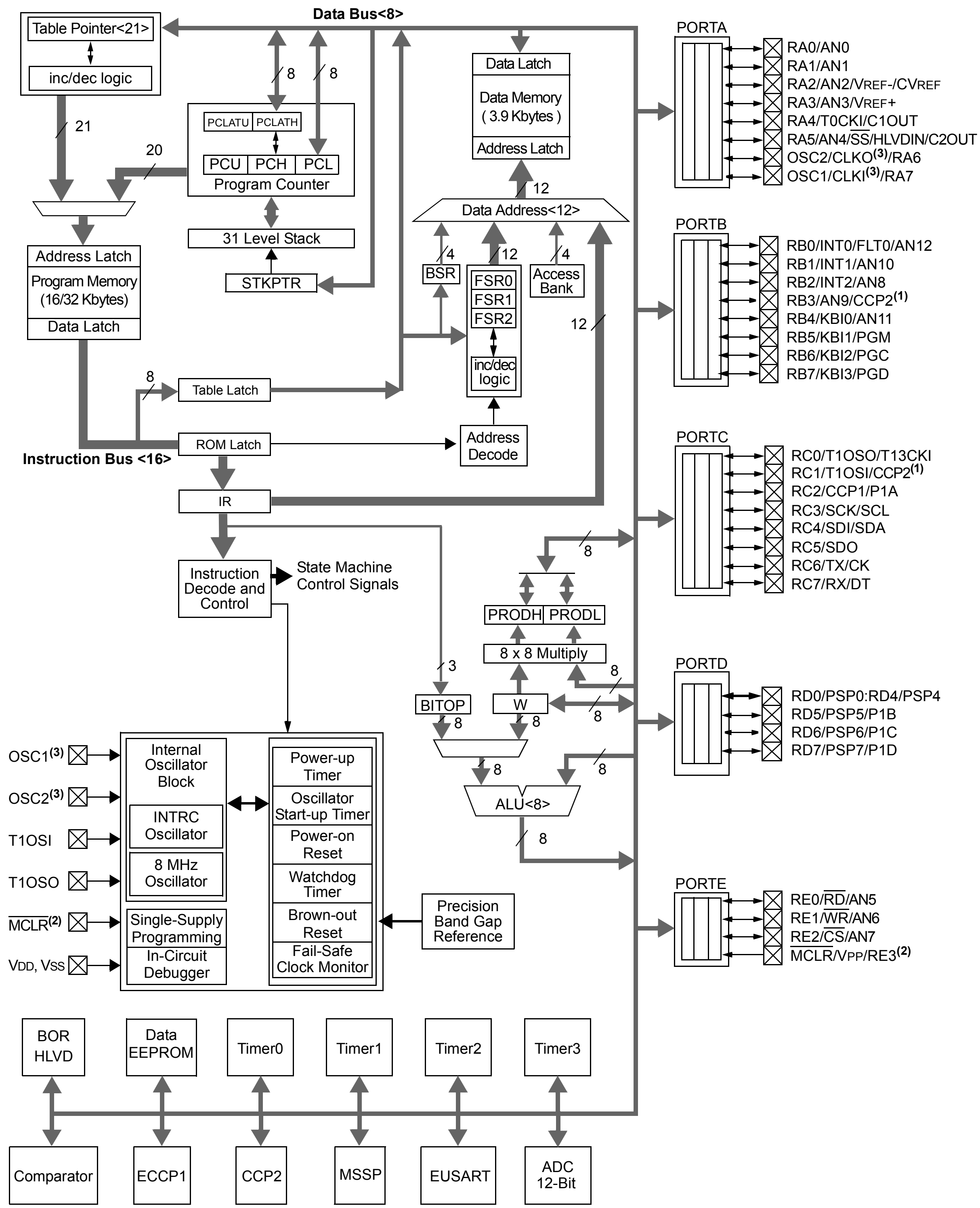
All of the devices in the PIC18F2423/2523/4423/4523 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- Two External RC Oscillator modes with the same pin options as the External Clock modes.
- An internal oscillator block that offers eight clock frequencies: an 8 MHz clock and an INTRC source (approximately 31 kHz), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and Internal Oscillator modes, allowing clock speeds of up to 40 MHz from the HS clock source. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz, all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** Constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** Allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

FIGURE 1-2: PIC18F4423/4523 (40/44-PIN) BLOCK DIAGRAM



Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

2: RE3 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 “Oscillator Configurations”** of the *“PIC18F2420/2520/4420/4520 Data Sheet”* (DS39631).

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
$\overline{MCLR}/V_{PP}$/RE3	1	18	18			Master Clear (input) or programming voltage (input).
$\overline{MCLR}$				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
V_{PP}				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI/RA7	13	32	30			Oscillator crystal or external clock input.
OSC1				I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; analog otherwise.
CLKI				I	CMOS	External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7				I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; I^2C = I^2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A				O	—	Enhanced CCP1 output.
RC3/SCK/SCL	18	37	37			
RC3				I/O	ST	Digital I/O.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	I^2C	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	23	42	42			
RC4				I/O	ST	Digital I/O.
SDI				I	ST	SPI data in.
SDA				I/O	I^2C	I^2C data I/O.
RC5/SDO	24	43	43			
RC5				I/O	ST	Digital I/O.
SDO				O	—	SPI data out.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see related RX/DT).
RC7/RX/DT	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see related TX/CK).

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; I = Input
O = Output; P = Power
I^2C = I^2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled.
RD0/PSP0	19	38	38			
RD0				I/O	ST	Digital I/O.
PSP0				I/O	TTL	Parallel Slave Port data.
RD1/PSP1	20	39	39			
RD1				I/O	ST	Digital I/O.
PSP1				I/O	TTL	Parallel Slave Port data.
RD2/PSP2	21	40	40			
RD2				I/O	ST	Digital I/O.
PSP2				I/O	TTL	Parallel Slave Port data.
RD3/PSP3	22	41	41			
RD3				I/O	ST	Digital I/O.
PSP3				I/O	TTL	Parallel Slave Port data.
RD4/PSP4	27	2	2			
RD4				I/O	ST	Digital I/O.
PSP4				I/O	TTL	Parallel Slave Port data.
RD5/PSP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
PSP5				I/O	TTL	Parallel Slave Port data.
P1B				O	—	Enhanced CCP1 output.
RD6/PSP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
PSP6				I/O	TTL	Parallel Slave Port data.
P1C				O	—	Enhanced CCP1 output.
RD7/PSP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
PSP7				I/O	TTL	Parallel Slave Port data.
P1D				O	—	Enhanced CCP1 output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; I^2C = I^2C™/SMBus

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

NOTES:

2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the PIC18F2423/2523 devices and 13 for the PIC18F4423/4523 devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

Of the ADCONx registers:

- ADCON0 (shown in Register 2-1) – Controls the module's operation
- ADCON1 (Register 2-2) – Configures the functions of the port pins
- ADCON2 (Register 2-3) – Configures the A/D clock source, programmed acquisition time and justification

REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS<3:0>:** Analog Channel Select bits

0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)[1,2]
0110 = Channel 6 (AN6)[1,2]
0111 = Channel 7 (AN7)[1,2]
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12
1101 = Unimplemented[2]
1110 = Unimplemented[2]
1111 = Unimplemented[2]

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

<u>When ADON = 1:</u>
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

Note 1: These channels are not implemented on PIC18F2423/2523 devices.
2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as ‘0’

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3.

The source impedance (R_S) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor, C_{HOLD}. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**.

After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note:	When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, T_{ACQ}. This calculation is based on the application system assumptions shown in Table 2-1:

TABLE 2-1: T_{ACQ} ASSUMPTIONS

C_{HOLD}	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
V_{DD}	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system maximum)

EQUATION 2-1: ACQUISITION TIME

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$

$$= T_{AMP} + T_C + T_{COFF}$$

EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$

or

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)$$

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$

$$T_{AMP} = 0.2\ \mu s$$

$$T_{COFF} = (Temp - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, T_{COFF} = 0 ms.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4095)\ \mu s$$
$$-(25\ pF)(1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega) \ln(0.0004883)\ \mu s$$
$$1.56\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$

2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/$\overline{DONE}$ bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/$\overline{DONE}$ bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/$\overline{DONE}$ bit.

Manual acquisition time is selected when ACQT<2:0> = `000`. When the GO/$\overline{DONE}$ bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/$\overline{DONE}$ bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/$\overline{DONE}$ bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-2: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 μs
Operation	**ADCS<2:0>**	**Maximum FOSC**
2 TOSC	`000`	2.50 MHz
4 TOSC	`100`	5.00 MHz
8 TOSC	`001`	10.00 MHz
16 TOSC	`101`	20.00 MHz
32 TOSC	`010`	40.00 MHz
64 TOSC	`110`	40.00 MHz
RC[2]	`x11`	1.00 MHz[1]

Note 1: The RC source has a typical TAD time of 2.5 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

TABLE 2-3: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	**(Note 4)**
PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	**(Note 4)**
PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	**(Note 4)**
IPR1	PSPIP(1)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	**(Note 4)**
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	**(Note 4)**
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	**(Note 4)**
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	**(Note 4)**
ADRESH	A/D Result Register High Byte								**(Note 4)**
ADRESL	A/D Result Register Low Byte								**(Note 4)**
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	**(Note 4)**
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	**(Note 4)**
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	**(Note 4)**
PORTA	RA7(2)	RA6(2)	RA5	RA4	RA3	RA2	RA1	RA0	**(Note 4)**
TRISA	TRISA7(2)	TRISA6(2)	PORTA Data Direction Control Register						**(Note 4)**
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	**(Note 4)**
TRISB	PORTB Data Direction Control Register								**(Note 4)**
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								**(Note 4)**
PORTE(1)	—	—	—	—	RE3(3)	RE2	RE1	RE0	**(Note 4)**
TRISE(1)	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	**(Note 4)**
LATE(1)	—	—	—	—	—	PORTE Data Latch Register			**(Note 4)**

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These registers and/or bits are not implemented on PIC18F2423/2523 devices and are read as '0'.

2: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

3: RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

4: For these Reset values, see **Section 4.0 "Reset"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

3.0 SPECIAL FEATURES OF THE CPU

Note:	For additional details on the Configuration bits, refer to **Section 23.1 "Configuration Bits" in** the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631). Device ID information presented in this section is for the PIC18F2423/2523/4423/4523 devices only.

3.1 Device ID Registers

The Device ID registers are read-only registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1(1)	DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0	xxxx xxxx(2)
3FFFFFh	DEVID2(1)	DEV11	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	xxxx xxxx(2)

Legend: x = unknown, u = unchanged, — = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: DEVID registers are read-only and cannot be programmed by the user.

2: See Register 3-1 and Register 3-2 for DEVID1 and DEVID2 values.

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-4 **DEV<3:0>:** Device ID bits
1101 = PIC18F4423
1001 = PIC18F4523
0101 = PIC18F2423
0001 = PIC18F2523

bit 3-0 **REV<3:0>:** Revision ID bits
These bits are used to indicate the device revision.

FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

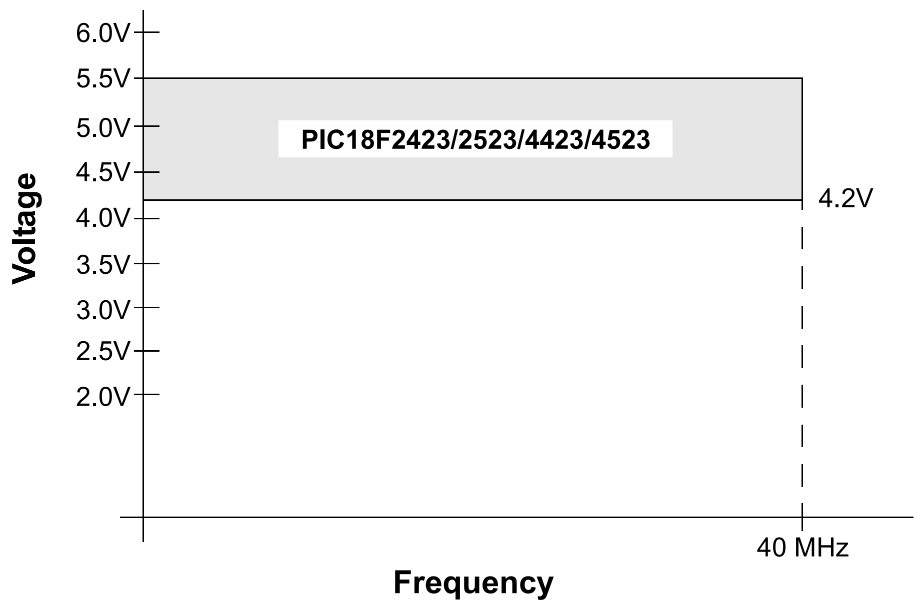
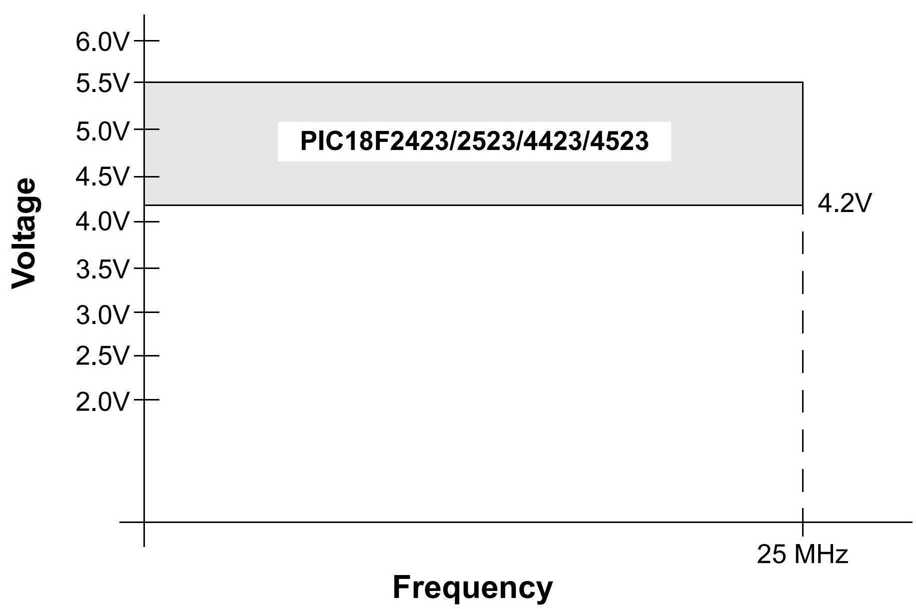


FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



APPENDIX A: REVISION HISTORY

Revision A (June 2006)

Original data sheet for PIC18F2423/2523/4423/4523 devices.

Revision B (January 2007)

This revision includes updates to the packaging diagrams.

Revision C (September 2009)

Electrical specifications updated. Preliminary condition status removed. Converted document to the “mini data sheet” format.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Program Memory (Bytes)	16384	32768	16384	32768
Program Memory (Instructions)	8192	16384	8192	16384
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC18F2423[(1)], PIC18F2523[(1)], PIC18F4423T[(2)], PIC18F4523T[(2)]; VDD range 4.2V to 5.5V PIC18F2423[(1)], PIC18F2523[(1)], PIC18F4423T[(2)], PIC18F4523T[(2)]; VDD range 2.0V to 5.5V	
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package	PT = TQFP (Thin Quad Flat pack) ML = QFN SO = SOIC SP = Skinny Plastic DIP P = PDIP	
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC18F4523-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.

b) PIC18F4523-I/PT = Industrial temp., TQFP package, Extended VDD limits.

c) PIC18F4523-E/P = Extended temp., PDIP package, normal VDD limits.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = In tape and reel PLCC, and TQFP packages only.