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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4523-i-ml

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28/40/44-Pin, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

Power Management Features:

- · Run: CPU on, Peripherals on
- · Idle: CPU off, Peripherals on
- · Sleep: CPU off, Peripherals off
- Ultra Low 50 nA Input Leakage
- Run mode Currents Down to 11 μA Typical
- Idle mode Currents Down to 2.5 μA Typical
- Sleep mode Current Down to 100 μA Typical
- · Timer1 Oscillator: 900 nA, 32 kHz, 2V
- Watchdog Timer: 1.4 μA, 2V Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- · Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL) Available for Crystal and Internal Oscillators
- · Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- · Internal Oscillator Block:
 - Fast wake from Sleep and Idle, 1 μs typical
 - 8 user-selectable frequencies, from 31 kHz to 8 MHz
 - Provides a complete range of clock speeds, from 31 kHz to 32 MHz, when used with PLL
- User-tunable to Compensate for Frequency Drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock stops

Peripheral Highlights:

- 12-Bit, Up to 13-Channel Analog-to-Digital Converter module (A/D):
 - Auto-acquisition capability
 - Conversion available during Sleep mode
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Three Programmable External Interrupts
- Four Input Change Interrupts
- Up to Two Capture/Compare/PWM (CCP) modules, One with Auto-Shutdown (28-pin devices)
- Enhanced Capture/Compare/PWM (ECCP) module (40/44-pin devices only):
 - One, two or four PWM outputs
 - Selectable polarity
 - Programmable dead time
- Auto-shutdown and auto-restart

Peripheral Highlights (Continued):

- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all four modes) and I²C™ Master and Slave modes
- · Enhanced USART module:
 - Support for RS-485, RS-232 and LIN/J2602
 - RS-232 operation using internal oscillator block (no external crystal required)
 - Auto-wake-up on Start bit
 - Auto-Baud Detect (ABD)

Special Microcontroller Features:

- C Compiler Optimized Architecture: Optional Extended Instruction Set Designed to Optimize Re-Entrant Code
- 100,000 Erase/Write Cycle, Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle, Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- · Self-Programmable under Software Control
- · Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT): Programmable Period, from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- · In-Circuit Debug (ICD) via Two Pins
- Operating Voltage Range: 2.0V to 5.5V
- Programmable, 16-Level High/Low-Voltage Detection (HLVD) module: Supports Interrupt on High/Low-Voltage Detection
- Programmable Brown-out Reset (BOR): With Software-Enable Option

Note: This document is supplemented by the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631). See Section 1.0 "Device Overview".

	Prog	ram Memory	Data Memory			40 Di4	CCP/	MSSP		RT		Timere
Device	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)	I/O	12-Bit A/D (ch)	ECCP (PWM)	SPI	Master I ² C™	EUSA	Comp.	Timers 8/16-Bit
PIC18F2423	16K	8192	768	256	25	10	2/0	Υ	Υ	1	2	1/3
PIC18F2523	32K	16384	1536	256	25	10	2/0	Υ	Υ	1	2	1/3
PIC18F4423	16K	8192	768	256	36	13	1/1	Υ	Υ	1	2	1/3
PIC18F4523	32K	16384	1536	256	36	13	1/1	Υ	Υ	1	2	1/3

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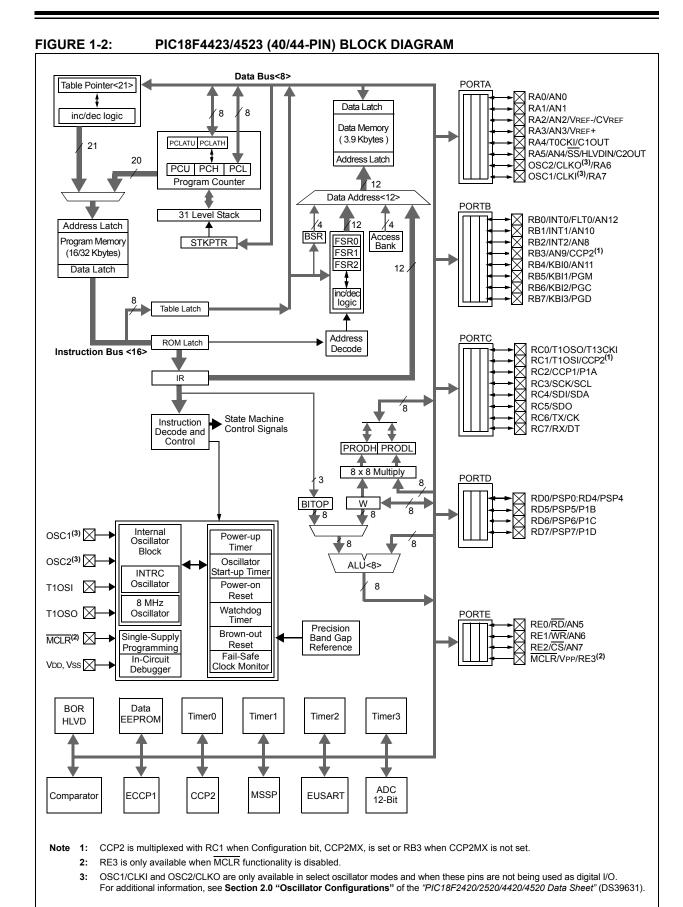


TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS

Pin Name	Piı	n Numb	er	Pin	Buffer	Description
PIII Name	PDIP	QFN	TQFP	Type	Type	Description
MCLR/VPP/RE3 MCLR	1	18	18	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				Р		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI/RA7 OSC1	13	32	30	I	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode;
CLKI				I	CMOS	analog otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7				I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6 OSC2	14	33	31	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				0	_	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

O = Output

 $I^2C = I^2C^{TM}/SMBus$

CMOS = CMOS compatible input or output

I = Input P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Piı	n Numb	er	Pin	Buffer	Description
riii ivailie	PDIP	QFN	TQFP	Type	Type	Description
						PORTC is a bidirectional I/O port.
RC0/T10S0/T13CKI RC0 T10S0 T13CKI	15	34	32	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 ⁽²⁾	16	35	35	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/P1A RC2 CCP1 P1A	17	36	36	I/O I/O O	ST ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output. Enhanced CCP1 output.
RC3/SCK/SCL RC3 SCK	18	37	37	I/O I/O	ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode.
SCL				I/O	I ² C	Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI/SDA RC4 SDI SDA	23	42	42	I/O I I/O	ST ST I ² C	Digital I/O. SPI data in. I ² C data I/O.
RC5/SDO RC5 SDO	24	43	43	I/O O	ST —	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	44	44	I/O O I/O	ST — ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see related RX/DT).
RC7/RX/DT RC7 RX DT	26	1	1	I/O I I/O	ST ST ST	Digital I/O. EUSART asynchronous receive. EUSART synchronous data (see related TX/CK).

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

s I = Input P = Power

CMOS = CMOS compatible input or output

O = Output

 $I^2C = I^2C^{TM}/SMBus$

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W ⁽¹⁾	R/W ⁽¹⁾	R/W ⁽¹⁾
_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 VCFG1: Voltage Reference Configuration bit (VREF- source)

1 = VREF- (AN2)

0 **= V**ss

bit 4 VCFG0: Voltage Reference Configuration bit (VREF+ source)

1 = VREF+ (AN3)

0 = VDD

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

PCFG<3:0>	AN12	AN11	AN10	6NA	AN8	AN7 ⁽²⁾	AN6 ⁽²⁾	AN5 ⁽²⁾	AN4	AN3	AN2	AN1	ANO
	٧	∢	٧	⋖	4	⋖	⋖	٧	٧	٧	٧	٧	٧
0000(1)	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0001	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0010	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0011	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0100	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0101	D	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0110	D	D	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α
0111(1)	D	D	D	D	D	Α	Α	Α	Α	Α	Α	Α	Α
1000	D	D	D	D	D	D	Α	Α	Α	Α	Α	Α	Α
1001	D	D	D	D	D	D	D	Α	Α	Α	Α	Α	Α
1010	D	D	D	D	D	D	D	D	Α	Α	Α	Α	Α
1011	D	D	D	D	D	D	D	D	D	Α	Α	Α	Α
1100	D	D	D	D	D	D	D	D	D	D	Α	Α	Α
1101	D	D	D	D	D	D	D	D	D	D	D	Α	Α
1110	D	D	D	D	D	D	D	D	D	D	D	D	Α
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are only available on PIC18F4423/4523 devices.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/ VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

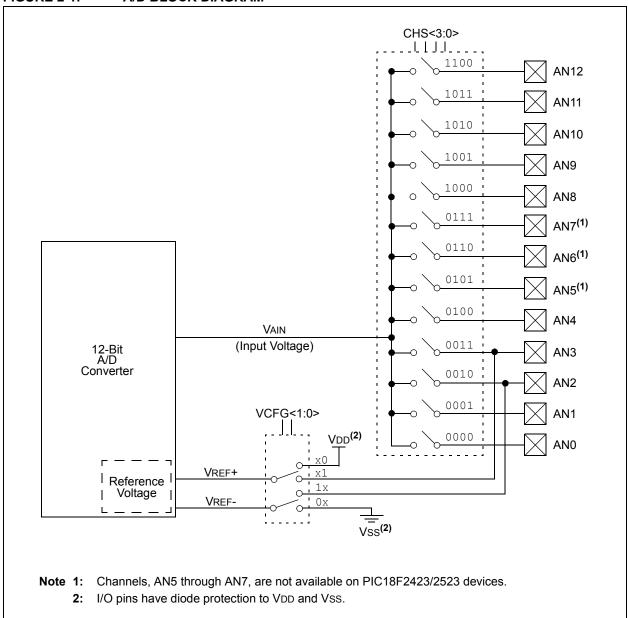
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM



The value in the ADRESH:ADRESL registers is unknown following POR and BOR Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**.

After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

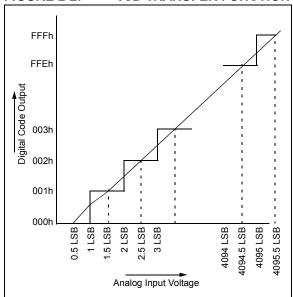
The following steps should be followed to perform an A/D conversion:

- 1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - · Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on the A/D module (ADCON0)
- 2. Configure the A/D interrupt (if desired):
 - · Clear ADIF bit
 - · Set ADIE bit
 - · Set GIE bit
- 3. Wait the required acquisition time (if required).
- 4. Start conversion by setting the GO/DONE bit (ADCON0<1>).

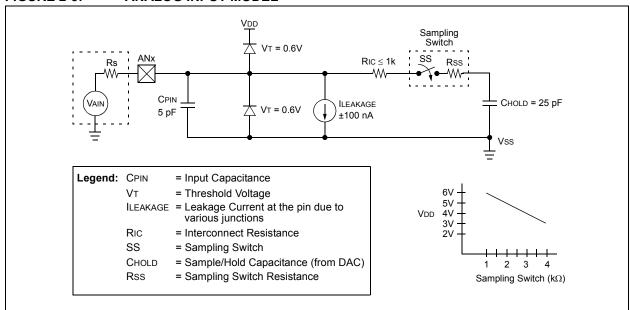
- 5. Wait for the A/D conversion to complete by either:
 - Polling for the GO/DONE bit to be cleared OR
 - · Waiting for the A/D interrupt
- Read the A/D Result registers (ADRESH:ADRESL) and clear the ADIF bit, if required.
- For the next conversion, go to step 1 or step 2, as required.

The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.









2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3.

The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 2.5 k Ω .

After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note: When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the application system assumptions shown in Table 2-1:

TABLE 2-1: TACQ ASSUMPTIONS

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
VDD	=	$3V \rightarrow Rss = 4 \text{ k}\Omega$
Temperature	=	85°C (system maximum)

EQUATION 2-1: ACQUISITION TIME

```
TACQ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient
= TAMP + TC + TCOFF
```

EQUATION 2-2: A/D MINIMUM CHARGING TIME

```
V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{(-T_{C}/C_{HOLD}(R_{IC} + R_{SS} + R_{S}))})
or
T_{C} = -(C_{HOLD})(R_{IC} + R_{SS} + R_{S}) \ln(1/4096)
```

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

```
TACQ = TAMP + TC + TCOFF

TAMP = 0.2 \,\mu s

TCOFF = (Temp - 25°C)(0.02 \,\mu s/°C)
(85^{\circ}C - 25^{\circ}C)(0.02 \,\mu s/°C)
1.2 \,\mu s

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 ms.

TC = -(CHOLD)(RIC + RSS + RS) ln(1/4095) \mu s
-(25 \,p F) (1 \,k \Omega + 4 \,k \Omega + 2.5 \,k \Omega) ln(0.0004883) \,\mu s
1.56 \,\mu s

TACQ = 0.2 \,\mu s + 1.56 \,\mu s + 1.2 \,\mu s
2.96 \,\mu s
```

2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition time is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

2 Tosc4 Tosc64 Tosc

8 Tosc
 Internal RC Oscillator

16 Tosc

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-2: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock So	urce (TAD)	Assumes TAD Min. = 0.8 μ s
Operation	ADCS<2:0>	Maximum Fosc
2 Tosc	000	2.50 MHz
4 Tosc	100	5.00 MHz
8 Tosc	001	10.00 MHz
16 Tosc	101	20.00 MHz
32 Tosc	010	40.00 MHz
64 Tosc	110	40.00 MHz
RC ⁽²⁾	x11	1.00 MHz ⁽¹⁾

Note 1: The RC source has a typical TAD time of 2.5 μ s.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

3.0 SPECIAL FEATURES OF THE CPU

Note: For additional details on the Configuration bits, refer to Section 23.1 "Configuration

Bits" in the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631). Device ID information presented in this section is for the PIC18F2423/2523/4423/4523 devices only.

3.1 Device ID Registers

The Device ID registers are read-only registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE IDs

File	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFEh	DEVID1 ⁽¹⁾	DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0	XXXX XXXX(2)
3FFFFFh	DEVID2 ⁽¹⁾	DEV11	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	×××× ××××(2)

Legend: x = unknown, u = unchanged, — = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: DEVID registers are read-only and cannot be programmed by the user.

2: See Register 3-1 and Register 3-2 for DEVID1 and DEVID2 values.

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV3	DEV2	DEV1	DEV0	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:

R = Read-only bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-4 **DEV<3:0>:** Device ID bits

1101 = PIC18F4423 1001 = PIC18F4523 0101 = PIC18F2423 0001 = PIC18F2523

bit 3-0 REV<3:0>: Revision ID bits

These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV11 ⁽¹⁾	DEV10 ⁽¹⁾	DEV9 ⁽¹⁾	DEV8 ⁽¹⁾	DEV7 ⁽¹⁾	DEV6 ⁽¹⁾	DEV5 ⁽¹⁾	DEV4 ⁽¹⁾
bit 7							bit 0

Legend:

R = Read-only bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-0 **DEV<11:4>:** Device ID bits⁽¹⁾

These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number.

0001 0001 = PIC18F2423/2523 devices 0001 0000 = PIC18F4423/4523 devices

Note 1: These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.

4.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F2423/2523/4423/4523 devices' specifications that differ from those of the PIC18F2420/2520/4420/4520 devices. For detailed information on the electrical specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

Absolute Maximum Ratings^(†)

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, liκ (VI < 0 or VI > VDD)	±20 mA
Output clamp current, loκ (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

- Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD Σ IOH} + Σ {(VDD VOH) x IOH} + Σ (VOL x IOL)
 - 2: Voltage spikes below Vss at the $\overline{\text{MCLR}/\text{VPP/RE3}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{\text{MCLR}/\text{VPP/RE3}}$ RE3 pin, rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.0 PACKAGING INFORMATION

For packaging information, see **Section 28.0 "Packaging Information"** in the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

APPENDIX A: REVISION HISTORY

Revision A (June 2006)

Original data sheet for PIC18F2423/2523/4423/4523 devices.

Revision B (January 2007)

This revision includes updates to the packaging diagrams.

Revision C (September 2009)

Electrical specifications updated. Preliminary condition status removed. Converted document to the "mini data sheet" format.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Program Memory (Bytes)	16384	32768	16384	32768
Program Memory (Instructions)	8192	16384	8192	16384
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

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