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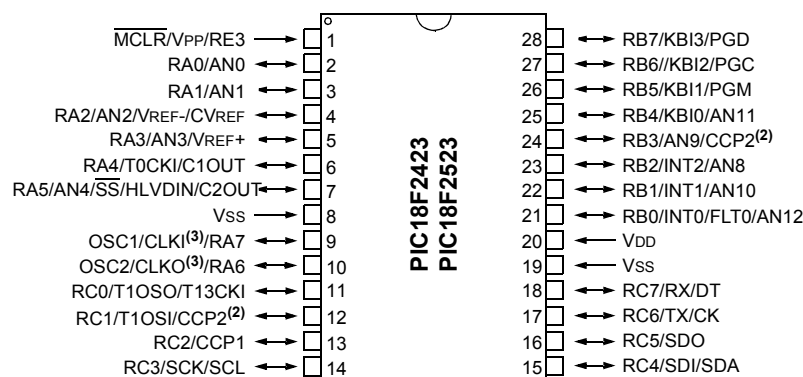
#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4523t-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4523t-i-ml</a>

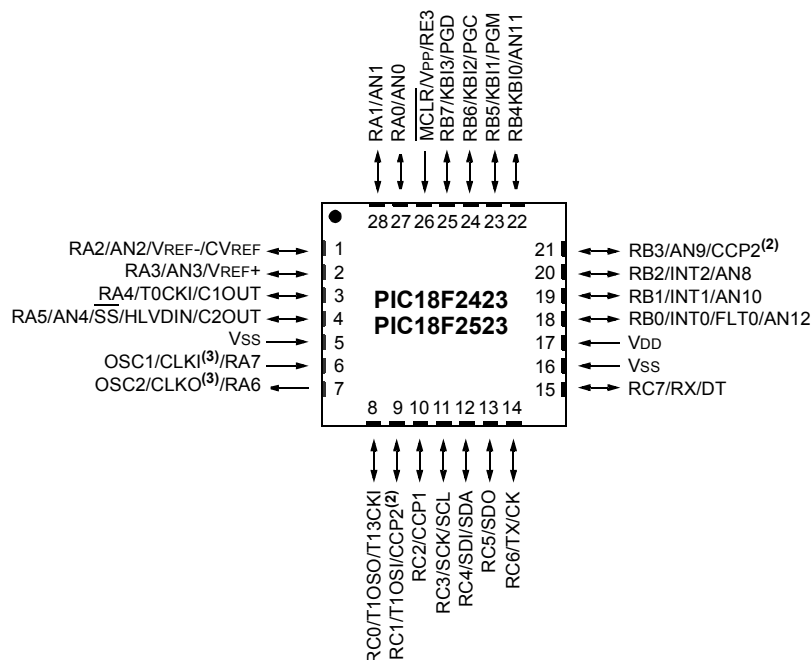
# PIC18F2423/2523/4423/4523

## Pin Diagrams

### 28-Pin PDIP, SOIC



### 28-Pin QFN<sup>(1)</sup>

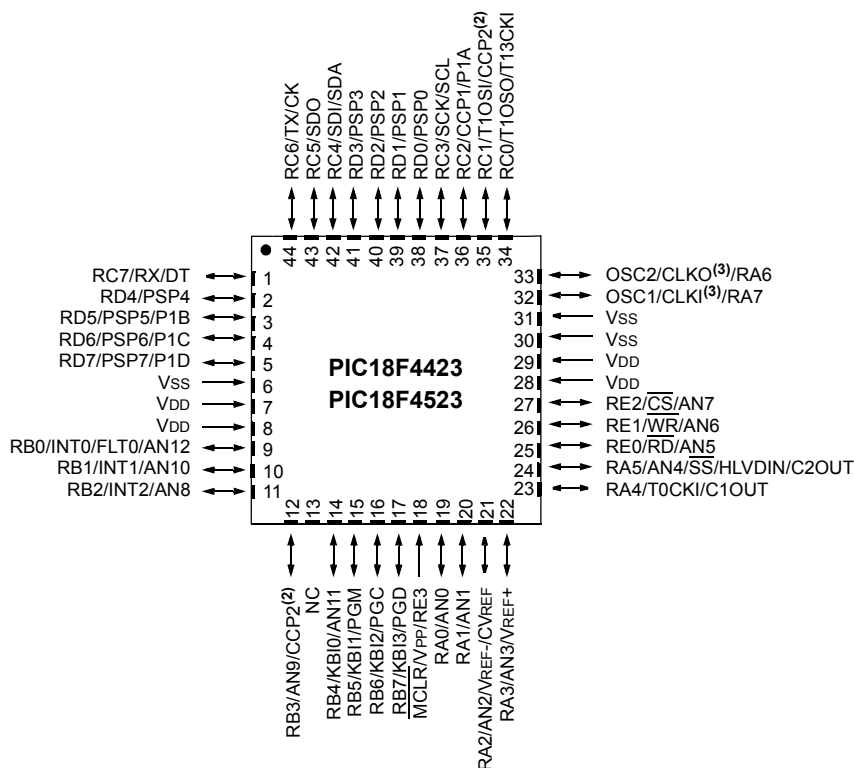


- Note**
- 1: It is recommended to connect the bottom pad of QFN package parts to Vss.
  - 2: RB3 is the alternate pin for CCP2 multiplexing.
  - 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

# PIC18F2423/2523/4423/4523

## Pin Diagrams (Continued)

### 44-Pin QFN<sup>(1)</sup>



- Note 1:** It is recommended to connect the bottom pad of QFN package parts to Vss.
- Note 2:** RB3 is the alternate pin for CCP2 multiplexing.
- Note 3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the "PIC18F2420/2520/4420/4520 Data Sheet" (DS39631).

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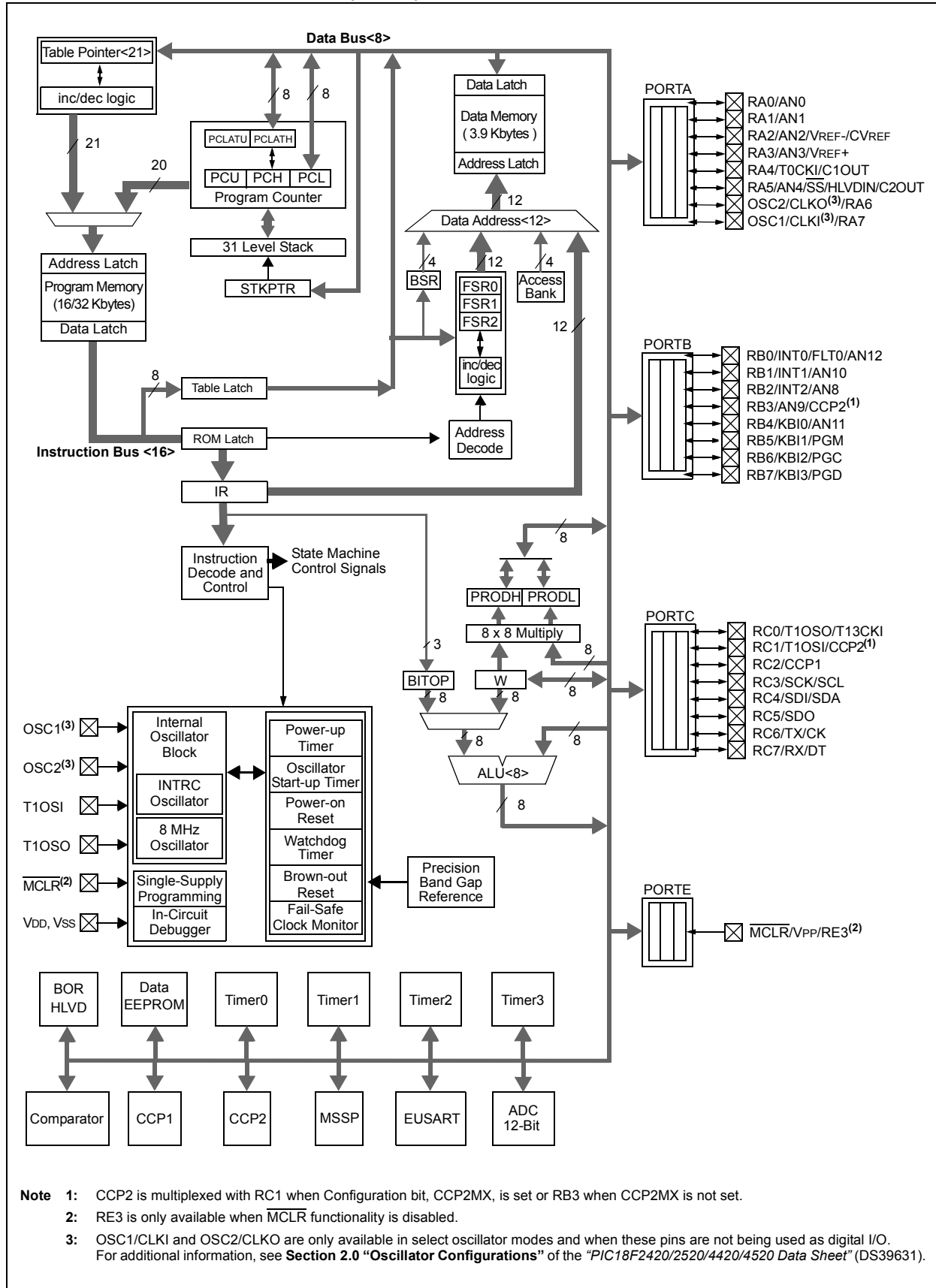
# PIC18F2423/2523/4423/4523

**TABLE 1-1: DEVICE FEATURES**

Features	PIC18F2423	PIC18F2523	PIC18F4423	PIC18F4523
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	16,384	32,768	16,384	32,768
Program Memory (Instructions)	8,192	16,384	8,192	16,384
Data Memory (Bytes)	768	1,536	768	1,536
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	28-Pin PDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin QFN 44-Pin TQFP	40-Pin PDIP 44-Pin QFN 44-Pin TQFP

# PIC18F2423/2523/4423/4523

**FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM**



# PIC18F2423/2523/4423/4523

**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
RA0/AN0	2	27	I/O	TTL	PORTA is a bidirectional I/O port.
RA0			I	Analog	Digital I/O.
AN0					Analog Input 0.
RA1/AN1	3	28	I/O	TTL	Digital I/O.
RA1			I	Analog	Analog Input 1.
AN1					
RA2/AN2/VREF-/CVREF	4	1	I/O	TTL	Digital I/O.
RA2			I	Analog	Analog Input 2.
AN2			I	Analog	A/D reference voltage (low) input.
VREF-					
CVREF			O	Analog	Comparator reference voltage output.
RA3/AN3/VREF+	5	2	I/O	TTL	Digital I/O.
RA3			I	Analog	Analog Input 3.
AN3			I	Analog	A/D reference voltage (high) input.
VREF+					
RA4/T0CKI/C1OUT	6	3	I/O	ST	Digital I/O.
RA4			I	ST	Timer0 external clock input.
T0CKI					
C1OUT			O	—	Comparator 1 output.
RA5/AN4/SS/HLVDIN/C2OUT	7	4	I/O	TTL	Digital I/O.
RA5			I	Analog	Analog Input 4.
AN4			I	TTL	SPI slave select input.
SS			I	Analog	High/Low-Voltage Detect input.
HLVDIN					
C2OUT			O	—	Comparator 2 output.
RA6					See the OSC2/CLKO/RA6 pin.
RA7					See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RA0/AN0	2	19	19	I/O	TTL	PORTA is a bidirectional I/O port.
RA0				I	Analog	Digital I/O.
AN0						Analog Input 0.
RA1/AN1	3	20	20	I/O	TTL	Digital I/O.
RA1				I	Analog	Analog Input 1.
AN1						
RA2/AN2/VREF-/CVREF	4	21	21	I/O	TTL	Digital I/O.
RA2				I	Analog	Analog Input 2.
AN2				I	Analog	A/D reference voltage (low) input.
VREF-				O	Analog	Comparator reference voltage output.
CVREF						
RA3/AN3/VREF+	5	22	22	I/O	TTL	Digital I/O.
RA3				I	Analog	Analog Input 3.
AN3				I	Analog	A/D reference voltage (high) input.
VREF+						
RA4/T0CKI/C1OUT	6	23	23	I/O	ST	Digital I/O.
RA4				I	ST	Timer0 external clock input.
T0CKI				O	—	Comparator 1 output.
C1OUT						
RA5/AN4/SS/HLVDIN/C2OUT	7	24	24	I/O	TTL	Digital I/O.
RA5				I	Analog	Analog Input 4.
AN4				I	TTL	SPI slave select input.
SS				I	Analog	High/Low-Voltage Detect input.
HLVDIN				O	—	Comparator 2 output.
C2OUT						
RA6						See the OSC2/CLKO/RA6 pin.
RA7						See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input  
ST = Schmitt Trigger input with CMOS levels  
O = Output  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus  
CMOS = CMOS compatible input or output  
I = Input  
P = Power

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled.
RD0/PSP0	19	38	38	I/O	ST	Digital I/O.
RD0				I/O	TTL	Parallel Slave Port data.
PSP0						
RD1/PSP1	20	39	39	I/O	ST	Digital I/O.
RD1				I/O	TTL	Parallel Slave Port data.
PSP1						
RD2/PSP2	21	40	40	I/O	ST	Digital I/O.
RD2				I/O	TTL	Parallel Slave Port data.
PSP2						
RD3/PSP3	22	41	41	I/O	ST	Digital I/O.
RD3				I/O	TTL	Parallel Slave Port data.
PSP3						
RD4/PSP4	27	2	2	I/O	ST	Digital I/O.
RD4				I/O	TTL	Parallel Slave Port data.
PSP4						
RD5/PSP5/P1B	28	3	3	I/O	ST	Digital I/O.
RD5				I/O	TTL	Parallel Slave Port data.
PSP5				O	—	Enhanced CCP1 output.
P1B						
RD6/PSP6/P1C	29	4	4	I/O	ST	Digital I/O.
RD6				I/O	TTL	Parallel Slave Port data.
PSP6				O	—	Enhanced CCP1 output.
P1C						
RD7/PSP7/P1D	30	5	5	I/O	ST	Digital I/O.
RD7				I/O	TTL	Parallel Slave Port data.
PSP7				O	—	Enhanced CCP1 output.
P1D						

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power  
I<sup>2</sup>C = I<sup>2</sup>C™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2423/2523/4423/4523

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NOTES:

# PIC18F2423/2523/4423/4523

## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the PIC18F2423/2523 devices and 13 for the PIC18F4423/4523 devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

Of the ADCONx registers:

- ADCON0 (shown in Register 2-1) – Controls the module's operation
- ADCON1 (Register 2-2) – Configures the functions of the port pins
- ADCON2 (Register 2-3) – Configures the A/D clock source, programmed acquisition time and justification

### REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS<3:0>:** Analog Channel Select bits

0000 = Channel 0 (AN0)  
 0001 = Channel 1 (AN1)  
 0010 = Channel 2 (AN2)  
 0011 = Channel 3 (AN3)  
 0100 = Channel 4 (AN4)  
 0101 = Channel 5 (AN5)<sup>(1,2)</sup>  
 0110 = Channel 6 (AN6)<sup>(1,2)</sup>  
 0111 = Channel 7 (AN7)<sup>(1,2)</sup>  
 1000 = Channel 8 (AN8)  
 1001 = Channel 9 (AN9)  
 1010 = Channel 10 (AN10)  
 1011 = Channel 11 (AN11)  
 1100 = Channel 12 (AN12)  
 1101 = Unimplemented<sup>(2)</sup>  
 1110 = Unimplemented<sup>(2)</sup>  
 1111 = Unimplemented<sup>(2)</sup>

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on PIC18F2423/2523 devices.

**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the  $ADCS<2:0>$  bits in  $ADCON2$  should be updated in accordance with the clock source to be used. The  $ACQT<2:0>$  bits do not need to be adjusted as the  $ADCS<2:0>$  bits adjust the  $TAD$  time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits,  $ACQT<2:0>$ , are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The  $IDLEN$  bit ( $OSCCON<7>$ ) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The  $ADCON1$ ,  $TRISA$ ,  $TRISB$  and  $TRISE$  registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding  $TRIS$  bits set (input). If the  $TRIS$  bit is cleared (output), the digital output level ( $V_{OH}$  or  $V_{OL}$ ) will be converted.

The A/D operation is independent of the state of the  $CHS<3:0>$  bits and the  $TRIS$  bits.

- Note 1:** When reading the  $PORT$  register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

**3:** The  $PBADEN$  bit in Configuration Register 3H configures  $PORTB$  pins to reset as analog or digital pins by controlling how the  $PCFG<3:0>$  bits in  $ADCON1$  are reset.

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the  $\text{ACQT}<2:0>$  bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set, the  $\text{ACQT}<2:0>$  bits have been set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means, the  $\text{ADRESH:ADRESL}$  registers will continue to contain the value of the last completed conversion (or the last value written to the  $\text{ADRESH:ADRESL}$  registers).

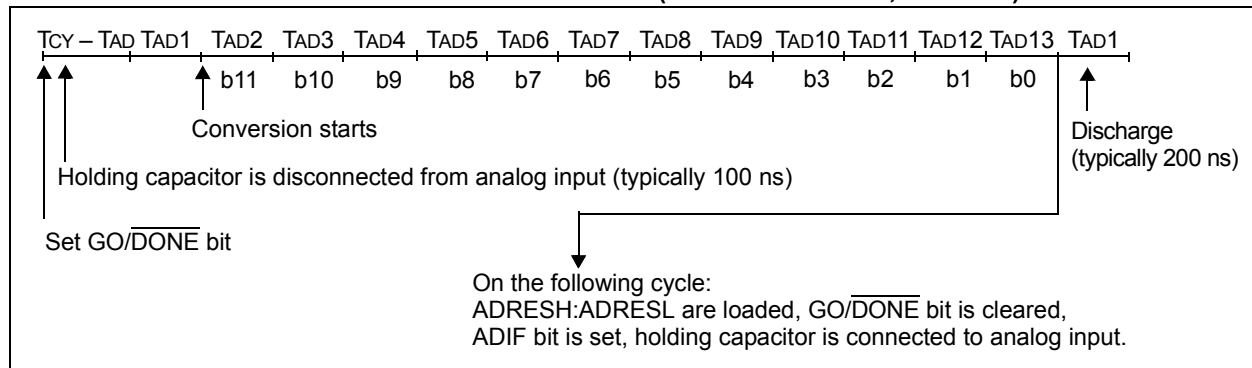
After the A/D conversion is completed or aborted, a 2  $\text{Tcy}$  wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 3 TAD after enabling the A/D before beginning an acquisition and conversion cycle.

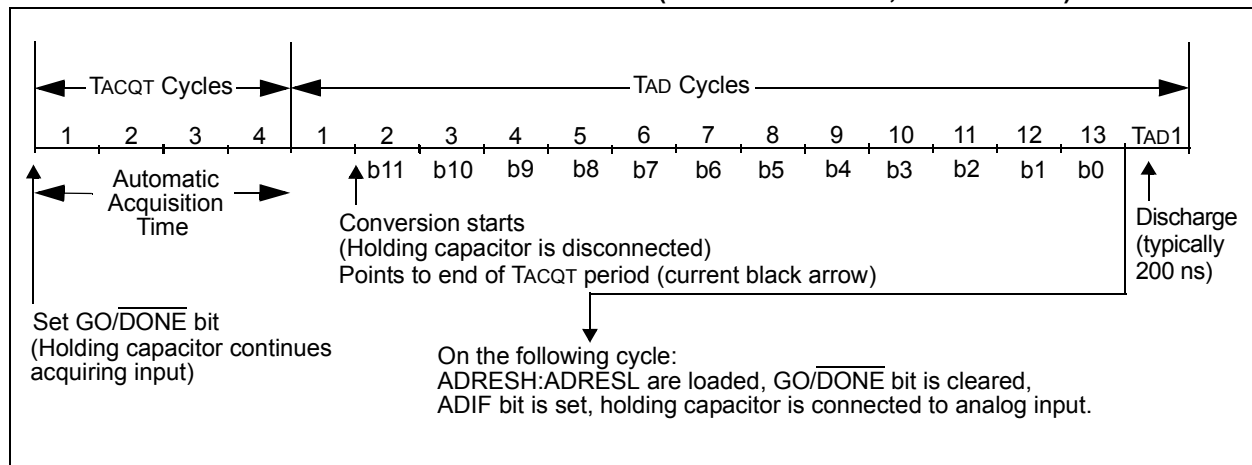
## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity-gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES ( $\text{ACQT}<2:0> = 000$ ,  $\text{Tacq} = 0$ )**



**FIGURE 2-5: A/D CONVERSION TAD CYCLES ( $\text{ACQT}<2:0> = 010$ ,  $\text{Tacq} = 4 \text{ TAD}$ )**



# PIC18F2423/2523/4423/4523

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523

R	R	R	R	R	R	R	R
DEV11 <sup>(1)</sup>	DEV10 <sup>(1)</sup>	DEV9 <sup>(1)</sup>	DEV8 <sup>(1)</sup>	DEV7 <sup>(1)</sup>	DEV6 <sup>(1)</sup>	DEV5 <sup>(1)</sup>	DEV4 <sup>(1)</sup>
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-0      **DEV<11:4>**: Device ID bits<sup>(1)</sup>

These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number.

0001 0001 = PIC18F2423/2523 devices

0001 0000 = PIC18F4423/4523 devices

**Note 1:** These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.

# PIC18F2423/2523/4423/4523

FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

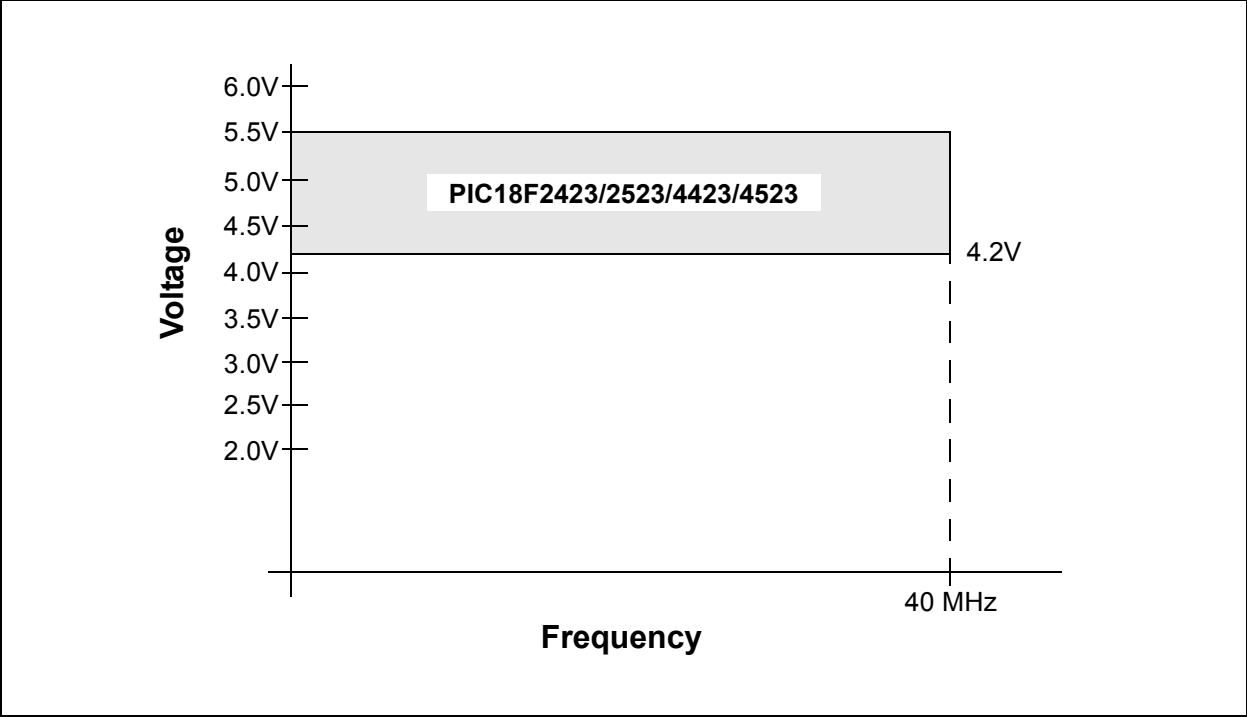
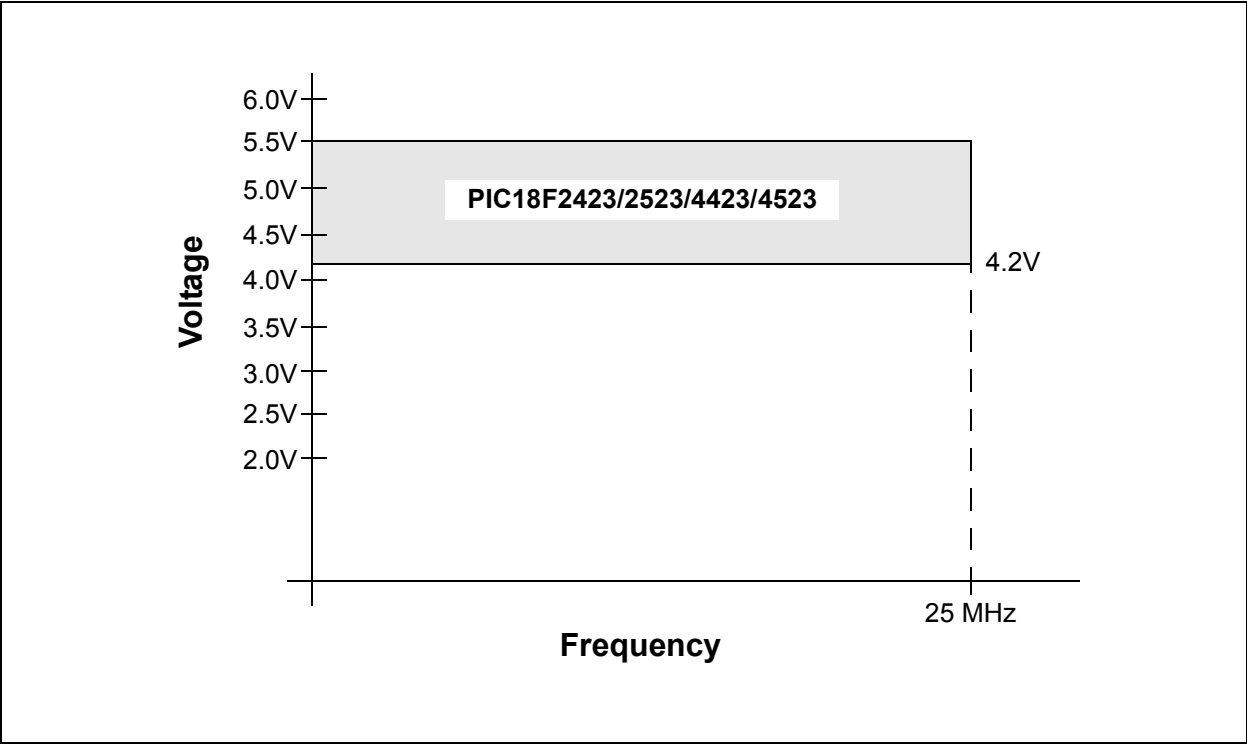
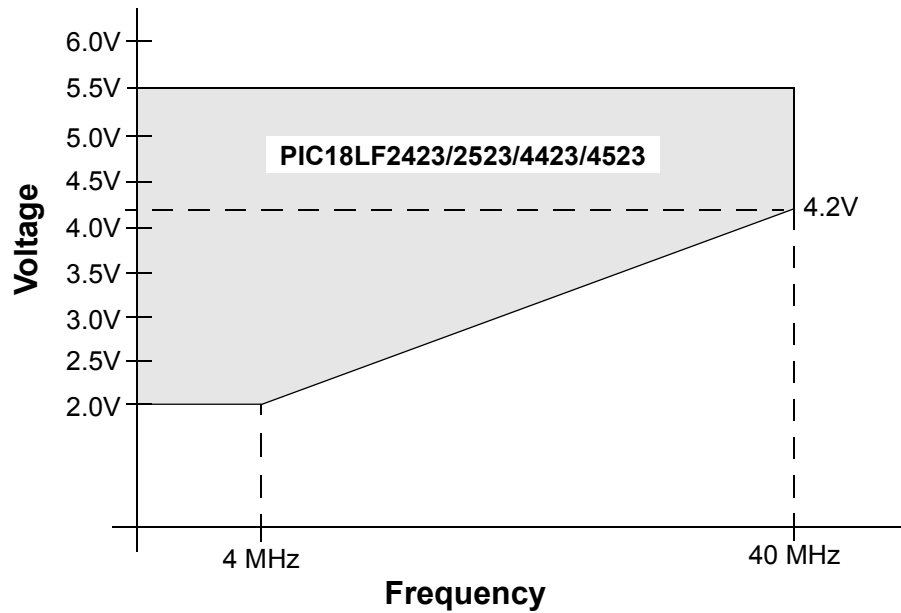


FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



# PIC18F2423/2523/4423/4523

FIGURE 4-3: PIC18LF2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

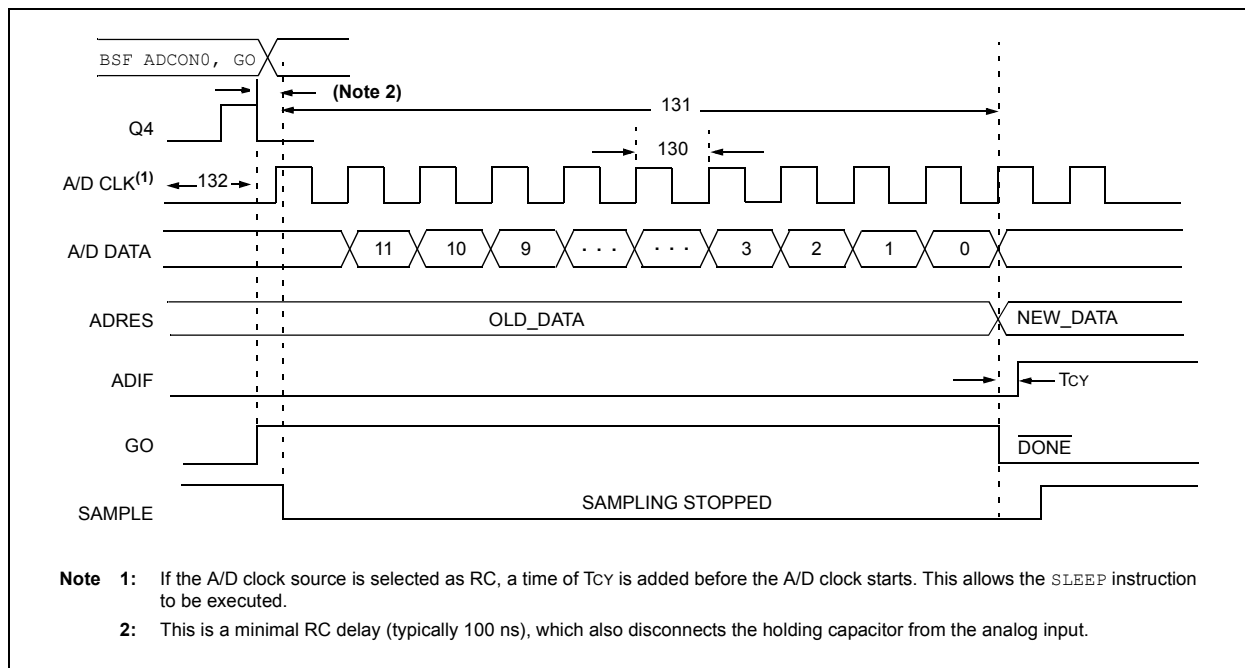


$$F_{MAX} = (16.36 \text{ MHz/V}) (V_{DDAPP\text{MIN}} - 2.0\text{V}) + 4 \text{ MHz}$$

**Note:**  $V_{DDAPP\text{MIN}}$  is the minimum voltage of the PIC<sup>®</sup> device in the application.

# PIC18F2423/2523/4423/4523

**FIGURE 4-4: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	μs	TOSC based, VREF ≥ 3.0V
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	μs	VDD = 3.0V; TOSC based, VREF full range
			PIC18FXXXX	—	1	μs	A/D RC mode
			PIC18LFXXXX	—	3	μs	VDD = 3.0V; A/D RC mode
131	TCNV	Conversion Time (not including acquisition time) <sup>(2)</sup>		13	14	TAD	
132	TACQ	Acquisition Time <sup>(3)</sup>		1.4	—	μs	
135	TSWC	Switching Time from Convert → Sample		—	(Note 4)		
137	TDIS	Discharge Time		0.2	—	μs	

**Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

**Note 2:** ADRES registers may be read on the following T<sub>cy</sub> cycle.

**Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (R<sub>s</sub>) on the input channels is 50Ω.

**Note 4:** On the following cycle of the device clock.

## 5.0 PACKAGING INFORMATION

For packaging information, see **Section 28.0 “Packaging Information”** in the *“PIC18F2420/2520/4420/4520 Data Sheet”* (DS39631).

# PIC18F2423/2523/4423/4523

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NOTES:

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**

## THE MICROCHIP WEB SITE

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- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

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**Technical support is available through the web site at: <http://support.microchip.com>**