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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	80KB (40K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2682-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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NOTES:

3.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute SLEEP. Although its value is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. The INTOSC multiplexer may be used to select a higher clock frequency, by modifying the IRCF bits, before executing the SLEEP instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value or the INTSRC bit is set, the INTOSC output is enabled. The IOFS bit becomes set, after the INTOSC output becomes stable, after an interval of TIOBST (parameter 39, Table 27-10). Clocks to the peripherals continue while the INTOSC source stabilizes. If the IRCF bits were previously at a non-zero value, or INTSRC was set before the SLEEP instruction was executed and the INTOSC source was already stable, the IOFS bit will remain set. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled, the IOFS bit will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TCSD following the wake event, the CPU begins executing code being clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

3.5 Exiting Idle and Sleep Modes

An exit from Sleep mode or any of the Idle modes is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes (see Section 3.2 "Run Modes", Section 3.3 "Sleep Mode" and Section 3.4 "Idle Modes").

3.5.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode or the Sleep mode to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCON or PIE registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/ GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see Section 9.0 "Interrupts").

A fixed delay of interval TCSD following the wake event is required when leaving the Sleep and Idle modes. This delay is required for the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

3.5.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is in when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see Section 3.2 "Run Modes" and Section 3.3 "Sleep Mode"). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see Section 24.2 "Watchdog Timer (WDT)").

The WDT timer and postscaler are cleared by executing a SLEEP or CLRWDT instruction, the loss of a currently selected clock source (if the Fail-Safe Clock Monitor is enabled) and modifying the IRCF bits in the OSCCON register if the internal oscillator block is the device clock source.

3.5.3 EXIT BY RESET

Normally, the device is held in Reset by the Oscillator Start-up Timer (OST) until the primary clock becomes ready. At that time, the OSTS bit is set and the device begins executing code. If the internal oscillator block is the new clock source, the IOFS bit is set instead.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up and the type of oscillator if the new clock source is the primary clock. Exit delays are summarized in Table 3-2.

Code execution can begin before the primary clock becomes ready. If either the Two-Speed Start-up (see **Section 24.3 "Two-Speed Start-up"**) or Fail-Safe Clock Monitor (see **Section 24.4 "Fail-Safe Clock Monitor**") is enabled, the device may begin execution as soon as the Reset source has cleared. Execution is clocked by the INTOSC multiplexer driven by the internal oscillator block. Execution is clocked by the internal oscillator block until either the primary clock becomes ready or a power-managed mode is entered before the primary clock becomes ready; the primary clock is then shut down.

5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the Program Counter (PC) is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).

A fetch cycle begins with the program counter incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 5-3: CLOCK/INSTRUCTION CYCLE

EXAMPLE 5-3: INSTRUCTION PIPELINE FLOW



5.5 Program Memory and the Extended Instruction Set

The operation of program memory is unaffected by the use of the extended instruction set.

Enabling the extended instruction set adds eight additional two-word commands to the existing PIC18 instruction set: ADDFSR, ADDULNK, CALLW, MOVSF, MOVSS, PUSHL, SUBFSR and SUBULNK. These instructions are executed as described in Section 5.2.4 "Two-Word Instructions".

5.6 Data Memory and the Extended Instruction Set

Enabling the PIC18 extended instruction set (XINST Configuration bit = 1) significantly changes certain aspects of data memory and its addressing. Specifically, the use of the Access Bank for many of the core PIC18 instructions is different. This is due to the introduction of a new addressing mode for the data memory space. This mode also alters the behavior of Indirect Addressing using FSR2 and its associated operands.

What does not change is just as important. The size of the data memory space is unchanged, as well as its linear addressing. The SFR map remains the same. Core PIC18 instructions can still operate in both Direct and Indirect Addressing mode; inherent and literal instructions do not change at all. Indirect Addressing with FSR0 and FSR1 also remains unchanged.

5.6.1 INDEXED ADDRESSING WITH LITERAL OFFSET

Enabling the PIC18 extended instruction set changes the behavior of Indirect Addressing using the FSR2 register pair and its associated file operands. Under the proper conditions, instructions that use the Access Bank – that is, most bit-oriented and byte-oriented – instructions – can invoke a form of Indexed Addressing using an offset specified in the instruction. This special addressing mode is known as Indexed Addressing with Literal Offset or Indexed Literal Offset mode. When using the extended instruction set, this addressing mode requires the following:

- The use of the Access Bank is forced ('a' = 0); and
- The file address argument is less than or equal to 5Fh.

Under these conditions, the file address of the instruction is not interpreted as the lower byte of an address (used with the BSR in Direct Addressing), or as an 8-bit address in the Access Bank. Instead, the value is interpreted as an offset value to an Address Pointer, specified by FSR2. The offset and the contents of FSR2 are added to obtain the target address of the operation.

5.6.2 INSTRUCTIONS AFFECTED BY INDEXED LITERAL OFFSET MODE

Any of the core PIC18 instructions that can use Direct Addressing are potentially affected by the Indexed Literal Offset Addressing mode. This includes all byteoriented and bit-oriented instructions, or almost one-half of the standard PIC18 instruction set. Instructions that only use Inherent or Literal Addressing modes are unaffected.

Additionally, byte-oriented and bit-oriented instructions are not affected if they use the Access Bank (Access RAM bit is '1'), or include a file address of 60h or above. Instructions meeting these criteria will continue to execute as before. A comparison of the different possible addressing modes when the extended instruction set is enabled in shown in Figure 5-8.

Those who desire to use byte-oriented or bit-oriented instructions in the Indexed Literal Offset mode should note the changes to assembler syntax for this mode. This is described in more detail in **Section 25.2.1** "Extended Instruction Syntax".

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch register (LAT) is useful for read-modifywrite operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. Pins RA6 and RA7 are multiplexed with the main oscillator pins. They are enabled as oscillator or I/O pins by the selection of the main oscillator in Configuration Register 1H (see **Section 24.1 "Configuration Bits"** for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of RA5 and RA3:RA0 pins as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note: On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE	10-1:	INITIALIZING PORTA

CLRF	PORTA	Initi	alize PORTA by
		clear	ing output
		data	latches
CLRF	LATA	Alter	nate method
		to cl	ear output
		data	latches
MOVLW	OFh	Confi	gure A/D
MOVWF	ADCON1	for d	igital inputs
MOVWF	07h	Confi	gure comparators
MOVWF	CMCON	for d	igital input
MOVLW	OCFh	Value	used to
		initi	alize data
		direc	tion
MOVWF	TRISA	Set R	A<3:0> as inputs
		RA<5:	4> as outputs

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page		
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	54		
LATC	LATC Data Output Register										
TRISC	PORTC Da	ata Directio	n Register						54		

TABLE 10-6: SUMMARY OF REGISTERS ASSOCIATE	D WITH PORTC
--	--------------

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1			
IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISE0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	t, read as '0'				
-n = Value at P	OR	'1' = Bit is se	t	'0' = Bit is cle	eared	x = Bit is unki	nown			
L:1 7			. L . L							
DIT /		mer Full Status	S DIT	to be read by						
	1 = A word has $0 = No$ word h	as been receiv	ived and waiting	to be read by	the CPU					
bit 6	OBF: Output	Buffer Full Sta	itus bit							
	1 = The outpu	ut buffer still he	olds a previous	ly written word	t					
	0 = The outpu	ut buffer has b	een read							
bit 5	IBOV: Input B	Suffer Overflow	v Detect bit (in	Microprocesso	or mode)					
	1 = A write occurred when a previously input word has not been read (must be cleared in software)									
hit 4		Dw occurred	Dort Mada Cal	at hit						
DIL 4	1 - Parallol S	Parallel Slave Port Mode Select bit								
	0 = General p	ourpose I/O m	ode							
bit 3	Unimplemen	ted: Read as	ʻ0 '							
bit 2	TRISE2: RE2	Direction Cor	ntrol bit							
	1 = Input									
	0 = Output									
bit 1	TRISE1: RE1	Direction Cor	ntrol bit							
	1 = Input									
hit 0		Direction Cor	stral bit							
DILU		Direction Col								
Dit U	1 = Input 0 = Output	Direction Cor								

REGISTER 10-1: TRISE REGISTER (PIC18F4682/4685 DEVICES ONLY)



FIGURE 15-1: CAPTURE MODE OPERATION BLOCK DIAGRAM

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation.

EQUATION 15-3:



Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	14	12	10	8	7	6.58

15.4.3 PWM AUTO-SHUTDOWN (ECCP1 ONLY)

The PWM auto-shutdown features of the Enhanced CCP1 module are available to ECCP1 in PIC18F4682/ 4685 (40/44-pin) devices. The operation of this feature is discussed in detail in **Section 16.4.7 "Enhanced PWM Auto-Shutdown"**.

Auto-shutdown features are not available for CCP1.

15.4.4 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP1 module for PWM operation:

- 1. Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- 3. Make the CCP1 pin an output by clearing the appropriate TRIS bit.
- 4. Set the TMR2 prescale value, then enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

18.3.2 EUSART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either the Single Receive Enable bit, SREN (RCSTA<5>), or the Continuous Receive Enable bit, CREN (RCSTA<4>). Data is sampled on the RX pin on the falling edge of the clock.

If enable bit SREN is set, only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.

- 3. Ensure bits CREN and SREN are clear.
- 4. If interrupts are desired, set enable bit RCIE.
- 5. If 9-bit reception is desired, set bit RX9.
- 6. If a single reception is required, set bit SREN. For continuous reception, set bit CREN.
- 7. Interrupt flag bit RCIF will be set when reception is complete and an interrupt will be generated if the enable bit RCIE was set.
- 8. Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
- 9. Read the 8-bit received data by reading the RCREG register.
- 10. If any error occurred, clear the error by clearing bit CREN.
- 11. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.



TABLE 18-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51	
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	54	
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	54	
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	54	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53	
RCREG	EUSART Re	ceive Registe	r						53	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53	
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	—	WUE	ABDEN	53	
SPBRGH	EUSART Baud Rate Generator Register High Byte									
SPBRG	EUSART Ba	ud Rate Gene	erator Registe	er Low Byte					53	

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

Note 1: Reserved in PIC18F2682/2685 devices; always maintain these bits clear.

NOTES:

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
FIL3_1	FIL3_0	FIL2_1	FIL2_0	FIL1_1	FIL1_0	FIL0_1	FIL0_0
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unk	nown
bit 7-6	FIL3_1:FIL3_	0: Filter 3 Sele	ect bits 1 and	0			
	11 = No mas	k					
	10 = Filter 15						
	01 = Accepta	nce Mask 1					
hit E 4		C Filter 2 Sol	ant hits 1 and 1	0			
DII 5-4	$\mathbf{FILZ}_{1.FILZ}_{1.1} = \mathbf{No} \operatorname{max}$	_0. Filler 2 Seit		0			
	10 = Filter 15						
	01 = Accepta	nce Mask 1					
	00 = Accepta	nce Mask 0					
bit 3-2	FIL1_1:FIL1_	_0: Filter 1 Sele	ect bits 1 and	0			
	11 = No mas	k					
	10 = Filter 15	nco Mask 1					
	00 = Accepta	nce Mask 0					
bit 1-0	FIL0 1:FIL0	0: Filter 0 Sele	ect bits 1 and	0			
	11 = No mas	- k					
	10 = Filter 15	i					
	01 = Accepta	nce Mask 1					
	00 = Accepta	nce Mask 0					

REGISTER 23-48: MSEL0: MASK SELECT REGISTER 0⁽¹⁾

Note 1: This register is available in Mode 1 and 2 only.

REGISTER 24-4: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	U-0					
MCLRE	—	—	—	—	LPT1OSC	PBADEN	—					
bit 7							bit 0					
r												
Legend:												
R = Readable b	bit	P = Programr	nable bit	U = Unimpler	mented bit, read	as '0'						
-n = Value whe	n device is unp	programmed		u = Unchang	ed from progran	nmed state						
bit 7	bit 7 MCLRE: MCLR Pin Enable bit 1 = MCLR pin enabled; RE3 input pin disabled 0 = RE3 input pin enabled; MCLR disabled											
bit 6-3	Unimplemen	ted: Read as '	0'									
bit 2	LPT1OSC: Lo 1 = Timer1 co 0 = Timer1 co	ow-Power Time Infigured for lov Infigured for hig	er1 Oscillator E w-power opera gher power op	Enable bit ation eration								
bit 1 PBADEN: PORTB A/D Enable bit (Affects ADCON1 Reset state. ADCON1 controls PORTB<4:0> pin configuration.) 1 = PORTB<4:0> pins are configured as analog input channels on Reset 0 = PORTB<4:0> pins are configured as digital I/O on Reset												
bit 0	Unimplemen	ted: Read as '	0'									

REGISTER 24-5: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/P-1	R/P-0	R/P-0	R/P-0	U-0	R/P-1	U-0	R/P-1
DEBUG	XINST	BBSIZ1	BBSIZ2	—	LVP	—	STVREN
bit 7							bit 0

Legend:								
R = Readable bit P = Programmable bit		U = Unimplemented bit, read as '0'						
-n = Value whe	n device is unprogrammed	u = Unchanged from programmed state						
bit 7	DEBUG: Background Debugger Enable b	pit						
	1 = Background debugger disabled, RB60 = Background debugger enabled, RB6	and RB7 configured as general purpose I/O pins and RB7 are dedicated to In-Circuit Debug						
bit 6	XINST: Extended Instruction Set Enable I	pit						
	1 = Instruction set extension and Indexed	Addressing mode enabled						
h :	0 = Instruction set extension and indexed	Addressing mode disabled (Legacy mode)						
DIT 5	BBSIZ1: BOOT BIOCK SIZE Select Bit 1 11 = 4K words (8 Kbytes) boot block							
	10 = 4K words (8 Kbytes) boot block							
bit 4	BBSIZ2: Boot Block Size Select Bit 0							
	01 = 2K words (4 Kbytes) boot block							
	00 = 1K words (2 Kbytes) boot block							
bit 3	Unimplemented: Read as '0'							
bit 2	LVP: Single-Supply ICSP™ Enable bit							
	1 = Single-Supply ICSP enabled							
1.11 A								
bit 1	Unimplemented: Read as '0'							
bit 0	STVREN: Stack Full/Underflow Reset En	able bit						
	1 = Stack full/underflow will cause Reset	aat						
	0 = Stack full/undernow will not cause Re	Set						

24.5 Program Verification and Code Protection

The overall structure of the code protection on the PIC18 Flash devices differs significantly from other PIC devices.

The user program memory is divided into five blocks. One of these is a boot block of 2 Kbytes. The remainder of the memory is divided into four blocks on binary boundaries. Each of the five blocks has three code protection bits associated with them. They are:

- Code-Protect bit (CPn)
- Write-Protect bit (WRTn)
- · External Block Table Read bit (EBTRn)

Figure 24-5 shows the program memory organization for 80- and 96-Kbyte devices and the specific code protection bit associated with each block. The actual locations of the bits are summarized in Table 24-3.

FIGURE 24-5: CODE-PROTECTED PROGRAM MEMORY FOR PIC18F2682/2685/4682/4685

MEMORY S	IZE/DEVICE					
80 Kbytes (PIC18F2682/4682)	96 Kbytes (PIC18F2685/4685)	Address Range	Block Code Protection Controlled By:			
Boot Block	Boot Block	000000h 0007FFh	CPB, WRTB, EBTRB			
Block 0	Block 0	000800h 003FFFh	CP0, WRT0, EBTR0			
Block 1	Block 1	004000h 007FFFh	CP1, WRT1, EBTR1			
Block 2	Block 2	008000h 00BFFFh	CP2, WRT2, EBTR2			
Block 3	Block 3	00C000h 00FFFFh	CP3, WRT3, EBTR3			
Block 4	Block 4	010000h 013FFFh	CP4, WRT4, EBTR4			
Unimplemented Read '0's	Block 5	014000h 017FFFh	CP5, WRT5, EBTR5			
Unimplemented Read '0's	Unimplemented Read '0's	018000h	(Unimplemented Memory Space)			
		_1FFFFFh				

TABLE 25-2: PIC18FXXXX INSTRUCTION SET

Mnemonic,		Description	Cycles	16-Bit Instruction Word				Status Bits	Notoo	
Operands			Cycles	MSb			LSb	Affected	Notes	
BYTE-ORI	ENTED	OPERATIONS								
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1, 2	
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1, 2	
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1,2	
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	2	
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1, 2	
CPFSEQ	f, a	Compare f with WREG, skip =	1 (2 or 3)	0110	001a	ffff	ffff	None	4	
CPFSGT	f, a	Compare f with WREG, skip >	1 (2 or 3)	0110	010a	ffff	ffff	None	4	
CPFSLT	f, a	Compare f with WREG, skip <	1 (2 or 3)	0110	000a	ffff	ffff	None	1, 2	
DECF	f, d, a	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4	
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None	1, 2, 3, 4	
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100	11da	ffff	ffff	None	1, 2	
INCF	f, d, a	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4	
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None	4	
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100	10da	ffff	ffff	None	1, 2	
IORWF	f, d, a	Inclusive OR WREG with f	1 1	0001	00da	ffff	ffff	Z, N	1, 2	
MOVF	f, d, a	Move f	1	0101	00da	ffff	ffff	Z, N	1	
MOVFF	f_s, f_d	Move f _s (source) to 1st word	2	1100	ffff	ffff	ffff	None		
	5. u	f _d (destination)2nd word		1111	ffff	ffff	ffff			
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None		
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	1, 2	
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N		
RLCF	f, d, a	Rotate Left f through Carry	1	0011	01da	ffff	ffff	C, Z, N	1, 2	
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff	ffff	Z, N	,	
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	C, Z, N		
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff	Z, N		
SETF	f, a	Set f	1	0110	100a	ffff	ffff	None	1, 2	
SUBFWB	f, d, a	Subtract f from WREG with	1	0101	01da	ffff	ffff	C, DC, Z, OV, N		
		borrow								
SUBWF	f, d, a	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N	1, 2	
SUBWFB	f, d, a	Subtract WREG from f with	1	0101	10da	ffff	ffff	C, DC, Z, OV, N		
		borrow								
SWAPF	f, d, a	Swap nibbles in f	1	0011	10da	ffff	ffff	None	4	
TSTFSZ	f, a	Test f, skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None	1, 2	
XORWF	f, d, a	Exclusive OR WREG with f	1 ′	0001	10da	ffff	ffff	Z, N		

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

5: If the table write starts the write cycle to internal memory, the write will continue until terminated.

27.2 DC Characteristics:

Power-Down and Supply Current PIC18F2682/2685/4682/4685 (Industrial) PIC18LF2682/2685/4682/4685 (Industrial) (Continued)

PIC18LF2682/2685/4682/4685 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial						
PIC18F2682/2685/4682/4685 (Industrial, Extended)		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$						
Param No.	Тур	Max	Units		Conditi	ons		
	Supply Current (IDD) ^(2,3)							
	All devices	9.00	18.00	mA	-40°C			
		8.90	17.00	mA	+25°C	VDD = 4.2V	FOSC = 4 MHZ (PRI RUN HSPLL)	
		8.80	16.00	mA	+85°C			
	All devices	12.00	24.00	mA	-40°C			
		12.00	22.00	mA	+25°C	VDD = 5.0V	(PRI RUN HSPLL)	
		12.00	21.00	mA	+85°C		(***_**********************************	
	All devices	21.00	39.00	mA	-40°C			
		21.00	39.00	mA	+25°C	VDD = 4.2V	(PRI RUN HSPLL)	
		21.00	39.00	mA	+85°C		(··· _ ·································	
	All devices	28.00	44.00	mA	-40°C			
		28.00	44.00	mA	+25°C	VDD = 5.0V		
		28.00	44.00	mA	+85°C		()	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

MCLR = VDD; WDT enabled/disabled as specified.

- **3:** For RC oscillator configurations, current through RExT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.
- 4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

27.3 DC Characteristics: PIC18F2682/2685/4682/4685 (Industrial) PIC18LF2682/2685/4682/4685 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial				
Param No.	Symbol	Characteristic	Min	Мах	Units	Conditions	
	Vol	Output Low Voltage					
D080		I/O ports	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C	
D083		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C	
	Vон	Output High Voltage ⁽³⁾					
D090		I/O ports	Vdd - 0.7	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C	
D092		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	Vdd - 0.7	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C	
		Capacitive Loading Specs on Output Pins					
D100 ⁽⁴⁾	Cosc2	OSC2 pin	_	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1	
D101	Сю	All I/O pins and OSC2 (in RC mode)	_	50	pF	To meet the AC timing specifications	
D102	Св	SCL, SDA	—	400	pF	I ² C [™] specification	

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC[®] device be driven with an external clock while in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.



TABLE 27-22: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Мах	Units	Conditions	
120	TCKH2DTV	SYNC XMIT (MASTER & SLAVE)					
		Clock High to Data Out Valid	PIC18FXXXX	_	40	ns	
			PIC18LFXXXX		100	ns	VDD = 2.0V
121	TCKRF	Clock Out Rise Time and Fall Time	PIC18FXXXX	_	20	ns	
	(Master mode)	PIC18LFXXXX	—	50	ns	VDD = 2.0V	
122	TDTRF	Data Out Rise Time and Fall Time	PIC18FXXXX	—	20	ns	
			PIC18LFXXXX		50	ns	VDD = 2.0V

FIGURE 27-21: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



TABLE 27-23: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Мах	Units	Conditions
125	TDTV2CKL	SYNC RCV (MASTER & SLAVE) Data Hold before CK \downarrow (DT hold time)	10	_	ns	
126	TCKL2DTL	Data Hold after CK \downarrow (DT hold time)	15	_	ns	

29.1 Package Marking Information (Continued)

44-Lead TQFP



Example



44-Lead QFN



Example

