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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f4685-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic18f4685-i-pt</a>

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**MICROCHIP****PIC18F2682/2685/4682/4685**

## 28/40/44-Pin Enhanced Flash Microcontrollers with ECAN™ Technology, 10-Bit A/D and nanoWatt Technology

**Power-Managed Modes:**

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8  $\mu$ A typical
- Sleep mode currents down to 0.1  $\mu$ A typical
- Timer1 Oscillator: 1.1  $\mu$ A, 32 kHz, 2V
- Watchdog Timer: 2.1  $\mu$ A
- Two-Speed Oscillator Start-up

**Flexible Oscillator Structure:**

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL) – available for crystal and internal oscillators
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds, from 31 kHz to 32 MHz when used with PLL
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripheral clock stops

**Special Microcontroller Features:**

- C compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Wide operating voltage range: 2.0V to 5.5V

**Peripheral Highlights:**

- High-Current Sink/source 25 mA/25 mA
- Three External Interrupts
- One Capture/Compare/PWM (CCP1) module
- Enhanced Capture/Compare/PWM (ECCP1) module (40/44-pin devices only):
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Master Synchronous Serial Port (MSSP) module supporting 3-Wire SPI (all 4 modes) and I<sup>2</sup>C™ Master and Slave modes
- Enhanced Addressable USART module:
  - Supports RS-485, RS-232 and LIN 1.3
  - RS-232 operation using internal oscillator block (no external crystal required)
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- 10-Bit, up to 11-Channel Analog-to-Digital Converter module (A/D), up to 100 kpsps:
  - Auto-acquisition capability
  - Conversion available during Sleep
- Dual Analog Comparators with Input Multiplexing

**ECAN Module Features:**

- Message bit rates up to 1 Mbps
- Conforms to CAN 2.0B ACTIVE Specification
- Fully Backward Compatible with PIC18XXX8 CAN modules
- Three Modes of Operation:
  - Legacy, Enhanced Legacy, FIFO
- Three Dedicated Transmit Buffers with Prioritization
- Two Dedicated Receive Buffers
- Six Programmable Receive/Transmit Buffers
- Three Full, 29-Bit Acceptance Masks
- 16 Full, 29-Bit Acceptance Filters w/Dynamic Association
- DeviceNet™ Data Byte Filter Support
- Automatic Remote Frame Handling
- Advanced Error Management Features

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP1/ ECCP1 (PWM)	MSSP		EUSART	Comp.	Timers 8/16-bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I <sup>2</sup> C™			
PIC18F2682	80K	40960	3328	1024	28	8	1/0	Y	Y	1	0	1/3
PIC18F2685	96K	49152	3328	1024	28	8	1/0	Y	Y	1	0	1/3
PIC18F4682	80K	40960	3328	1024	40/44	11	1/1	Y	Y	1	2	1/3
PIC18F4685	96K	49152	3328	1024	40/44	11	1/1	Y	Y	1	2	1/3

# PIC18F2682/2685/4682/4685

**TABLE 1-2: PIC18F2682/2685 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
RA0/AN0	2	I/O I	TTL Analog	PORTA is a bidirectional I/O port.
RA0				Digital I/O.
AN0				Analog input 0.
RA1/AN1	3	I/O I	TTL Analog	Digital I/O.
RA1				Analog input 1.
AN1				
RA2/AN2/VREF-	4	I/O I	TTL Analog Analog	Digital I/O.
RA2				Analog input 2.
AN2				A/D reference voltage (low) input.
VREF-	5	I/O I	TTL Analog Analog	Digital I/O.
RA3/AN3/VREF+				Analog input 3.
RA3				A/D reference voltage (high) input.
AN3	6	I/O I	TTL ST	Digital I/O.
VREF+				Timer0 external clock input.
RA4/T0CKI				
RA4	7	I/O I	TTL Analog TTL Analog	Digital I/O.
T0CKI				Analog input 4.
RA5/AN4/ $\overline{SS}$ /HLVDIN				SPI slave select input.
RA5				High/Low-Voltage Detect input.
AN4	6	I/O I	TTL ST	Digital I/O.
$\overline{SS}$				Timer0 external clock input.
HLVDIN				
RA6				See the OSC2/CLKO/RA6 pin.
RA7	7	I/O I	TTL Analog TTL Analog	See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power

# PIC18F2682/2685/4682/4685

**TABLE 1-2: PIC18F2682/2685 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
RB0/INT0/AN10	21			PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
AN10		I	Analog	Analog input 10.
RB1/INT1/AN8	22			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
AN8		I	Analog	Analog input 8.
RB2/INT2/CANTX	23			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
CANTX		O	TTL	CAN bus TX.
RB3/CANRX	24			
RB3		I/O	TTL	Digital I/O.
CANRX		I	TTL	CAN bus RX.
RB4/KBI0/AN9	25			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
AN9		I	Analog	Analog input 9.
RB5/KBI1/PGM	26			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	27			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

O = Output

CMOS = CMOS compatible input or output

I = Input

P = Power

## 2.0 OSCILLATOR CONFIGURATIONS

### 2.1 Oscillator Types

PIC18F2682/2685/4682/4685 devices can be operated in ten different oscillator modes. The user can program the Configuration bits, FOSC3:FOSC0, in Configuration Register 1H to select one of these ten modes:

1. LP Low-Power Crystal
2. XT Crystal/Resonator
3. HS High-Speed Crystal/Resonator
4. HSPLL High-Speed Crystal/Resonator with PLL enabled
5. RC External Resistor/Capacitor with Fosc/4 output on RA6
6. RCIO External Resistor/Capacitor with I/O on RA6
7. INTIO1 Internal Oscillator with Fosc/4 output on RA6 and I/O on RA7
8. INTIO2 Internal Oscillator with I/O on RA6 and RA7
9. EC External Clock with Fosc/4 output
10. ECIO External Clock with I/O on RA6

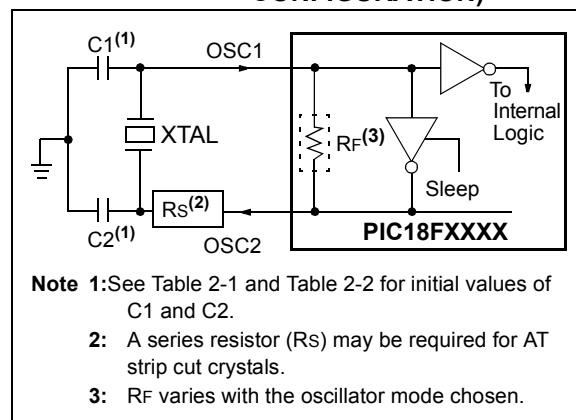
### 2.2 Crystal Oscillator/Ceramic Resonators

In XT, LP, HS or HSPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-1 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

**Note:** Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

**FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, LP, HS OR HSPLL CONFIGURATION)**



**TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS**

Typical Capacitor Values Used:			
Mode	Freq	OSC1	OSC2
XT	455 kHz	56 pF	56 pF
	2.0 MHz	47 pF	47 pF
	4.0 MHz	33 pF	33 pF
HS	8.0 MHz	27 pF	27 pF
	16.0 MHz	22 pF	22 pF

**Capacitor values are for design guidance only.**  
 These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized.**  
 Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.  
 See the notes on page 26 for additional information.

Resonators Used:	
455 kHz	4.0 MHz
2.0 MHz	8.0 MHz
16.0 MHz	

**Note:** When using resonators with frequencies above 3.5 MHz, the use of HS mode, rather than XT mode, is recommended. HS mode may be used at any VDD for which the controller is rated. If HS is selected, it is possible that the gain of the oscillator will overdrive the resonator. Therefore, a series resistor should be placed between the OSC2 pin and the resonator. As a good starting point, the recommended value of Rs is 330Ω.

## 3.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Three bits indicate the current clock source and its status. They are:

- OSTS (OSCCON<3>)
- IOFS (OSCCON<2>)
- T1RUN (T1CON<6>)

In general, only one of these bits will be set while in a given power-managed mode. When the OSTS bit is set, the primary clock is providing the device clock. When the IOFS bit is set, the INTOSC output is providing a stable 8 MHz clock source to a divider that actually drives the device clock. When the T1RUN bit is set, the Timer1 oscillator is providing the clock. If none of these bits are set, then either the INTRC clock source is clocking the device, or the INTOSC source is not yet stable.

If the internal oscillator block is configured as the primary clock source by the FOSC3:FOSC0 Configuration bits, then both the OSTS and IOFS bits may be set when in PRI\_RUN or PRI\_IDLE modes. This indicates that the primary clock (INTOSC output) is generating a stable 8 MHz output. Entering another power-managed RC mode at the same frequency would clear the OSTS bit.

- Note 1:** Caution should be used when modifying a single IRCF bit. If VDD is less than 3V, it is possible to select a higher clock speed than is supported by the low VDD. Improper device operation may result if the VDD/FOSC specifications are violated.
- 2:** Executing a `SLEEP` instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep mode or one of the Idle modes, depending on the setting of the IDLEN bit.

## 3.1.4 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the `SLEEP` instruction is determined by the setting of the IDLEN bit at the time the instruction is executed. If another `SLEEP` instruction is executed, the device will enter the power-managed mode specified by IDLEN at that time. If IDLEN has changed, the device will enter the new power-managed mode specified by the new setting.

## 3.2 Run Modes

In the Run modes, clocks to both the core and peripherals are active. The difference between these modes is the clock source.

### 3.2.1 PRI\_RUN MODE

The PRI\_RUN mode is the normal, full power execution mode of the microcontroller. This is also the default mode upon a device Reset, unless Two-Speed Start-up is enabled (see **Section 24.3 “Two-Speed Start-up”** for details). In this mode, the OSTS bit is set. The IOFS bit may be set if the internal oscillator block is the primary clock source (see **Section 2.7.1 “Oscillator Control Register”**).

### 3.2.2 SEC\_RUN MODE

The SEC\_RUN mode is the compatible mode to the “clock switching” feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high accuracy clock source.

SEC\_RUN mode is entered by setting the SCS1:SCS0 bits to ‘01’. The device clock source is switched to the Timer1 oscillator (see Figure 3-1), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

**Note:** The Timer1 oscillator should already be running prior to entering SEC\_RUN mode. If the T1OSCEN bit is not set when the SCS1:SCS0 bits are set to ‘01’, entry to SEC\_RUN mode will not occur. If the Timer1 oscillator is enabled but not yet running, device clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.

On transitions from SEC\_RUN to PRI\_RUN mode, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see Figure 3-2). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the clock. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run.

## 4.5 Device Reset Timers

PIC18F2682/2685/4682/4685 devices incorporate three separate on-chip timers that help regulate the Power-on Reset process. Their main function is to ensure that the device clock is stable before code is executed. These timers are:

- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- PLL Lock Time-out

### 4.5.1 POWER-UP TIMER (PWRT)

The Power-up Timer (PWRT) of PIC18F2682/2685/4682/4685 devices is an 11-bit counter which uses the INTRC source as the clock input. This yields an approximate time interval of  $2048 \times 32 \mu\text{s} = 65.6 \text{ ms}$ . While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC clock and will vary from chip-to-chip due to temperature and process variation. See DC parameter 33 for details.

The PWRT is enabled by clearing the  $\overline{\text{PWRTE}}\text{N}$  Configuration bit.

### 4.5.2 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (parameter 33). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP, HS and HSPLL modes and only on Power-on Reset or on exit from most power-managed modes.

### 4.5.3 PLL LOCK TIME-OUT

With the PLL enabled in its PLL mode, the time-out sequence following a Power-on Reset is slightly different from other oscillator modes. A separate timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL lock time-out ( $\text{T}_{\text{PLL}}$ ) is typically 2 ms and follows the oscillator start-up time-out.

### 4.5.4 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

1. After the POR pulse has cleared, PWRT time-out is invoked (if enabled).
2. Then, the OST is activated.

The total time-out will vary based on oscillator configuration and the status of the PWRT. Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7 all depict time-out sequences on power-up, with the Power-up Timer enabled and the device operating in HS Oscillator mode. Figures 4-3 through 4-6 also apply to devices operating in XT or LP modes. For devices in RC mode and with the PWRT disabled, on the other hand, there will be no time-out at all.

Since the time-outs occur from the POR pulse, if  $\overline{\text{MCLR}}$  is kept low long enough, all time-outs will expire. Bringing  $\overline{\text{MCLR}}$  high will begin execution immediately (Figure 4-5). This is useful for testing purposes or to synchronize more than one PIC18FXXXX device operating in parallel.

**TABLE 4-2: TIME-OUT IN VARIOUS SITUATIONS**

Oscillator Configuration	Power-up <sup>(2)</sup> and Brown-out		Exit From Power-Managed Mode
	$\overline{\text{PWRTE}}\text{N} = 0$	$\overline{\text{PWRTE}}\text{N} = 1$	
HSPLL	$66 \text{ ms}^{(1)} + 1024 \text{ T}_{\text{OSC}} + 2 \text{ ms}^{(2)}$	$1024 \text{ T}_{\text{OSC}} + 2 \text{ ms}^{(2)}$	$1024 \text{ T}_{\text{OSC}} + 2 \text{ ms}^{(2)}$
HS, XT, LP	$66 \text{ ms}^{(1)} + 1024 \text{ T}_{\text{OSC}}$	$1024 \text{ T}_{\text{OSC}}$	$1024 \text{ T}_{\text{OSC}}$
EC, ECIO	$66 \text{ ms}^{(1)}$	—	—
RC, RCIO	$66 \text{ ms}^{(1)}$	—	—
INTIO1, INTIO2	$66 \text{ ms}^{(1)}$	—	—

**Note 1:** 66 ms (65.5 ms) is the nominal Power-up Timer (PWRT) delay.

**Note 2:** 2 ms is the nominal time required for the PLL to lock.



# PIC18F2682/2685/4682/4685

**TABLE 5-2: REGISTER FILE SUMMARY (PIC18F2682/2685/4682/4685) (CONTINUED)**

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
RXF1SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xxx- x-xx	58, 305
RXF1SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	58, 306
RXF0EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	58, 306
RXF0EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	58, 306
RXF0SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xxx- x-xx	58, 305
RXF0SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	58, 306
B5D7 <sup>(8)</sup>	B5D77	B5D76	B5D75	B5D74	B5D73	B5D72	B5D71	B5D70	xxxx xxxx	58, 302
B5D6 <sup>(8)</sup>	B5D67	B5D66	B5D65	B5D64	B5D63	B5D62	B5D61	B5D60	xxxx xxxx	58, 302
B5D5 <sup>(8)</sup>	B5D57	B5D56	B5D55	B5D54	B5D53	B5D52	B5D51	B5D50	xxxx xxxx	58, 302
B5D4 <sup>(8)</sup>	B5D47	B5D46	B5D45	B5D44	B5D43	B5D42	B5D41	B5D40	xxxx xxxx	58, 302
B5D3 <sup>(8)</sup>	B5D37	B5D36	B5D35	B5D34	B5D33	B5D32	B5D31	B5D30	xxxx xxxx	58, 302
B5D2 <sup>(8)</sup>	B5D27	B5D26	B5D25	B5D24	B5D23	B5D22	B5D21	B5D20	xxxx xxxx	58, 302
B5D1 <sup>(8)</sup>	B5D17	B5D16	B5D15	B5D14	B5D13	B5D12	B5D11	B5D10	xxxx xxxx	58, 302
B5D0 <sup>(8)</sup>	B5D07	B5D06	B5D05	B5D04	B5D03	B5D02	B5D01	B5D00	xxxx xxxx	58, 302
B5DLC <sup>(8)</sup> Receive mode	—	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0	-xxx xxxx	58, 303
B5DLC <sup>(8)</sup> Transmit mode	—	TXRTR	—	—	DLC3	DLC2	DLC1	DLC0	-x-- xxxx	58, 304
B5EIDL <sup>(8)</sup>	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	58, 301
B5EIDH <sup>(8)</sup>	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	58, 301
B5SIDL <sup>(8)</sup> Receive mode	SID2	SID1	SID0	SRR	EXID	—	EID17	EID16	xxxx x-xx	58, 300
B5SIDL <sup>(8)</sup> Transmit mode	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxx- x-xx	58, 300
B5SIDH <sup>(8)</sup>	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx x-xx	58, 299
B5CON <sup>(8)</sup> Receive mode	RXFUL	RXM1	RXRTRRO	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	0000 0000	58, 298
B5CON <sup>(8)</sup> Transmit mode	TXBIF	TXABT	TXLARB	TXERR	TXREQ	RTREN	TXPRI1	TXPRI0	0000 0000	58, 298
B4D7 <sup>(8)</sup>	B4D77	B4D76	B4D75	B4D74	B4D73	B4D72	B4D71	B4D70	xxxx xxxx	58, 302
B4D6 <sup>(8)</sup>	B4D67	B4D66	B4D65	B4D64	B4D63	B4D62	B4D61	B4D60	xxxx xxxx	58, 302
B4D5 <sup>(8)</sup>	B4D57	B4D56	B4D55	B4D54	B4D53	B4D52	B4D51	B4D50	xxxx xxxx	58, 302
B4D4 <sup>(8)</sup>	B4D47	B4D46	B4D45	B4D44	B4D43	B4D42	B4D41	B4D40	xxxx xxxx	59, 302
B4D3 <sup>(8)</sup>	B4D37	B4D36	B4D35	B4D34	B4D33	B4D32	B4D31	B4D30	xxxx xxxx	59, 302
B4D2 <sup>(8)</sup>	B4D27	B4D26	B4D25	B4D24	B4D23	B4D22	B4D21	B4D20	xxxx xxxx	59, 302
B4D1 <sup>(8)</sup>	B4D17	B4D16	B4D15	B4D14	B4D13	B4D12	B4D11	B4D10	xxxx xxxx	59, 302
B4D0 <sup>(8)</sup>	B4D07	B4D06	B4D05	B4D04	B4D03	B4D02	B4D01	B4D00	xxxx xxxx	58, 302
B4DLC <sup>(8)</sup> Receive mode	—	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0	-xxx xxxx	58, 303
B4DLC <sup>(8)</sup> Transmit mode	—	TXRTR	—	—	DLC3	DLC2	DLC1	DLC0	-x-- xxxx	58, 304
B4EIDL <sup>(8)</sup>	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	59, 301
B4EIDH <sup>(8)</sup>	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	59, 301

**Legend:** x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

**Note 1:** Bit 21 of the PC is only available in Test mode and Serial Programming modes.

**2:** The SBOREN bit is only available when CONFIG2L<1:0> = 01; otherwise, it is disabled and reads as '0'. See **Section 4.4 “Brown-out Reset (BOR)”**.

**3:** These registers and/or bits are not implemented on PIC18F2682/2685 devices and are read as '0'. Reset values are shown for PIC18F4682/4685 devices; individual unimplemented bits should be interpreted as '—'.

**4:** The PLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See **Section 2.6.4 “PLL in INTOSC Modes”**.

**5:** The RE3 bit is only available when Master Clear Reset is disabled (CONFIG3H<7> = 0); otherwise, RE3 reads as '0'. This bit is read-only.

**6:** RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**7:** CAN bits have multiple functions depending on the selected mode of the CAN module.

**8:** This register reads all '0's until the ECAN™ technology is set up in Mode 1 or Mode 2.

**9:** These registers and/or bits are available on PIC18F4682/4685 devices only.

# PIC18F2682/2685/4682/4685

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NOTES:

# PIC18F2682/2685/4682/4685

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation.

## EQUATION 15-3:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{F_{\text{OSC}}}{F_{\text{PWM}}}\right)}{\log(2)} \text{ bits}$$

**Note:** If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

**TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz**

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	14	12	10	8	7	6.58

### 15.4.3 PWM AUTO-SHUTDOWN (ECCP1 ONLY)

The PWM auto-shutdown features of the Enhanced CCP1 module are available to ECCP1 in PIC18F4682/4685 (40/44-pin) devices. The operation of this feature is discussed in detail in **Section 16.4.7 “Enhanced PWM Auto-Shutdown”**.

Auto-shutdown features are not available for CCP1.

### 15.4.4 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP1 module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the appropriate TRIS bit.
4. Set the TMR2 prescale value, then enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

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## 17.4.5 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I<sup>2</sup>C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I<sup>2</sup>C protocol. It consists of all '0's with R/W = 0.

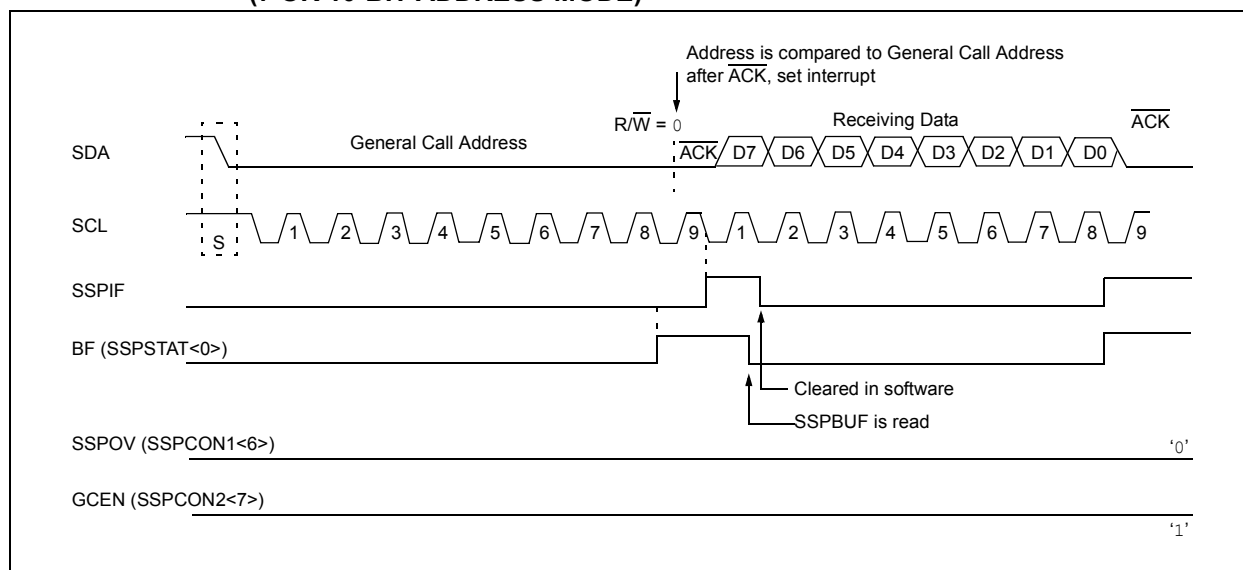
The general call address is recognized when the General Call Enable bit, GCEN, is enabled (SSPCON2<7> set). Following a Start bit detect, 8 bits are shifted into the SSPSR and the address is compared against the SSPADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag bit is set (eighth bit) and on the falling edge of the ninth bit ( $\overline{\text{ACK}}$  bit), the SSPIF interrupt flag bit is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF. The value can be used to determine if the address was device specific or a general call address.

In 10-Bit Address mode, the SSPADD is required to be updated for the second half of the address to match and the UA bit is set (SSPSTAT<1>). If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-Bit Address mode, then the second half of the address is not necessary, the UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 17-15).

**FIGURE 17-15: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7 OR 10-BIT ADDRESS MODE)**



# PIC18F2682/2685/4682/4685

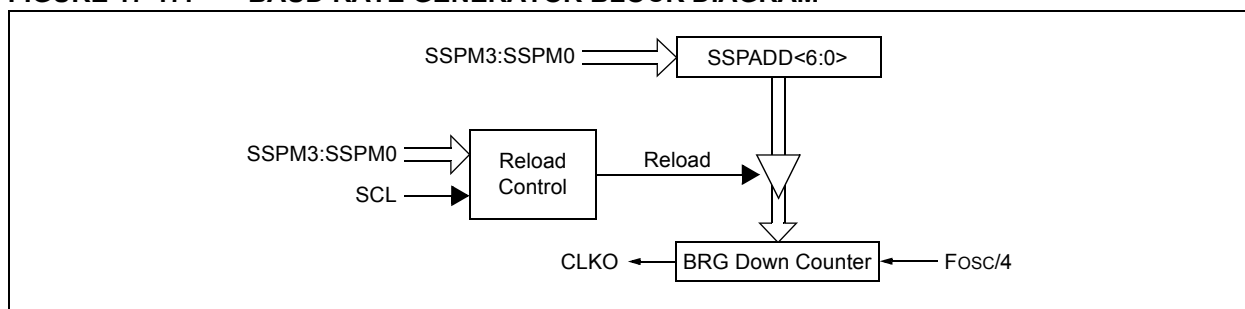
## 17.4.7 BAUD RATE

In I<sup>2</sup>C Master mode, the Baud Rate Generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 17-17). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting. The BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (T<sub>cy</sub>) on the Q2 and Q4 clocks. In I<sup>2</sup>C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 17-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

**FIGURE 17-17: BAUD RATE GENERATOR BLOCK DIAGRAM**



**TABLE 17-3: I<sup>2</sup>C™ CLOCK RATE w/BRG**

F <sub>cy</sub>	F <sub>cy</sub> *2	BRG Value	F <sub>scl</sub> (2 Rollovers of BRG)
10 MHz	20 MHz	19h	400 kHz <sup>(1)</sup>
10 MHz	20 MHz	20h	312.5 kHz
10 MHz	20 MHz	64h	100 kHz
4 MHz	8 MHz	0Ah	400 kHz <sup>(1)</sup>
4 MHz	8 MHz	0Dh	308 kHz
4 MHz	8 MHz	28h	100 kHz
1 MHz	2 MHz	03h	333 kHz <sup>(1)</sup>
1 MHz	2 MHz	0Ah	100 kHz
1 MHz	2 MHz	00h	1 MHz <sup>(1)</sup>

**Note 1:** The I<sup>2</sup>C™ interface does not conform to the 400 kHz I<sup>2</sup>C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

## 18.3 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTA<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit, SPEN (RCSTA<7>), is set in order to configure the TX and RX pins to CK (clock) and DT (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CK line. Clock polarity is selected with the SCKP bit (BAUDCON<4>); setting SCKP sets the Idle state on CK as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

### 18.3.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 18-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available).

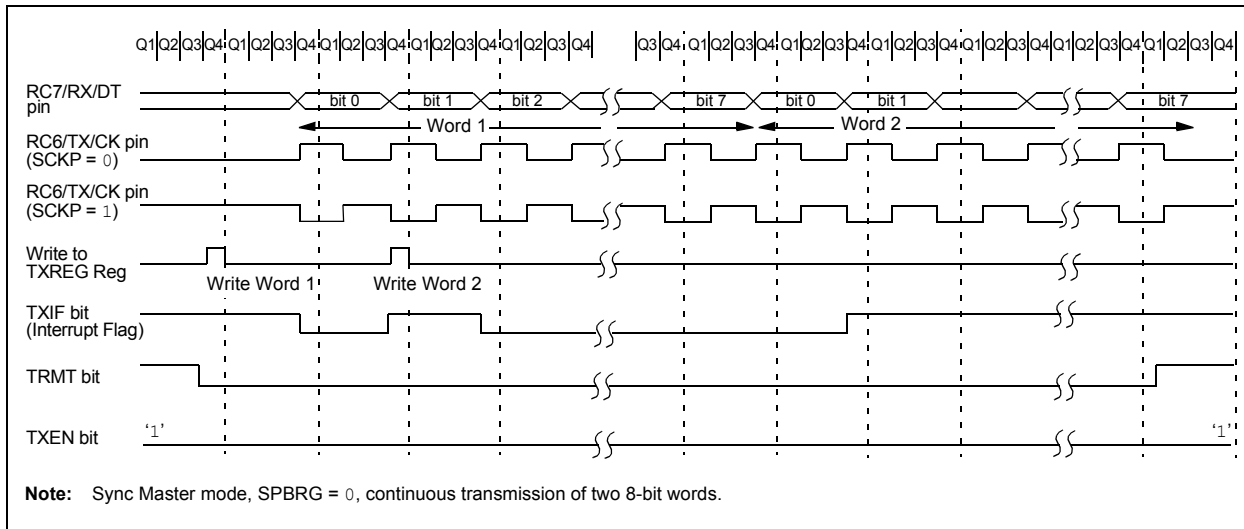
Once the TXREG register transfers the data to the TSR register (occurs in one T<sub>CYCLE</sub>), the TXREG is empty and the TXIF flag bit (PIR1<4>) is set. The interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXIE (PIE1<4>). TXIF is set regardless of the state of enable bit TXIE; it cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

To set up a Synchronous Master Transmission:

1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
2. Enable the synchronous master serial port by setting bits SYNC SPEN and CSRC.
3. If interrupts are desired, set enable bit TXIE.
4. If 9-bit transmission is desired, set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

**FIGURE 18-11: SYNCHRONOUS TRANSMISSION**



## 23.2 CAN Module Registers

**Note:** Not all CAN registers are available in the Access Bank.

There are many control and data registers associated with the CAN module. For convenience, their descriptions have been grouped into the following sections:

- Control and Status Registers
- Dedicated Transmit Buffer Registers
- Dedicated Receive Buffer Registers
- Programmable TX/RX and Auto RTR Buffers
- Baud Rate Control Registers
- I/O Control Register
- Interrupt Status and Control Registers

Detailed descriptions of each register and their usage are described in the following sections.

### 23.2.1 CAN CONTROL AND STATUS REGISTERS

The registers described in this section control the overall operation of the CAN module and show its operational status.

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## 23.2.3.2 Message Acceptance Filters and Masks

This section describes the message acceptance filters and masks for the CAN receive buffers.

### REGISTER 23-37: RXFnSIDH: RECEIVE ACCEPTANCE FILTER n STANDARD IDENTIFIER FILTER REGISTERS, HIGH BYTE [0 ≤ n ≤ 15]<sup>(1)</sup>

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0      **SID10:SID3:** Standard Identifier Filter bits (if EXIDEN = 0)  
Extended Identifier Filter bits EID28:EID21 (if EXIDEN = 1).

**Note 1:** Registers RXF6SIDH:RXF15SIDH are available in Mode 1 and 2 only.

### REGISTER 23-38: RXFnSIDL: RECEIVE ACCEPTANCE FILTER n STANDARD IDENTIFIER FILTER REGISTERS, LOW BYTE [0 ≤ n ≤ 15]<sup>(1)</sup>

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDEN <sup>(2)</sup>	—	EID17	EID16
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5      **SID2:SID0:** Standard Identifier Filter bits (if EXIDEN = 0)  
Extended Identifier Filter bits EID20:EID18 (if EXIDEN = 1).

bit 4      **Unimplemented:** Read as '0'

bit 3      **EXIDEN:** Extended Identifier Filter Enable bit<sup>(2)</sup>  
1 = Filter will only accept extended ID messages  
0 = Filter will only accept standard ID messages

bit 2      **Unimplemented:** Read as '0'

bit 1-0      **EID17:EID16:** Extended Identifier Filter bits

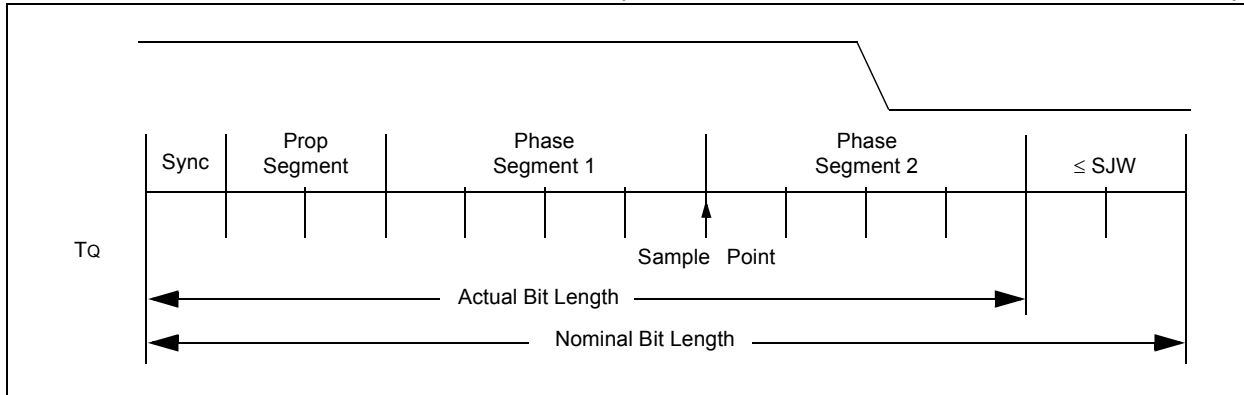
**Note 1:** Registers RXF6SIDL:RXF15SIDL are available in Mode 1 and 2 only.

**2:** In Mode 0, this bit must be set/cleared as required, irrespective of corresponding mask register value.



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**FIGURE 23-7: SHORTENING A BIT PERIOD (SUBTRACTING SJW FROM PHASE SEGMENT 2)**



## 23.11 Programming Time Segments

Some requirements for programming of the time segments:

- Prop\_Seg + Phase\_Seg 1 ≥ Phase\_Seg 2
- Phase\_Seg 2 ≥ Sync Jump Width.

For example, assume that a 125 kHz CAN baud rate is desired, using 20 MHz for FOSC. With a TOSC of 50 ns, a baud rate prescaler value of 04h gives a TQ of 500 ns. To obtain a Nominal Bit Rate of 125 kHz, the Nominal Bit Time must be 8 μs or 16 TQ.

Using 1 TQ for the Sync\_Seg, 2 TQ for the Prop\_Seg and 7 TQ for Phase Segment 1 would place the sample point at 10 TQ after the transition. This leaves 6 TQ for Phase Segment 2.

By the rules above, the Sync Jump Width could be the maximum of 4 TQ. However, normally a large SJW is only necessary when the clock generation of the different nodes is inaccurate or unstable, such as using ceramic resonators. Typically, an SJW of 1 is enough.

## 23.12 Oscillator Tolerance

As a rule of thumb, the bit timing requirements allow ceramic resonators to be used in applications with transmission rates of up to 125 Kbit/sec. For the full bus speed range of the CAN protocol, a quartz oscillator is required. A maximum node-to-node oscillator variation of 1.7% is allowed.

## 23.13 Bit Timing Configuration Registers

The Baud Rate Control registers (BRGCON1, BRGCON2, BRGCON3) control the bit timing for the CAN bus interface. These registers can only be modified when the PIC18F2682/2685/4682/4685 devices are in Configuration mode.

### 23.13.1 BRGCON1

The BRP bits control the baud rate prescaler. The SJW<1:0> bits select the synchronization jump width in terms of multiples of TQ.

### 23.13.2 BRGCON2

The PRSEG bits set the length of the propagation segment in terms of TQ. The SEG1PH bits set the length of Phase Segment 1 in TQ. The SAM bit controls how many times the RXCAN pin is sampled. Setting this bit to a '1' causes the bus to be sampled three times: twice at TQ/2 before the sample point and once at the normal sample point (which is at the end of Phase Segment 1). The value of the bus is determined to be the value read during at least two of the samples. If the SAM bit is set to a '0', then the RXCAN pin is sampled only once at the sample point. The SEG2PHTS bit controls how the length of Phase Segment 2 is determined. If this bit is set to a '1', then the length of Phase Segment 2 is determined by the SEG2PH bits of BRGCON3. If the SEG2PHTS bit is set to a '0', then the length of Phase Segment 2 is the greater of Phase Segment 1 and the Information Processing Time (which is fixed at 2 TQ for the PIC18F2682/2685/4682/4685).

### 23.13.3 BRGCON3

The PHSEG2<2:0> bits set the length (in TQ) of Phase Segment 2 if the SEG2PHTS bit is set to a '1'. If the SEG2PHTS bit is set to a '0', then the PHSEG2<2:0> bits have no effect.

# PIC18F2682/2685/4682/4685

## RETURN Return from Subroutine

**Syntax:** RETURN {s}

**Operands:**  $s \in [0,1]$

**Operation:** (TOS) → PC;  
if  $s = 1$ ,  
(WS) → W,  
(STATUS) → STATUS,  
(BSRS) → BSR,  
PCLATU, PCLATH are unchanged

**Status Affected:** None

**Encoding:**

0000	0000	0001	001s
------	------	------	------

**Description:** Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's' = 1, the contents of the shadow registers, WS, STATUS and BSRS, are loaded into their corresponding registers, W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default).

**Words:** 1

**Cycles:** 2

**Q Cycle Activity:**

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	POP PC from stack
No operation	No operation	No operation	No operation

**Example:** RETURN

After Interrupt  
PC = TOS

## RLCF Rotate Left f through Carry

**Syntax:** RLCF f{,d{,a}}

**Operands:**  $0 \leq f \leq 255$   
 $d \in [0,1]$   
 $a \in [0,1]$

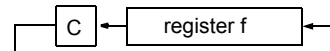
**Operation:** (f<n>) → dest<n + 1>,  
(f<7>) → C,  
(C) → dest<0>

**Status Affected:** C, N, Z

**Encoding:**

0011	01da	ffff	ffff
------	------	------	------

**Description:** The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default).  
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).  
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever  $f \leq 95$  (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

**Example:** RLCF REG, 0, 0

Before Instruction

REG = 1110 0110  
C = 0

After Instruction

REG = 1110 0110  
W = 1100 1100  
C = 1

# PIC18F2682/2685/4682/4685

**TABLE 27-1: MEMORY PROGRAMMING REQUIREMENTS**

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
<b>Internal Program Memory Programming Specifications<sup>(1)</sup></b>							
D110	VPP	Voltage on $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$ pin	9.00	—	13.25	V	<b>(Note 3)</b>
D113	IDDP	Supply Current during Programming	—	—	10	mA	
<b>Data EEPROM Memory</b>							
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C to +85°C Using EECON to read/write V <sub>MIN</sub> = Minimum operating voltage
D121	VDRW	VDD for Read/Write	V <sub>MIN</sub>	—	5.5	V	
D122	TDEW	Erase/Write Cycle Time	—	4	—	ms	Provided no other specifications are violated -40°C to +85°C
D123	TRETD	Characteristic Retention	40	—	—	Year	
D124	TREF	Number of Total Erase/Write Cycles before Refresh <sup>(2)</sup>	1M	10M	—	E/W	
<b>Program Flash Memory</b>							
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C to +85°C V <sub>MIN</sub> = Minimum operating voltage
D131	VPR	VDD for Read	V <sub>MIN</sub>	—	5.5	V	
D132	VIE	VDD for Block Erase	4.5	—	5.5	V	Using ICSP™ port
D132A	VIW	VDD for Externally Timed Erase or Write	4.5	—	5.5	V	Using ICSP port
D132B	VPEW	VDD for Self-timed Write	V <sub>MIN</sub>	—	5.5	V	V <sub>MIN</sub> = Minimum operating voltage
D133	TIE	ICSP™ Block Erase Cycle Time	—	4	—	ms	VDD > 4.5V
D133A	TIW	ICSP Erase or Write Cycle Time (externally timed)	1	—	—	ms	VDD > 4.5V
D133A	TIW	Self-timed Write Cycle Time	—	2	—	ms	
D134	TRETD	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

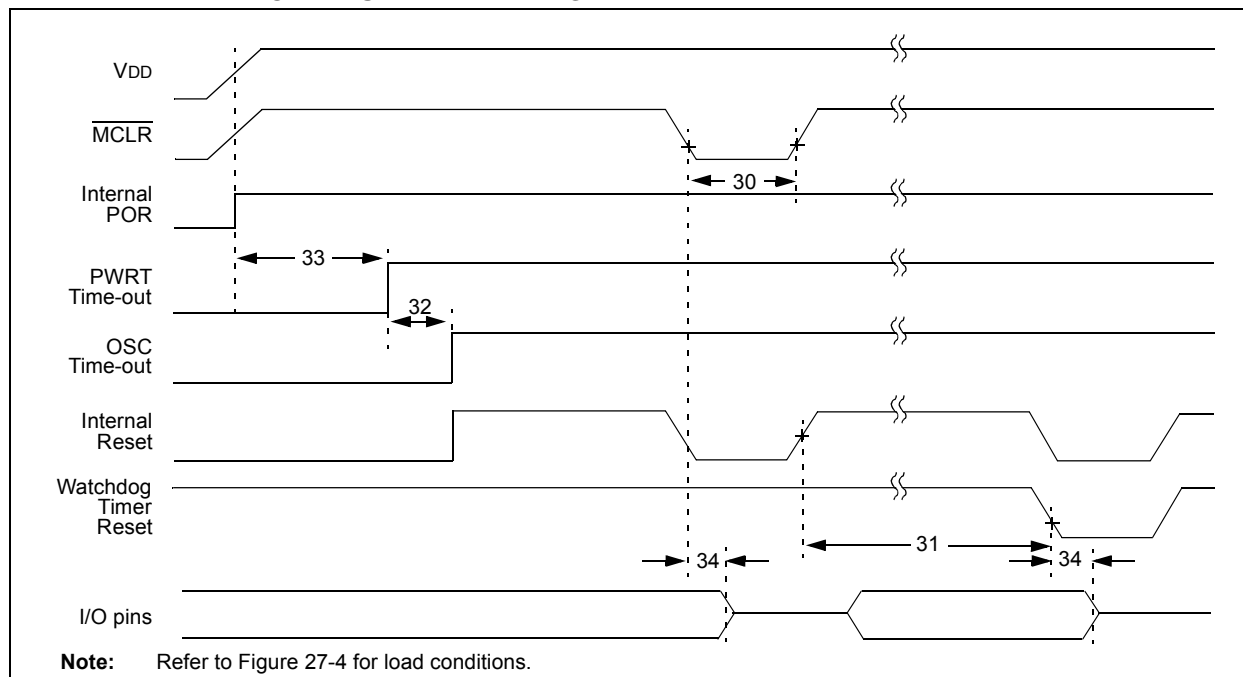
**Note 1:** These specifications are for programming the on-chip program memory through the use of table write instructions.

**2:** Refer to **Section 7.8 “Using the Data EEPROM”** for a more detailed discussion on data EEPROM endurance.

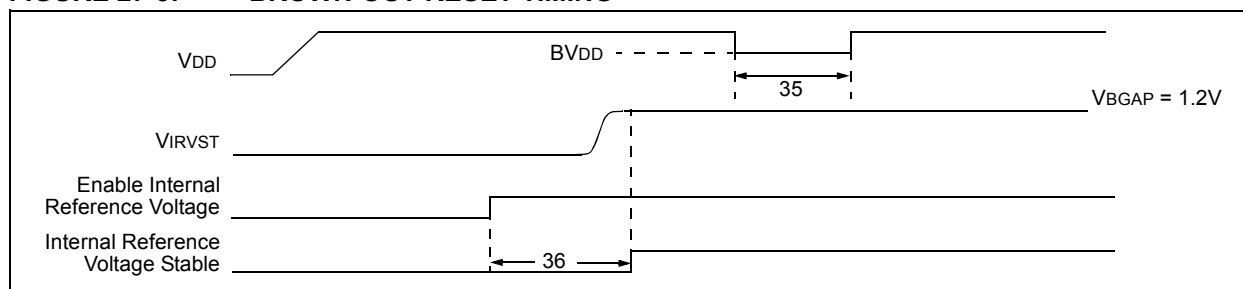
**3:** Required only if Single-Supply Programming is disabled.

# PIC18F2682/2685/4682/4685

**FIGURE 27-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**FIGURE 27-8: BROWN-OUT RESET TIMING**



**TABLE 27-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS**

Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	—	μs	
31	TWDT	Watchdog Timer Time-out Period (no postscaler)	3.4	4.00	4.6	ms	
32	TOST	Oscillation Start-up Timer Period	1024 TOSC	—	1024 TOSC	—	TOSC = OSC1 period
33	TPWRT	Power-up Timer Period	55.6	65.5	75	ms	
34	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μs	
35	TBOR	Brown-out Reset Pulse Width	200	—	—	μs	VDD ≤ BVDD (see D005)
36	TIRVST	Time for Internal Reference Voltage to become stable	—	20	50	μs	
37	TLVD	High/Low-Voltage Detect Pulse Width	200	—	—	μs	VDD ≤ VLVD
38	TCSD	CPU Start-up Time	—	10	—	μs	
39	TIOBST	Time for INTOSC to stabilize	—	1	—	μs	

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