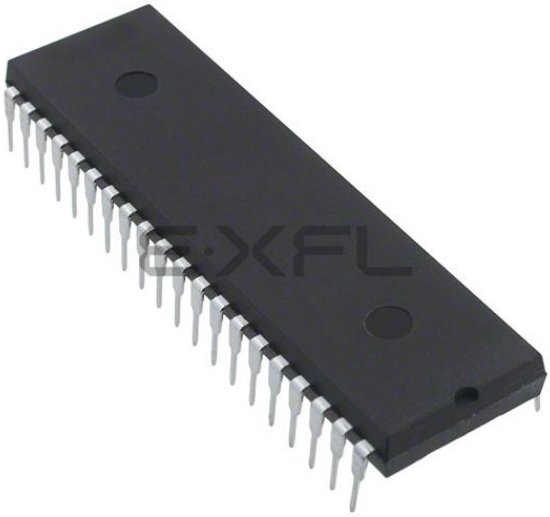

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	80KB (40K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4682-i-p

TABLE 1-2: PIC18F2682/2685 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/AN10	21			
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
AN10		I	Analog	Analog input 10.
RB1/INT1/AN8	22			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
AN8		I	Analog	Analog input 8.
RB2/INT2/CANTX	23			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
CANTX		O	TTL	CAN bus TX.
RB3/CANRX	24			
RB3		I/O	TTL	Digital I/O.
CANRX		I	TTL	CAN bus RX.
RB4/KBI0/AN9	25			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
AN9		I	Analog	Analog input 9.
RB5/KBI1/PGM	26			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	27			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

If the IRCF bits were previously at a non-zero value or if INTSRC was set before setting SCS1 and the INTOSC source was already stable, the IOFS bit will remain set.

On transitions from RC_RUN mode to PRI_RUN mode, the device continues to be clocked from the INTOSC multiplexer while the primary clock is started. When the primary clock becomes ready, a clock switch to the primary clock occurs (see Figure 3-4). When the clock switch is complete, the IOFS bit is cleared, the OSTS bit is set and the primary clock is providing the device clock. The IDLEN and SCS bits are not affected by the switch. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

FIGURE 3-3: TRANSITION TIMING TO RC_RUN MODE

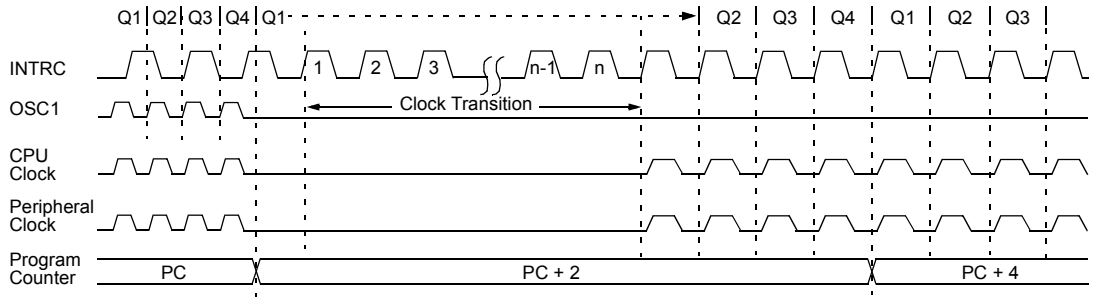
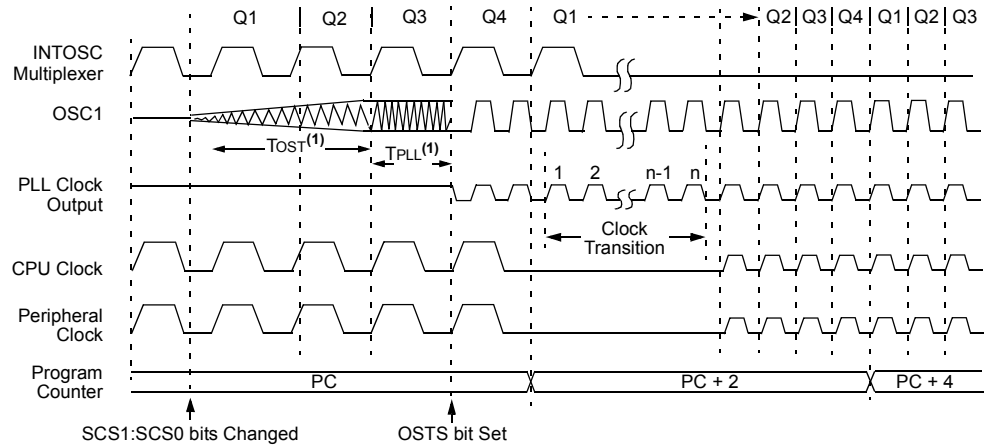


FIGURE 3-4: TRANSITION TIMING FROM RC_RUN MODE TO PRI_RUN MODE



Note 1: TOST = 1024 TOSC; TPLL = 2 ms (approx). These intervals are not shown to scale.

TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2682/2685/4682/4685 DEVICES (CONTINUED)

Address	Name	Address	Name	Address	Name	Address	Name
EFFh	—	EDFh	—	EBFh	—	E9Fh	—
EFEh	—	EDEh	—	EBEh	—	E9Eh	—
EFDh	—	EDDh	—	EBDh	—	E9Dh	—
EFCh	—	EDCh	—	EBCh	—	E9Ch	—
EFBh	—	EDBh	—	EBBh	—	E9Bh	—
EFAh	—	EDAh	—	EBAh	—	E9Ah	—
EF9h	—	ED9h	—	EB9h	—	E99h	—
EF8h	—	ED8h	—	EB8h	—	E98h	—
EF7h	—	ED7h	—	EB7h	—	E97h	—
EF6h	—	ED6h	—	EB6h	—	E96h	—
EF5h	—	ED5h	—	EB5h	—	E95h	—
EF4h	—	ED4h	—	EB4h	—	E94h	—
EF3h	—	ED3h	—	EB3h	—	E93h	—
EF2h	—	ED2h	—	EB2h	—	E92h	—
EF1h	—	ED1h	—	EB1h	—	E91h	—
EF0h	—	ED0h	—	EB0h	—	E90h	—
EEFh	—	ECFh	—	EAFh	—	E8Fh	—
EEEh	—	ECEh	—	EAEh	—	E8Eh	—
EEDh	—	ECDh	—	EADh	—	E8Dh	—
EECh	—	ECCh	—	EACh	—	E8Ch	—
EEBh	—	ECBh	—	EABh	—	E8Bh	—
EEAh	—	ECAh	—	EAAh	—	E8Ah	—
EE9h	—	EC9h	—	EA9h	—	E89h	—
EE8h	—	EC8h	—	EA8h	—	E88h	—
EE7h	—	EC7h	—	EA7h	—	E87h	—
EE6h	—	EC6h	—	EA6h	—	E86h	—
EE5h	—	EC5h	—	EA5h	—	E85h	—
EE4h	—	EC4h	—	EA4h	—	E84h	—
EE3h	—	EC3h	—	EA3h	—	E83h	—
EE2h	—	EC2h	—	EA2h	—	E82h	—
EE1h	—	EC1h	—	EA1h	—	E81h	—
EE0h	—	EC0h	—	EA0h	—	E80h	—

Note 1: Registers available only on PIC18F4X8X devices; otherwise, the registers read as '0'.
2: When any TX_ENn bit in RX_TX_SELn is set, then the corresponding bit in this register has transmit properties.
3: This is not a physical register.

TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2682/2685/4682/4685 DEVICES (CONTINUED)

Address	Name	Address	Name	Address	Name	Address	Name
DFFh	—	DDFh	—	DBFh	—	D9Fh	—
DFEh	—	DDEh	—	DBEh	—	D9Eh	—
DFDh	—	DDDh	—	DBDh	—	D9Dh	—
DFCh	TXBIE	DDCh	—	DBCh	—	D9Ch	—
DFBh	—	DDBh	—	DBBh	—	D9Bh	—
DFAh	BIE0	DDAh	—	DBAh	—	D9Ah	—
DF9h	—	DD9h	—	DB9h	—	D99h	—
DF8h	BSEL0	DD8h	SDFLC	DB8h	—	D98h	—
DF7h	—	DD7h	—	DB7h	—	D97h	—
DF6h	—	DD6h	—	DB6h	—	D96h	—
DF5h	—	DD5h	RXFCON1	DB5h	—	D95h	—
DF4h	—	DD4h	RXFCON0	DB4h	—	D94h	—
DF3h	MSEL3	DD3h	—	DB3h	—	D93h	RXF15EIDL
DF2h	MSEL2	DD2h	—	DB2h	—	D92h	RXF15EIDH
DF1h	MSEL1	DD1h	—	DB1h	—	D91h	RXF15SIDL
DF0h	MSEL0	DD0h	—	DB0h	—	D90h	RXF15SIDH
DEFh	—	DCFh	—	DAFh	—	D8Fh	—
DEEh	—	DCEh	—	DAEh	—	D8Eh	—
DEDh	—	DCDh	—	DADh	—	D8Dh	—
DECh	—	DCCh	—	DACh	—	D8Ch	—
DEBh	—	DCBh	—	DABh	—	D8Bh	RXF14EIDL
DEAh	—	DCAh	—	DAAh	—	D8Ah	RXF14EIDH
DE9h	—	DC9h	—	DA9h	—	D89h	RXF14SIDL
DE8h	—	DC8h	—	DA8h	—	D88h	RXF14SIDH
DE7h	RXFBCON7	DC7h	—	DA7h	—	D87h	RXF13EIDL
DE6h	RXFBCON6	DC6h	—	DA6h	—	D86h	RXF13EIDH
DE5h	RXFBCON5	DC5h	—	DA5h	—	D85h	RXF13SIDL
DE4h	RXFBCON4	DC4h	—	DA4h	—	D84h	RXF13SIDH
DE3h	RXFBCON3	DC3h	—	DA3h	—	D83h	RXF12EIDL
DE2h	RXFBCON2	DC2h	—	DA2h	—	D82h	RXF12EIDH
DE1h	RXFBCON1	DC1h	—	DA1h	—	D81h	RXF12SIDL
DE0h	RXFBCON0	DC0h	—	DA0h	—	D80h	RXF12SIDH

Note 1: Registers available only on PIC18F4X8X devices; otherwise, the registers read as '0'.
2: When any TX_ENn bit in RX_TX_SELn is set, then the corresponding bit in this register has transmit properties.
3: This is not a physical register.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB Data Output Register								54
TRISB	PORTB Data Direction Register								54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

TABLE 10-5: PORTC I/O SUMMARY

Pin Name	Function	I/O	TRIS	Buffer	Description
RC0/T1OSO/ T13CKI	RC0	OUT	0	DIG	LATC<0> data output.
		IN	1	ST	PORTC<0> data input.
	T1OSO	OUT	x	ANA	Timer1 oscillator output – overrides the TRIS<0> control when enabled.
	T13CKI	IN	1	ST	Timer1/Timer3 clock input.
RC1/T1OSI	RC1	OUT	0	DIG	LATC<1> data output.
		IN	1	ST	PORTC<1> data input.
	T1OSI	IN	x	ANA	Timer1 oscillator input – overrides the TRIS<1> control when enabled.
RC2/CCP1	RC2	OUT	0	DIG	LATC<2> data output.
		IN	1	ST	PORTC<2> data input.
	CCP1	OUT	0	DIG	CCP1 compare output.
		IN	1	ST	CCP1 capture input.
RC3/SCK/SCL	RC3	OUT	0	DIG	LATC<3> data output.
		IN	1	ST	PORTC<3> data input.
	SCK	OUT	0	DIG	SPI clock output (MSSP module) – must have TRIS set to '1' to allow the MSSP module to control the bidirectional communication.
		IN	1	ST	SPI clock input (MSSP module).
	SCL	OUT	0	DIG	I^2C™/SMBus clock output (MSSP module) – must have TRIS set to '1' to allow the MSSP module to control the bidirectional communication.
		IN	1	I^2C/SMB	I^2C/SMBus clock input.
RC4/SDI/SDA	RC4	OUT	0	DIG	LATC<4> data output.
		IN	1	ST	PORTC<4> data input.
	SDI	IN	1	ST	SPI data input (MSSP module).
	SDA	OUT	1	DIG	I^2C/SMBus data output (MSSP module) – must have TRIS set to '1' to allow the MSSP module to control the bidirectional communication.
		IN	1	I^2C/SMB	I^2C/SMBus data input (MSSP module) – must have TRIS set to '1' to allow the MSSP module to control the bidirectional communication.
RC5/SDO	RC5	OUT	0	DIG	LATC<5> data output.
		IN	1	ST	PORTC<5> data input.
	SDO	OUT	0	DIG	SPI data output (MSSP module).
RC6/TX/CK	RC6	OUT	0	DIG	LATC<6> data output.
		IN	1	ST	PORTC<6> data input.
	TX	OUT	0	DIG	EUSART data output.
	CK	OUT	1	DIG	EUSART synchronous clock output – must have TRIS set to '1' to enable EUSART to control the bidirectional communication.
		IN	1	ST	EUSART synchronous clock input.
RC7/RX/DT	RC7	OUT	0	DIG	LATC<7> data output.
		IN	1	ST	PORTC<7> data input.
	RX	IN	1	ST	EUSART asynchronous data input.
	DT	OUT	1	DIG	EUSART synchronous data output – must have TRIS set to '1' to enable EUSART to control the bidirectional communication.
		IN	1	ST	EUSART synchronous data input.

Legend: OUT = Output; IN = Input; ANA = Analog Signal; DIG = Digital Output; ST = Schmitt Buffer Input; TTL = TTL Buffer Input; I^2C = Inter-Integrated Circuit; SMBus = System Management Bus

TABLE 10-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTD(1)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	54
LATD(1)	LATD Data Output Register								54
TRISD(1)	PORTD Data Direction Register								54
TRISE(1)	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	54
ECCP1CON(1)	EPWM1M1	EPWM1M0	EDC1B1	EDC1B0	ECCP1M3	ECCP1M2	ECCP1M1	ECCP1M0	53

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTD.
Note 1: These registers are available on PIC18F4682/4685 devices only.

TABLE 16-3: REGISTERS ASSOCIATED WITH ECCP1 MODULE AND TIMER1 TO TIMER3

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
RCON	IPEN	SBOREN(3)	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	52
IPR1	PSPIP(2)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	54
PIR1	PSPIF(2)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	54
PIE1	PSPIE(2)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	54
IPR2	OSCFIP	CMIP(2)	—	EEIP	BCLIP	HLVDIP	TMR3IP	ECCP1IP(2)	53
PIR2	OSCFIF	CMIF(2)	—	EEIF	BCLIF	HLVDIF	TMR3IF	ECCP1IF(2)	54
PIE2	OSCFIE	CMIE(2)	—	EEIE	BCLIE	HLVDIE	TMR3IE	ECCP1IE(2)	54
TRISB	PORTB Data Direction Register								54
TRISC	PORTC Data Direction Register								54
TRISD(1)	PORTD Data Direction Register								54
TMR1L	Timer1 Register Low Byte								52
TMR1H	Timer1 Register High Byte								52
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	52
TMR2	Timer2 Register								52
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	52
PR2	Timer2 Period Register								52
TMR3L	Timer3 Register Low Byte								53
TMR3H	Timer3 Register High Byte								53
T3CON	RD16	T3ECCP1(2)	T3CKPS1	T3CKPS0	T3CCP1(2)	$\overline{T3SYNC}$	TMR3CS	TMR3ON	53
ECCPR1L(1)	Enhanced Capture/Compare/PWM Register 1 Low Byte								53
ECCPR1H(1)	Enhanced Capture/Compare/PWM Register 1 High Byte								53
ECCP1CON(1)	EPWM1M1	EPWM1M0	EDC1B1	EDC1B0	ECCP1M3	ECCP1M2	ECCP1M1	ECCP1M0	53
ECCP1AS(1)	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	53
ECCP1DEL(1)	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	53

Legend: — = unimplemented, read as '0'. Shaded cells are not used during ECCP1 operation.

Note 1: These registers are available on PIC18F4682/4685 devices only.

2: These bits are available on PIC18F4682/4685 and reserved on PIC18F2682/2685 devices.

3: The SBOREN bit is only available when CONFIG2L<1:0> = 01; otherwise, it is disabled and reads as '0'.

17.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level.

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 17-29). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 17-30.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 17-29: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

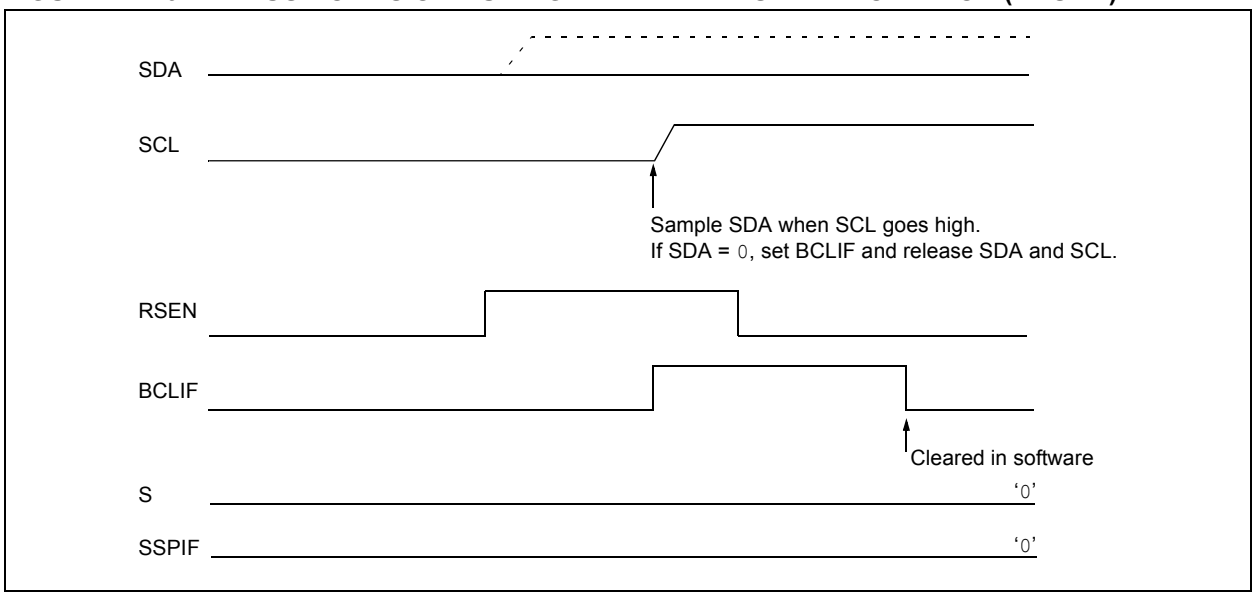
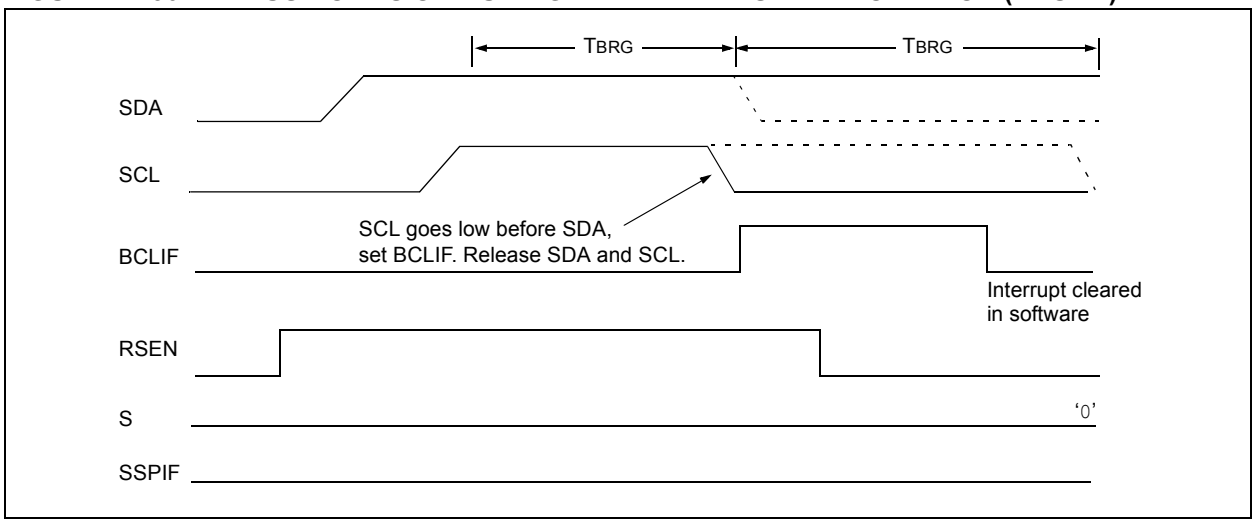


FIGURE 17-30: BUS COLLISION DURING A REPEATED START CONDITION (CASE 2)



18.0 ENHANCED UNIVERSAL SYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI.) The EUSART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers. It can also be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs and so on.

The EUSART module implements additional features, including Auto-Baud Rate Detection and calibration, automatic wake-up on Sync Break reception and 12-bit Break character transmit. These features make it ideally suited for use in Local Interconnect Network bus (LIN bus) systems.

The EUSART can be configured in the following modes:

- Asynchronous (full duplex) with:
  - Auto-Wake-up on Character Reception
  - Auto-Baud Calibration
  - 12-Bit Break Character Transmission
- Synchronous – Master (half duplex) with Selectable Clock Polarity
- Synchronous – Slave (half duplex) with Selectable Clock Polarity

The pins of the Enhanced USART are multiplexed with PORTC. In order to configure RC6/TX/CK and RC7/RX/DT as an EUSART:

- bit SPEN (RCSTA<7>) must be set (= 1)
- bit TRISC<7> must be set (= 1)
- bit TRISC<6> must be cleared (= 0) for Asynchronous and Synchronous Master modes, or set (= 1) for Synchronous Slave mode

Note:	The EUSART control will automatically reconfigure the pin from input to output as needed.

The operation of the Enhanced USART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These are detailed on the following pages in Register 18-1, Register 18-2 and Register 18-3, respectively.

19.7 Use of the ECCP1 Trigger

An A/D conversion can be started by the "Special Event Trigger" of the ECCP1 module. This requires that the ECCP1M3:ECCP1M0 bits (ECCP1CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH/ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the "Special Event Trigger" sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the "Special Event Trigger" will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

TABLE 19-2: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
IPR1	PSPIP(1)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	54
PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	54
PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	54
IPR2	OSCFIP	CMIP(1)	—	EEIP	BCLIP	HLVDIP	TMR3IP	ECCP1IP(1)	53
PIR2	OSCFIF	CMIF(1)	—	EEIF	BCLIF	HLVDIF	TMR3IF	ECCP1IF(1)	54
PIE2	OSCFIE	CMIE(1)	—	EEIE	BCLIE	HLVDIE	TMR3IE	ECCP1IE(1)	54
ADRESH	A/D Result Register High Byte								52
ADRESL	A/D Result Register Low Byte								52
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	52
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	53
PORTA	RA7(2)	RA6(2)	RA5	RA4	RA3	RA2	RA1	RA0	54
TRISA	TRISA7(2)	TRISA6(2)	PORTA Data Direction Register						54
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
TRISB	PORTB Data Direction Register								54
LATB	LATB Data Output Register								54
PORTE(4)	—	—	—	—	RE3(3)	RE2(1)	RE1(1)	RE0(1)	54
TRISE(4)	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	54
LATE(4)	—	—	—	—	—	LATE Data Output Register			54

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These bits are unimplemented on PIC18F2682/2685 devices; always maintain these bits clear.

2: These pins may be configured as port pins depending on the oscillator mode selected.

3: RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

4: These registers are not implemented on PIC18F2682/2685 devices.

NOTES:

23.7.3 ENHANCED FIFO MODE

When configured for Mode 2, two of the dedicated receive buffers in combination with one or more programmable transmit/receive buffers, are used to create a maximum of an 8-buffer deep FIFO buffer. In this mode, there is no direct correlation between filters and receive buffer registers. Any filter that has been enabled can generate an acceptance. When a message has been accepted, it is stored in the next available Receive Buffer register and an Internal Write Pointer is incremented. The FIFO can be a maximum of 8 buffers deep. The entire FIFO must consist of contiguous receive buffers. The FIFO head begins at RXB0 buffer and its tail spans toward B5. The maximum length of the FIFO is limited by the presence or absence of the first transmit buffer starting from B0. If a buffer is configured as a transmit buffer, the FIFO length is reduced accordingly. For instance, if B3 is configured as a transmit buffer, the actual FIFO will consist of RXB0, RXB1, B0, B1 and B2, a total of 5 buffers. If B0 is configured as a transmit buffer, the FIFO length will be 2. If none of the programmable buffers are configured as a transmit buffer, the FIFO will be 8 buffers deep. A system that requires more transmit buffers should try to locate transmit buffers at the very end of B0-B5 buffers to maximize available FIFO length.

When a message is received in FIFO mode, the interrupt flag code bits (EICODE<4:0>) in the CANSTAT register will have a value of '10000', indicating the FIFO has received a message. FIFO Pointer bits, FP<3:0> in the CANCON register, point to the buffer that contains data not yet read. The FIFO Pointer bits, in this sense, serve as the FIFO Read Pointer. The user should use FP bits and read corresponding buffer data. When receive data is no longer needed, the RXFUL bit in the current buffer must be cleared, causing FP<3:0> to be updated by the module.

To determine whether FIFO is empty or not, the user may use FP<3:0> bits to access the RXFUL bit in the current buffer. If RXFUL is cleared, the FIFO is considered to be empty. If it is set, the FIFO may contain one or more messages. In Mode 2, the module also provides a bit called FIFO High Water Mark (FIFOWM) in the ECANCON register. This bit can be used to cause an interrupt whenever the FIFO contains only one or four empty buffers. The FIFO high water mark interrupt can serve as an early warning to a full FIFO condition.

23.7.4 TIME-STAMPING

The CAN module can be programmed to generate a time-stamp for every message that is received. When enabled, the module generates a capture signal for CCP1, which in turn, captures the value of either Timer1 or Timer3. This value can be used as the message time-stamp.

To use the time-stamp capability, the CANCAP bit (CIOCAN<4>) must be set. This replaces the capture input for CCP1 with the signal generated from the CAN module. In addition, CCP1CON<3:0> must be set to '0011' to enable the CCP Special Event Trigger for CAN events.

23.8 Message Acceptance Filters and Masks

The message acceptance filters and masks are used to determine if a message in the Message Assembly Buffer should be loaded into any of the receive buffers. Once a valid message has been received into the MAB, the identifier fields of the message are compared to the filter values. If there is a match, that message will be loaded into the appropriate receive buffer. The filter masks are used to determine which bits in the identifier are examined with the filters. A truth table is shown below in Table 23-2 that indicates how each bit in the identifier is compared to the masks and filters to determine if a message should be loaded into a receive buffer. The mask essentially determines which bits to apply the acceptance filters to. If any mask bit is set to a zero, then that bit will automatically be accepted regardless of the filter bit.

TABLE 23-2: FILTER/MASK TRUTH TABLE

Mask bit n	Filter bit n	Message Identifier bit n001	Accept or Reject bit n
0	x	x	Accept
1	0	0	Accept
1	0	1	Reject
1	1	0	Reject
1	1	1	Accept

Legend: x = don't care

In Mode 0, acceptance filters RXF0 and RXF1 and filter mask RXM0 are associated with RXB0. Filters RXF2, RXF3, RXF4 and RXF5 and mask RXM1 are associated with RXB1.

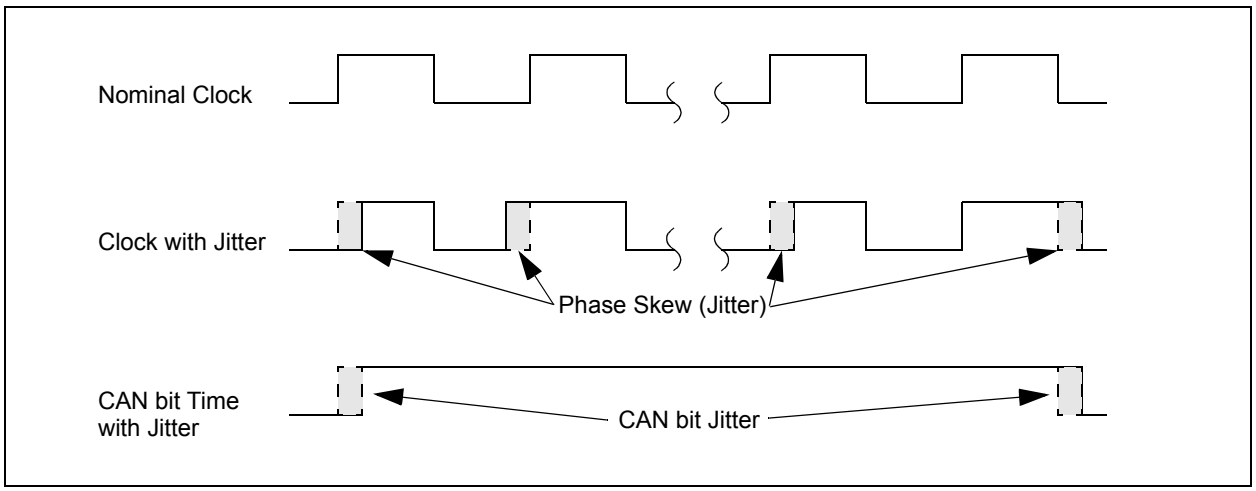
23.9.1 EXTERNAL CLOCK, INTERNAL CLOCK AND MEASURABLE JITTER IN HSPLL-BASED OSCILLATORS

The microcontroller clock frequency generated from a PLL circuit is subject to a jitter, also defined as Phase Jitter or Phase Skew. For its PIC18 Enhanced microcontrollers, Microchip specifies phase jitter (P_{jitter}) as being 2% (Gaussian distribution, within 3 standard deviations, see parameter F13 in Table 27-7) and Total Jitter (T_{jitter}) as being 2 * P_{jitter}.

The CAN protocol uses a bit-stuffing technique that inserts a bit of a given polarity following five bits with the opposite polarity. This gives a total of 10 bits transmitted without re-synchronization (compensation for jitter or phase error).

Given the random nature of the jitter error added, it can be shown that the total error caused by the jitter tends to cancel itself over time. For a period of 10 bits, it is necessary to add only two jitter intervals to correct for jitter-induced error: one interval in the beginning of the 10-bit period and another at the end. The overall effect is shown in Figure 23-5.

FIGURE 23-5: EFFECTS OF PHASE JITTER ON THE MICROCONTROLLER CLOCK AND CAN BIT TIME



Once these considerations are taken into account, it is possible to show that the relation between the jitter and the total frequency error can be defined as:

EQUATION 23-4:

$$\Delta f = \frac{T_{jitter}}{10 \times NBT} = \frac{2 \times P_{jitter}}{10 \times NBT}$$

where jitter is expressed in terms of time and NBT is the Nominal Bit Time.

For example, assume a CAN bit rate of 125 Kb/s, which gives an NBT of 8 μs. For a 16 MHz clock generated from a 4x PLL, the jitter at this clock frequency is:

EQUATION 23-5:

$$2\% \times \frac{1}{16\ MHz} = \frac{0.02}{16 \times 10^6} = 1.25ns$$

The resultant frequency error is:

EQUATION 23-6:

$$\frac{2 \times (1.25 \times 10^{-9})}{10 \times (8 \times 10^{-6})} = 3.125 \times 10^{-5} = 0.0031\%$$

24.0 SPECIAL FEATURES OF THE CPU

PIC18F2682/2685/4682/4685 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These are:

- Oscillator Selection
- Resets:
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor
- Two-Speed Start-up
- Code Protection
- ID Locations
- In-Circuit Serial Programming

The oscillator can be configured for the application depending on frequency, power, accuracy and cost. All of the options are discussed in detail in **Section 2.0 "Oscillator Configurations"**.

A complete discussion of device Resets and interrupts is available in previous sections of this data sheet.

In addition to their Power-up and Oscillator Start-up Timers provided for Resets, PIC18F2682/2685/4682/4685 devices have a Watchdog Timer, which is either permanently enabled via the Configuration bits or software controlled (if configured as disabled).

The inclusion of an internal RC oscillator also provides the additional benefits of a Fail-Safe Clock Monitor (FSCM) and Two-Speed Start-up. FSCM provides for background monitoring of the peripheral clock and automatic switchover in the event of its failure. Two-Speed Start-up enables code to be executed almost immediately on start-up, while the primary clock source completes its start-up delays.

All of these features are enabled and configured by setting the appropriate Configuration register bits.

24.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped starting at program memory location 300000h.

The user will note that address 300000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h-3FFFFFh), which can only be accessed using table reads and table writes.

Programming the Configuration registers is done in a manner similar to programming the Flash memory. The WR bit in the EECON1 register starts a self-timed write to the Configuration register. In normal operation mode, a TBLWT instruction with the TBLPTR pointing to the Configuration register sets up the address and the data for the Configuration register write. Setting the WR bit starts a long write to the Configuration register. The Configuration registers are written a byte at a time. To write or erase a configuration cell, a TBLWT instruction can write a '1' or a '0' into the cell. For additional details on Flash programming, refer to **Section 6.5 "Writing to Flash Program Memory"**.

TABLE 24-1: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h	CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	$\overline{\text{PWRTEN}}$	---1 1111
300003h	CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h	CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	—	1--- -01-
300006h	CONFIG4L	$\overline{\text{DEBUG}}$	XINST	BBSIZ1	BBSIZ2	—	LVP	—	STVREN	1000 -1-1
300008h	CONFIG5L	—	—	CP5(1)	CP4	CP3	CP2	CP1	CP0	--11 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	—	—	WRT5(1)	WRT4	WRT3	WRT2	WRT1	WRT0	--11 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	—	—	EBTR5(1)	EBTR4	EBTR3	EBTR2	EBTR1	EBTR0	--11 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx(2)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx(2)

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

Note 1: Unimplemented in PIC18F2682/4682 devices; maintain this bIt set.

2: See Register 24-12 and Register 24-13 for DEVID1 and DEVID2 values. DEVID registers are read-only and cannot be programmed by the user.

ANDWF **AND W with f**

Syntax: ANDWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .AND. (f) → dest

Status Affected: N, Z

Encoding:

0001	01da	ffff	ffff

Description: The contents of W are ANDed with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `ANDWF REG, 0, 0`

Before Instruction
W = 17h
REG = C2h
After Instruction
W = 02h
REG = C2h

BC **Branch if Carry**

Syntax: BC n

Operands: $-128 \le n \le 127$

Operation: if Carry bit is '1'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0010	nnnn	nnnn

Description: If the Carry bit is '1', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example:
```
HERE    BC   5
```
Before Instruction
PC = address (HERE)
After Instruction
If Carry = 1;
PC = address (HERE + 12)
If Carry = 0;
PC = address (HERE + 2)

CPFSGT — Compare f with W, Skip if f > W

Syntax: CPFSGT f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (f) – (W),
skip if (f) > (W)
(unsigned comparison)

Status Affected: None

Encoding:

0110	010a	ffff	ffff

Description: Compares the contents of data memory location 'f' to the contents of the W by performing an unsigned subtraction.

If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)

Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```
HERE      CPFSGT REG, 0
NGREATER  :
GREATER   :
```

Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG > W;
PC = Address (GREATER)
If REG ≤ W;
PC = Address (NGREATER)

CPFSLT — Compare f with W, Skip if f < W

Syntax: CPFSLT f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (f) – (W),
skip if (f) < (W)
(unsigned comparison)

Status Affected: None

Encoding:

0110	000a	ffff	ffff

Description: Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction.

If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

Words: 1

Cycles: 1(2)

Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```
HERE    CPFSLT REG, 1
NLESS   :
LESS    :
```

Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG < W;
PC = Address (LESS)
If REG ≥ W;
PC = Address (NLESS)

XORWF **Exclusive OR W with f**

Syntax: XORWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .XOR. (f) → dest

Status Affected: N, Z

Encoding:

0001	10da	ffff	ffff

Description: Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

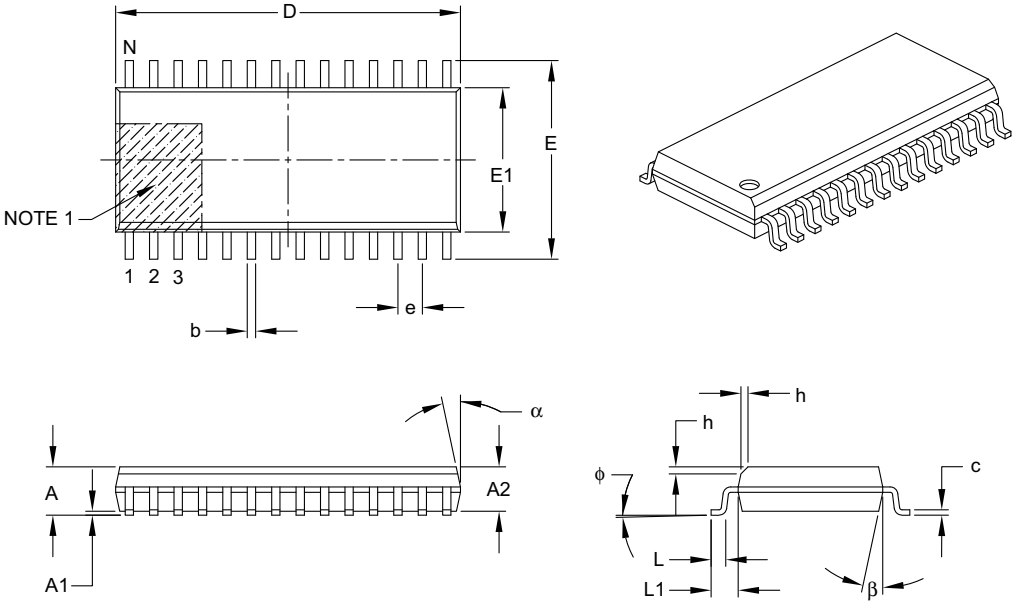
Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `XORWF REG, 1, 0`

Before Instruction
REG = AFh
W = B5h
After Instruction
REG = 1Ah
W = B5h

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle Top	ϕ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

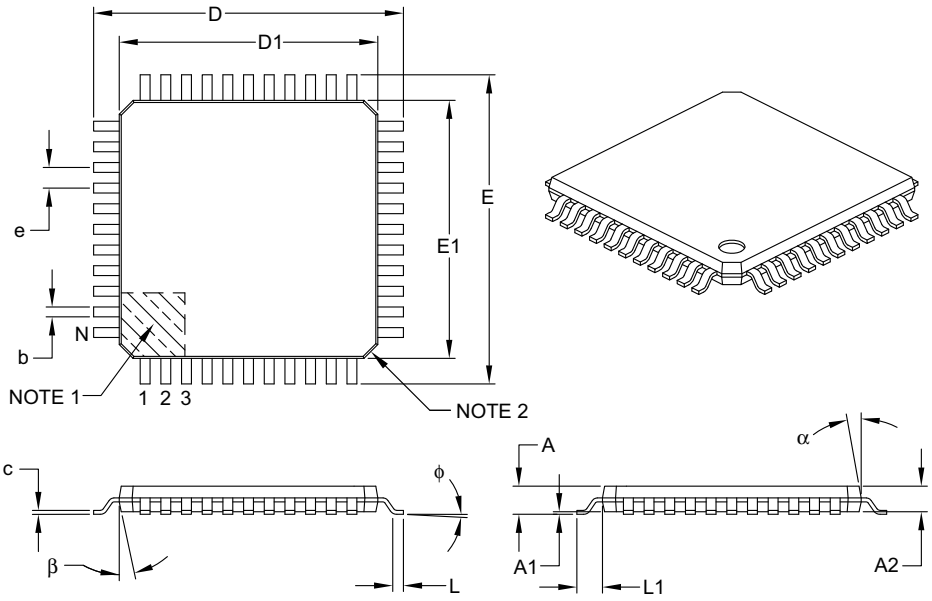
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B