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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4685t-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.4 RC Oscillator

For timing insensitive applications, the "RC" and "RCIO" device options offer additional cost savings. The actual oscillator frequency is a function of several factors:

- supply voltage
- values of the external resistor (REXT) and capacitor (CEXT)
- operating temperature

Given the same device, operating voltage and temperature and component values, there will also be unit-to-unit frequency variations. These are due to factors such as:

- normal manufacturing variation
- difference in lead frame capacitance between package types (especially for low CEXT values)
- variations within the tolerance of limits of $\ensuremath{\mathsf{REXT}}$ and $\ensuremath{\mathsf{CEXT}}$

In the RC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-5 shows how the R/C combination is connected.





The RCIO Oscillator mode (Figure 2-6) functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).



2.5 PLL Frequency Multiplier

A Phase Locked Loop (PLL) circuit is provided as an option for users who wish to use a lower frequency oscillator circuit or to clock the device up to its highest rated frequency from a crystal oscillator. This may be useful for customers who are concerned with EMI due to high-frequency crystals or users who require higher clock speeds from an internal oscillator.

2.5.1 HSPLL OSCILLATOR MODE

The HSPLL mode makes use of the HS mode oscillator for frequencies up to 10 MHz. A PLL then multiplies the oscillator output frequency by 4 to produce an internal clock frequency up to 40 MHz.

The PLL is only available to the crystal oscillator when the FOSC3:FOSC0 Configuration bits are programmed for HSPLL mode (= 0110).

FIGURE 2-7: PLL BLOCK DIAGRAM (HS MODE)



2.5.2 PLL AND INTOSC

The PLL is also available to the internal oscillator block in selected oscillator modes. In this configuration, the PLL is enabled in software and generates a clock output of up to 32 MHz. The operation of INTOSC with the PLL is described in **Section 2.6.4 "PLL in INTOSC Modes"**.

4.2 Master Clear Reset (MCLR)

The MCLR pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the MCLR Reset path which detects and ignores small pulses.

The MCLR pin is not driven low by any internal Resets, including the WDT.

In PIC18F2682/2685/4682/4685 devices, the $\overline{\text{MCLR}}$ input can be disabled with the MCLRE Configuration bit. When $\overline{\text{MCLR}}$ is disabled, the pin becomes a digital input. See **Section 10.5 "PORTE, TRISE and LATE Registers"** for more information.

4.3 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the $\overline{\text{MCLR}}$ pin through a resistor (1 k Ω to 10 k Ω) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the POR bit (RCON<1>). The state of the bit is set to '0' whenever a Power-on Reset occurs; it does not change for any other Reset event. POR is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any Power-on Reset.





10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch register (LAT) is useful for read-modifywrite operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. Pins RA6 and RA7 are multiplexed with the main oscillator pins. They are enabled as oscillator or I/O pins by the selection of the main oscillator in Configuration Register 1H (see **Section 24.1 "Configuration Bits"** for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of RA5 and RA3:RA0 pins as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note: On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE	10-1:	INITIALIZING PORTA

CLRF	PORTA	Initi	alize PORTA by
		clear	ing output
		data	latches
CLRF	LATA	Alter	nate method
		to cl	ear output
		data	latches
MOVLW	OFh	Confi	gure A/D
MOVWF	ADCON1	for d	igital inputs
MOVWF	07h	Confi	gure comparators
MOVWF	CMCON	for d	igital input
MOVLW	OCFh	Value	used to
		initi	alize data
		direc	tion
MOVWF	TRISA	Set R	A<3:0> as inputs
		RA<5:	4> as outputs

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB Data Output Register								
TRISB	PORTB Dat	a Direction F	Register						54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	_	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1		_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

13.0 TIMER2 MODULE

The Timer2 module incorporates the following features:

- 8-bit timer and period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- Interrupt on TMR2 to PR2 match
- Optional use as the shift clock for the MSSP module

The module is controlled through the T2CON register (Register 13-1), which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 13-1.

13.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (Fosc/4). A 2-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divideby-16 prescale options. These options are selected by the prescaler control bits, T2CKPS1:T2CKPS0 (T2CON<1:0>). The value of TMR2 is compared to that of the period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see Section 13.2 "Timer2 Interrupt").

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- · a write to the T2CON register
- any device Reset (Power-on Reset, MCLR Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 13-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:				
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7	Unimplemented: Read as '0'
bit 6-3	T2OUTPS3:T2OUTPS0: Timer2 Output Postscale Select bits
	0000 = 1:1 Postscale
	0001 = 1:2 Postscale
	•
	•
	•
	1111 = 1:16 Postscale
bit 2	TMR2ON: Timer2 On bit
	1 = Timer2 is on
	0 = Timer2 is off
bit 1-0	T2CKPS1:T2CKPS0: Timer2 Clock Prescale Select bits
	00 = Prescaler is 1
	01 = Prescaler is 4
	1x = Prescaler is 16

17.4.7 BAUD RATE

In I²C Master mode, the Baud Rate Generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 17-17). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting. The BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TcY) on the Q2 and Q4 clocks. In I²C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 17-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

FIGURE 17-17: BAUD RATE GENERATOR BLOCK DIAGRAM



TABLE 17-3: I²C[™] CLOCK RATE w/BRG

Fcy	Fcy*2	BRG Value	FscL (2 Rollovers of BRG)
10 MHz	20 MHz	19h	400 kHz ⁽¹⁾
10 MHz	20 MHz	20h	312.5 kHz
10 MHz	20 MHz	64h	100 kHz
4 MHz	8 MHz	0Ah	400 kHz ⁽¹⁾
4 MHz	8 MHz	0Dh	308 kHz
4 MHz	8 MHz	28h	100 kHz
1 MHz	2 MHz	03h	333 kHz ⁽¹⁾
1 MHz	2 MHz	0Ah	100 kHz
1 MHz	2 MHz	00h	1 MHz ⁽¹⁾

Note 1: The I²C[™] interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

17.4.7.1 Clock Arbitration

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, deasserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the

SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 17-18).





18.3 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTA<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit, SPEN (RCSTA<7>), is set in order to configure the TX and RX pins to CK (clock) and DT (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CK line. Clock polarity is selected with the SCKP bit (BAUDCON<4>); setting SCKP sets the Idle state on CK as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

18.3.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 18-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and the TXIF flag bit (PIR1<4>) is set. The interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXIE (PIE1<4>). TXIF is set regardless of the state of enable bit TXIE; it cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

To set up a Synchronous Master Transmission:

- 1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits SYNC SPEN and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.



FIGURE 18-11: SYNCHRONOUS TRANSMISSION

18.4 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTA<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

18.4.1 EUSART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical, except in the case of the Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- a) The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in the TXREG register.
- c) Flag bit TXIF will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- e) If enable bit TXIE is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. Clear bits CREN and SREN.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting enable bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREGx register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	54
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	54
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	54
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
TXREG	EUSART T	ransmit Regi	ister						53
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	53
SPBRGH	EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART E	Baud Rate Ge	enerator Re	gister Low E	Byte				53

TABLE 18-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: Reserved in PIC18F2682/2685 devices; always maintain these bits clear.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (AVDD and AVss), or the voltage level on the RA3/AN3/ VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D converter's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.



A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D converter can be configured as an analog input, or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH/ ADRESL registers, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 19-1.



PIC18F2682/2685/4682/4685



EXAMPLE 23-2: WIN AND ICODE BITS USAGE IN INTERRUPT SERVICE ROUTINE TO ACCESS TX/RX BUFFERS (CONTINUED)

ErrorInter	rupt	
BCF	PIR3, ERRIF	; Clear the interrupt flag
		; Handle error.
RETFIE		
TXB2Interr	upt	
BCF	PIR3, TXB2IF	; Clear the interrupt flag
GOTO	AccessBuffer	
TXB1Interr	upt	
BCF	PIR3, TXB1IF	; Clear the interrupt flag
GOTO	AccessBuffer	
TXB0Interr	upt	
BCF	PIR3, TXBOIF	; Clear the interrupt flag
GOTO	AccessBuffer	
RXBlInterr	upt	
BCF	PIR3, RXB1IF	; Clear the interrupt flag
GOTO	Accessbuffer	
RXB0Interr	upt	
BCF	PIR3, RXB0IF	; Clear the interrupt flag
GOTO	AccessBuffer	
AccessBuff	er	; This is either TX or RX interrupt
; Copy	CANSTAT.ICODE bits to CANC	CON.WIN bits
MOVF	TempCANCON, W	; Clear CANCON.WIN bits before copying
		; new ones.
ANDLW	B'11110001'	; Use previously saved CANCON value to
		; make sure same value.
MOVWF	TempCANCON	; Copy masked value back to TempCANCON
MOVF	TempCANSTAT, W	; Retrieve ICODE bits
ANDLW	B'00001110'	; Use previously saved CANSTAT value
		; to make sure same value.
IORWF	TempCANCON	; Copy ICODE bits to WIN bits.
MOVFF	TempCANCON, CANCON	; Copy the result to actual CANCON
; Acce	ss current buffer…	
; User	code	
; Rest	ore CANCON.WIN bits	
MOVF	CANCON, W	; Preserve current non WIN bits
ANDLW	B'11110001'	
IORWF	TempCANCON	; Restore original WIN bits
; Do n	ot need to restore CANSTAT	- it is read-only register.
; Retu	rn from interrupt or check	for another module interrupt source

$\label{eq:register23-11:} \textbf{TXBnDLC: TRANSMIT BUFFER n DATA LENGTH CODE $REGISTERS [0 \le n \le 2]$}$

U-0	R/W-x	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x					
_	TXRTR	_	_	DLC3	DLC2	DLC1	DLCO					
bit 7							bit 0					
Legend:												
R = Readab	le bit	W = Writable I	bit	U = Unimplei	mented bit, rea	d as '0'						
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown					
bit 7	Unimplemer	nted: Read as ')'									
bit 6	TXRTR: Trar	nsmit Remote Fi	rame Transm	nission Request	t bit							
	1 = Transmit	ted message wi	ll have TXRT	R bit set								
	0 = Transmit	ted message wi	ll have TXRT	R bit cleared								
bit 5-4	Unimplemer	nted: Read as '0)'									
bit 3-0	DLC3:DLC0:	: Data Length C	ode bits									
	1111 = Rese	erved										
	1110 = Rese	erved										
	1101 = Rese	erved										
	1100 = Rese	1100 = Reserved										
	1011 = Rese	erved										
	1010 = Rese	erved										
	1001 = Rese	erved										
	1000 = Data	length = 8 bytes	S									
	0111 = Data	length = 7 bytes	5									
	0110 = Data	length = 6 bytes	5									
	0101 - Dala	length = 4 bytes	5									
	0011 = Data	length = 3 byte	5									
	0011 = Data	length = 2 byte	s									
	0001 = Data	length = 1 byte	5									
	0000 = Data	length = 0 bytes	S									

REGISTER 23-12: TXERRCNT: TRANSMIT ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TEC7:TEC0:** Transmit Error Counter bits This register contains a value which is derived from the rate at which errors occur. When the error count overflows, the bus-off state occurs. When the bus has 128 occurrences of 11 consecutive recessive bits, the counter value is cleared.

24.3 **Two-Speed Start-up**

The Two-Speed Start-up feature helps to minimize the latency period from oscillator start-up to code execution by allowing the microcontroller to use the INTRC oscillator as a clock source until the primary clock source is available. It is enabled by setting the IESO Configuration bit.

Two-Speed Start-up should be enabled only if the primary oscillator mode is LP, XT, HS or HSPLL (Crystal-based modes). Other sources do not require an OST start-up delay; for these, Two-Speed Start-up should be disabled.

When enabled, Resets and wake-ups from Sleep mode cause the device to configure itself to run from the internal oscillator block as the clock source, following the time-out of the Power-up Timer after a Power-on Reset is enabled. This allows almost immediate code execution while the primary oscillator starts and the OST is running. Once the OST times out, the device automatically switches to PRI RUN mode.

Because the OSCCON register is cleared on Reset events, the INTOSC (or postscaler) clock source is not initially available after a Reset event; the INTRC clock is used directly at its base frequency. To use a higher clock speed on wake-up, the INTOSC or postscaler clock sources can be selected to provide a higher clock speed by setting bits, IRCF2:IRCF0, immediately after

Reset. For wake-ups from Sleep, the INTOSC or postscaler clock sources can be selected by setting the IRCF2:IRCF0 bits prior to entering Sleep mode.

In all other power-managed modes, Two-Speed Start-up is not used. The device will be clocked by the currently selected clock source until the primary clock source becomes available. The setting of the IESO bit is ignored.

24.3.1 SPECIAL CONSIDERATIONS FOR USING TWO-SPEED START-UP

While using the INTRC oscillator in Two-Speed Start-up, the device still obeys the normal command sequences for entering power-managed modes, including serial SLEEP instructions (refer to Section 3.1.4 "Multiple Sleep Commands"). In practice, this means that user code can change the SCS1:SCS0 bit settings or issue SLEEP instructions before the OST times out. This would allow an application to briefly wake-up, perform routine "housekeeping" tasks and return to Sleep before the device starts to operate from the primary oscillator.

User code can also check if the primary clock source is currently providing the device clocking by checking the status of the OSTS bit (OSCCON<3>). If the bit is set, the primary oscillator is providing the clock. Otherwise, the internal oscillator block is providing the clock during wake-up from Reset or Sleep mode.



FIGURE 24-2: TIMING TRANSITION FOR TWO-SPEED START-UP (INTOSC TO HSPLL)

24.5.2 DATA EEPROM CODE PROTECTION

The entire data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of data EEPROM. WRTD inhibits internal and external writes to data EEPROM. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

24.5.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In normal execution mode, the WRTC bit is readable only. WRTC can only be written via ICSP or an external programmer.

24.6 ID Locations

Eight memory locations (20000h-200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are both readable and writable during normal execution through the TBLRD and TBLWT instructions or during program/verify. The ID locations can be read when the device is code-protected.

24.7 In-Circuit Serial Programming

PIC18F2682/2685/4682/4685 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

24.8 In-Circuit Debugger

When the DEBUG Configuration bit is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB[®] IDE. When the microcontroller has this feature enabled, some resources are not available for general use. Table 24-4 shows which resources are required by the background debugger.

TABLE 24-4: DEBUGGER RESOURCES

I/O pins:	RB6, RB7
Stack:	2 levels
	-

Note: Memory sources listed in MPLAB[®] IDE.

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP/RE3, VDD, Vss, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

24.9 Single-Supply ICSP Programming

The LVP Configuration bit enables Single-Supply ICSP programming (formerly known as *Low-Voltage ICSP Programming* or *LVP*). When Single-Supply Programming is enabled, the microcontroller can be programmed without requiring high voltage being applied to the MCLR/VPP/RE3 pin, but the RB5/KBI1/PGM pin is then dedicated to controlling Program mode entry and is not available as a general purpose I/O pin.

While programming using Single-Supply Programming, VDD is applied to the MCLR/VPP/RE3 pin as in normal execution mode. To enter Programming mode, VDD is applied to the PGM pin.

- Note 1: High-voltage programming is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR pin.
 - 2: While in Low-Voltage ICSP Programming mode, the RB5 pin can no longer be used as a general purpose I/O pin and should be held low during normal operation.
 - 3: When using Low-Voltage ICSP Programming (LVP) and the pull-ups on PORTB are enabled, bit 5 in the TRISB register must be cleared to disable the pull-up on RB5 and ensure the proper operation of the device.
 - 4: If the device Master Clear is disabled, verify that either of the following is done to ensure proper entry into ICSP mode:
 - a) disable Low-Voltage Programming (CONFIG4L<2> = 0); or
 - b) make certain that RB5/KBI1/PGM is held low during entry into ICSP.

If Single-Supply ICSP Programming mode will not be used, the LVP bit can be cleared. RB5/KB11/PGM then becomes available as the digital I/O pin, RB5. The LVP bit may be set or cleared only when using standard high-voltage programming (VIHH applied to the MCLR/ VPP/RE3 pin). Once LVP has been disabled, only the standard high-voltage programming is available and must be used to program the device.

Memory that is not code-protected can be erased using either a block erase, or erased row by row, then written at any specified VDD. If code-protected memory is to be erased, a block erase is required. If a block erase is to be performed when using Low-Voltage Programming, the device must be supplied with VDD of 4.5V to 5.5V.

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DECFSZ Decrement f, Skip if 0									
Syntax:	DECFSZ f	DECFSZ f {,d {,a}}							
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$							
Operation:	(f) – 1 \rightarrow de skip if result	$(f) - 1 \rightarrow dest,$ skip if result = 0							
Status Affected:	None								
Encoding:	0010	11da ffi	ff ffff						
Description: Words:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If the result is '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f \leq 95 (5Fh). See Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.								
Cycles:	1(2)	1(2)							
	Note: 3 c by	Note: 3 cycles if skip and followed by a 2-word instruction.							
Q Cycle Activity:									
Q1 Decode	Q2 Read	Q3 Process	Q4 Write to						
lf skin:	register f	Data	destination						
Ω1	02	Q3	04						
No	No	No	No						
operation	operation	operation	operation						
If skip and followe	d by 2-word in	struction:							
Q1	Q2	Q3	Q4						
No	No	No	No						
No	No	No	No						
operation	operation	operation	operation						
			. · .						
Example:	HERE CONTINUE	DECFSZ GOTO	CNT, 1, 1 LOOP						
Before Instruct PC	ction = Address	G (HERE)							
CNT If CNT PC If CNT PC	= CNT – 1 = 0; = Address ≠ 0; = Address	G (CONTINUE G (HERE + 2)						

DCF	SNZ	Decreme	Decrement f, Skip if Not 0							
Synta	ax:	DCFSNZ	DCFSNZ f {,d {,a}}							
Oper	ands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$							
Oper	ation:	(f) – 1 \rightarrow de skip if resul	$(f) - 1 \rightarrow dest,$ skip if result $\neq 0$							
Statu	s Affected:	None								
Enco	ding:	0100	0100 11da ffff ffff							
Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If the result is not '0', the next instruction which is already fetched i discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is '0', the Access Bank is selectrif 'a' is '0', the BSR is used to select for GPR bank (default). If 'a' is '0', and the extended instruction operation in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed										
Word	ls:	1	1							
Cycle	es: vcle Activity:	1(2) Note: 3 o by	1(2) Note: 3 cycles if skip and followed by a 2-word instruction.							
<u> </u>	Q1	Q2	Q3	Q4						
	Decode	Read register 'f'	Process Data	Write to destination						
lf sk	ip:									
	Q1	Q2	Q3	Q4						
	No	No	No	No						
lfek	in and follower	operation	operation:	operation						
11 51		0.2	0.3	04						
	No	No	No	No						
	operation	operation	operation	operation						
No		No	No	No						
	operation	operation	operation	operation						
<u>Example:</u>		HERE ZERO NZERO	HERE DCFSNZ TEMP, 1, ZERO : NZERO :							
	Before Instruc	tion –	2							
After Instruction		= on	ſ							
TEMP		=	TEMP – 1,							
	IT LEMP PC	=	U; Address (ZERO)							
	If TEMP	≠ =	0; Address	NZERO)						
	. 0			,						

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POF)	Рор Тор	of Retu	rn Stad	ck				
Synta	ax:	POP	POP						
Oper	ands:	None							
Oper	ation:	$(TOS) \rightarrow b$	oit bucket						
Statu	is Affected:	None	None						
Enco	oding:	0000	0000	0 0110					
Desc	ription:	The TOS v stack and then becon was pushe This instru the user to stack to in	The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack. This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.						
Word	ds:	1	1						
Cycle	es:	1							
QC	ycle Activity:								
	Q1	Q2	Q3		Q4				
	Decode	No operation	POP T valu	OS e	No operation				
Example:		POP GOTO	NEW						
Before Instructio TOS Stack (1 le		tion level down)	= () = ()	031A21 0143321	h 1				
After Instruction TOS PC		n	= (= N)14332h NEW	ı				

PUSH	Push Top	Push Top of Return Stack					
Syntax:	PUSH	PUSH					
Operands:	None						
Operation:	$(PC + 2) \rightarrow$	TOS					
Status Affected:	None						
Encoding:	0000	0000	000	0 (0101		
Description:	The PC + 2 the return s value is pus This instruc software sta then pushir	The PC + 2 is pushed onto the top of the return stack. The previous TOS value is pushed down on the stack. This instruction allows implementing a software stack by modifying TOS and then pushing it onto the return stack					
Words:	1	-					
Cycles:	1						
Q Cycle Activity:							
Q1	Q2	Q3 No operation			Q4		
Decode	PUSH PC + 2 onto return stack			ор	No eration		
Example:	PUSH						
Before Instru TOS PC	ction	= (345Ah)124h				
After Instruct PC TOS	ion	= ()126h)126h				

27.2 DC Characteristics:

Power-Down and Supply Current PIC18F2682/2685/4682/4685 (Industrial) PIC18LF2682/2685/4682/4685 (Industrial) (Continued)

PIC18LF: (Indus	2682/2685/4682/4685 strial)	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial						
PIC18F20 (Indus	682/2685/4682/4685 strial, Extended)	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Device	Тур	Max	Units	Conditions			
	Supply Current (IDD) ^(2,3)							
	All devices	9.00	18.00	mA	-40°C			
		8.90	17.00	mA	+25°C	VDD = 4.2V	FOSC = 4 MHZ (PRI RUN HSPLL)	
		8.80	16.00	mA	+85°C			
	All devices	12.00	24.00	mA	-40°C			
		12.00	22.00	mA	+25°C	VDD = 5.0V	(PRI RUN HSPLL)	
		12.00	21.00	mA	+85°C		(***_**********************************	
	All devices	21.00	39.00	mA	-40°C			
		21.00	39.00	mA	+25°C	VDD = 4.2V	(PRI RUN HSPLL)	
		21.00	39.00	mA	+85°C			
	All devices	28.00	44.00	mA	-40°C			
		28.00	44.00	mA	+25°C	VDD = 5.0V		
		28.00	44.00	mA	+85°C		()	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

MCLR = VDD; WDT enabled/disabled as specified.

- **3:** For RC oscillator configurations, current through RExT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.
- 4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

27.4.3 TIMING DIAGRAMS AND SPECIFICATIONS



TABLE 27-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Мах	Units	Conditions
1A	Fosc	External CLKI Frequency ⁽¹⁾	DC	1	MHz	XT, RC Oscillator modes
			DC	25	MHz	HS Oscillator mode
			DC	31.25	kHz	LP Oscillator mode
			DC	40	MHz	EC Oscillator mode
		Oscillator Frequency ⁽¹⁾	DC	4	MHz	RC Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	25	MHz	HS Oscillator mode
			4	10	MHz	HSPLL Oscillator mode
			5	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period ⁽¹⁾	1000	—	ns	XT, RC Oscillator modes
			40	—	ns	HS Oscillator mode
			32	—	μS	LP Oscillator mode
			25	—	ns	EC Oscillator mode
		Oscillator Period ⁽¹⁾	250	—	ns	RC Oscillator mode
			250	1	μS	XT Oscillator mode
			40	250	ns	HS Oscillator mode
			100	250	ns	HSPLL Oscillator mode
			5	200	μS	LP Oscillator mode
2	Тсү	Instruction Cycle Time ⁽¹⁾	100	—	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1)	30	—	ns	XT Oscillator mode
	TosH	High or Low Time	2.5	—	μS	LP Oscillator mode
			10	—	ns	HS Oscillator mode
4	TosR,	External Clock in (OSC1)	—	20	ns	XT Oscillator mode
	TosF	Rise or Fall Time	—	50	ns	LP Oscillator mode
			—	7.5	ns	HS Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

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