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XMOS - XS1-L6A-64-LQ64-I4 Datasheet



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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	XCore
Core Size	32-Bit 6-Core
Speed	400MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	36
Program Memory Size	64KB (16K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-l6a-64-lq64-i4

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Channels and channel ends Tasks running on logical cores communicate using channels formed between two channel ends. Data can be passed synchronously or asynchronously between the channel ends assigned to the communicating tasks. Section 5.5
- xCONNECT Switch and Links Between tiles, channel communications are implemented over a high performance network of xCONNECT Links and routed through a hardware xCONNECT Switch. Section 5.6
- ▶ **Ports** The I/O pins are connected to the processing cores by Hardware Response ports. The port logic can drive its pins high and low, or it can sample the value on its pins optionally waiting for a particular condition. Section 5.3
- Clock blocks xCORE devices include a set of programmable clock blocks that can be used to govern the rate at which ports execute. Section 5.4
- Memory Each xCORE Tile integrates a bank of SRAM for instructions and data, and a block of one-time programmable (OTP) memory that can be configured for system wide security features. Section 8
- PLL The PLL is used to create a high-speed processor clock given a low speed external oscillator. Section 6
- JTAG The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory. Section 9

1.1 Software

Devices are programmed using C, C++ or xC (C with multicore extensions). XMOS provides tested and proven software libraries, which allow you to quickly add interface and processor functionality such as USB, Ethernet, PWM, graphics driver, and audio EQ to your applications.

1.2 xTIMEcomposer Studio

The xTIMEcomposer Studio development environment provides all the tools you need to write and debug your programs, profile your application, and write images into flash memory or OTP memory on the device. Because xCORE devices operate deterministically, they can be simulated like hardware within xTIMEcomposer: uniquely in the embedded world, xTIMEcomposer Studio therefore includes a static timing analyzer, cycle-accurate simulator, and high-speed in-circuit instrumentation.

xTIMEcomposer can be driven from either a graphical development environment, or the command line. The tools are supported on Windows, Linux and MacOS X and available at no cost from xmos.com/downloads. Information on using the tools is provided in the xTIMEcomposer User Guide, X3766.

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3 Pin Configuration



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- ► A 32-bit program size *s* in words.
- Program consisting of $s \times 4$ bytes.
- A 32-bit CRC, or the value 0x0D15AB1E to indicate that no CRC check should be performed.

The program size and CRC are stored least significant byte first. The program is loaded into the lowest memory address of RAM, and the program is started from that address. The CRC is calculated over the byte stream represented by the program size and the program itself. The polynomial used is 0xEDB88320 (IEEE 802.3); the CRC register is initialized with 0xFFFFFFFF and the residue is inverted to produce the CRC.

7.1 Boot from SPI master

If set to boot from SPI master, the processor enables the four pins specified in Figure 9, and drives the SPI clock at 2.5 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

Figure 9: SPI master pins

PinSignalDescriptionX0D00MISOMaster In Slave Out (Data)9:X0D01SSSlave Select2rX0D10SCLKClockSX0D11MOSIMaster Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. Programmers who write bytes into an SPI interface using the most significant bit first may have to reverse the bits in each byte of the image stored in the SPI device.

If a large boot image is to be read in, it is faster to first load a small boot-loader that reads the large image using a faster SPI clock, for example 50 MHz or as fast as the flash device supports.

The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

7.2 Boot from xConnect Link

If set to boot from an xConnect Link, the processor enables Link B around 200 ns after the boot process starts. Enabling the Link switches off the pull-down on resistors X0D16..X0D19, drives X0D16 and X0D17 low (the initial state for the Link), and monitors pins X0D18 and X0D19 for boot-traffic. X0D18 and X0D19 must be low at this stage. If the internal pull-down is too weak to drain any residual charge, external pull-downs of 10K may be required on those pins.

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The boot-rom on the core will then:

- 1. Allocate channel-end 0.
- 2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
- 3. Input the boot image specified above, including the CRC.
- 4. Input an END control token.
- 5. Output an END control token to the channel-end received in step 2.
- 6. Free channel-end 0.
- 7. Jump to the loaded code.

7.3 Boot from OTP

If an xCORE tile is set to use secure boot (see Figure 7), the boot image is read from address 0 of the OTP memory in the tile's security module.

This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

Each tile has its own individual OTP memory, and hence some tiles can be booted from OTP while others are booted from SPI or the channel interface. This enables systems to be partially programmed, dedicating one or more tiles to perform a particular function, leaving the other tiles user-programmable.

7.4 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 10 provide a strong level of protection and are sufficient for providing strong IP security.

8 Memory

8.1 OTP

The xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in four sectors each containing 512 rows of 32 bits which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

The OTP memory is programmed using three special I/O ports: the OTP address port is a 16-bit port with resource ID 0x100200, the OTP data is written via a 32-bit



Solder paste and ground via recommendations are based on our engineering and development kit board production. They have been found to work and optimized as appropriate to achieve a high yield. The size, type and number of vias used in the center pad affects how much solder wicks down the vias during reflow. This in turn, along with solder paster coverage, affects the final assembled package height. These factors should be taken into account during design and manufacturing of the PCB.

The following land patterns and solder paste contains recommendations. Final land pattern and solder paste decisions are the responsibility of the customer. These should be tuned during manufacture to suit the manufacturing process.

The package is a 64 pin Low profile Quad Flat Pack package with exposed heat slug on a 0.5mm pitch. An example land pattern is shown in Figure 14.



Figure 14: Example land pattern

> For the 64 pin LQFP package, a 3x3 array of squares for solder paste is recommended as shown in Figure 15. This gives a paste level of 48%.



10.2 Ground and Thermal Vias

Vias under the heat slug into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. A 3×3 grid of vias, with a 0.6mm diameter annular ring and a 0.3mm drill, equally spaced across the heat slug, would be suitable.

10.3 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour pressure of moisture. Example damage can include bond wire damage, die lifting, internal or external package cracks and/or delamination.

All XMOS devices are Moisture Sensitivity Level (MSL) 3 - devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from *Joint IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices* J-STD-020 Revision D.

11 DC and Switching Characteristics

Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIO	I/O supply voltage	3.00	3.30	3.60	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	
CI	xCORE Tile I/O load capacitance			25	pF	
Та	Ambient operating temperature (Commercial)	0		70	°C	
	Ambient operating temperature (Industrial)	-40		85	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

11.1 Operating Conditions

Figure 16: Operating conditions

11.2 DC Characteristics

Sy	mbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(I	IH)	Input high voltage	2.00		3.60	V	А
V(I	IL)	Input low voltage	-0.30		0.70	V	А
V(0	OH)	Output high voltage	2.00			V	B, C
V(0	OL)	Output low voltage			0.60	V	B, C
R(F	PU)	Pull-up resistance		35K		Ω	D
R(F	PD)	Pull-down resistance		35K		Ω	D

Figure 17: DC characteristics

A All pins except power supply pins.

B Ports 1A, 1D, 1E, 1H, 1I, 1J, 1K and 1L are nominal 8 mA drivers, the remainder of the general-purpose I/Os are 4 mA.

C Measured with 4 mA drivers sourcing 4 mA, 8 mA drivers sourcing 8 mA.

D Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.

11.3 ESD Stress Voltage

Figure 18:	
ESD stress	
voltage	-

Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
HBM	Human body model	-2.00		2.00	KV	
MM	Machine model	-200		200	V	



11.4 Reset Timing

Figure 19: Reset timing

Symbol	Parameters	MIN	ТҮР	MAX	UNITS	Notes
T(RST)	Reset pulse width	5			μs	
T(INIT)	Initialization time			150	μs	А

A Shows the time taken to start booting after RST_N has gone high.

11.5 Power Consumption

Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		14		mA	А, В, С
PD	Tile power dissipation		450		µW/MIPS	A, D, E, F
IDD	Active VDD current (Speed Grade 4)		160	300	mA	A, G
	Active VDD current (Speed Grade 5)		200	375	mA	А, Н
I(ADDPLL)	PLL_AVDD current			7	mA	I

Figure 20: xCORE Tile currents

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages with no switching activity.

C Includes PLL current.

D Assumes typical tile and I/O voltages with nominal switching activity.

E Assumes 1 MHz = 1 MIPS.

F PD(TYP) value is the usage power consumption under typical operating conditions.

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G Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 400 MHz, average device resource usage.

H Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.

I PLL_AVDD = 1.0 V



The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.

More detailed power analysis can be found in the XS1-L Power Consumption document, X2999.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			18	MHz	
f(TCK_B)	TCK frequency (boundary scan)			10	MHz	
T(SETUP)	TDO to TCK setup time	5			ns	А
T(HOLD)	TDO to TCK hold time	5			ns	А
T(DELAY)	TCK to output delay			15	ns	В

11.9 JTAG Timing

Figure 24: JTAG timing

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.



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- ITE : DATUM A-B AND D TO DETERMINE AT DATUM PLANE H. TO BE DETERMINED AT SEATING DATUM PLANE C. DIMENSION DI AND EI DO NDT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DI AND EI ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH. DIMENSION SHALL NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 6 DIMENSION BY MORE THAN 0.08mm, DAMBAR CANNOT BE LOCATED DN THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGE. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP. AI IS THE DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY. PACKAGE DIMENSIONS REFERENCE TO JEDEC MS-026 Rev.D, except D2 and E2 ④
- ര
- 6 7

LF Ref# Symbol Min Nom Max 5.03 5.13 D2 4.93 L - 16 - 090064.93 5.03 5.13 E2

<u>B</u> /1

: 20:1

DETAIL SCALE



B.8 Ring Oscillator Value: 0x08

This register contains the current count of the xCORE Tile Wire ring oscillator. This value is not reset on a system reset.

0x08: Ring Oscillator Value

Bits	Perm	Init	Description	
31:16	RO	-	Reserved	
15:0	RO	-	Ring oscillator counter data.	

B.9 Ring Oscillator Value: 0x09

This register contains the current count of the Peripheral Cell ring oscillator. This value is not reset on a system reset.

0x09 Ring Oscillator Value

:	Bits	Perm	Init	Description
-	31:16	RO	-	Reserved
2	15:0	RO	-	Ring oscillator counter data.

B.10 Ring Oscillator Value: 0x0A

This register contains the current count of the Peripheral Wire ring oscillator. This value is not reset on a system reset.

0x0A: Ring Oscillator Value

A:	Bits	Perm	Init	Description
9 Dr	31:16	RO	-	Reserved
e	15:0	RO	-	Ring oscillator counter data.

B.11 Debug SSR: 0x10

This register contains the value of the SSR register when the debugger was called.

0x10:	Bits	Perm	Init	Description
Debug SSR	31:0	RO	-	Reserved

B.12 Debug SPC: 0x11

This register contains the value of the SPC register when the debugger was called.

C.1 Device identification: 0x00

0x00:
Device
identification

Bits	Perm	Init	Description
31:24	RO		Processor ID of this xCORE tile.
23:16	RO		Number of the node in which this xCORE tile is located.
15:8	RO		xCORE tile revision.
7:0	RO		xCORE tile version.

C.2 xCORE Tile description 1: 0x01

This register describes the number of logical cores, synchronisers, locks and channel ends available on this xCORE tile.

	Bits	Perm	Init	Description
	31:24	RO		Number of channel ends.
-	23:16	RO		Number of locks.
e.	15:8	RO		Number of synchronisers.
1	7:0	RO	-	Reserved
	L	1		l

xCORE Tile description 1

0x0

C.3 xCORE Tile description 2: 0x02

This register describes the number of timers and clock blocks available on this xCORE tile.

0x02: xCORE Tile description 2

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:8	RO		Number of clock blocks.
7:0	RO		Number of timers.

C.4 Control PSwitch permissions to debug registers: 0x04

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This register can be used to control whether the debug registers (marked with permission CRW) are accessible through the tile configuration registers. When this bit is set, write -access to those registers is disabled, preventing debugging of the xCORE tile over the interconnect.

C.11 PC of logical core 1: 0x41

Ox41:PC of logical
core 131:0

C.12 PC of logical core 2: 0x42

0x42: PC of logical	Bits	Perm	Init	Description
core 2	31:0	RO		Value.

Description

Value.

C.13 PC of logical core 3: 0x43

0x43.				
PC of logical	Bits	Perm	Init	Description
core 3	31:0	RO		Value.

C.14 PC of logical core 4: 0x44

0x44: PC of logical core 4

Bits	Perm	Init	Description
31:0	RO		Value.

C.15 PC of logical core 5: 0x45

0.45				
PC of logical	Bits	Perm	Init	Description
core 5	31:0	RO		Value.

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C.16 SR of logical core 0: 0x60

Value of the SR of logical core 0

D Node Configuration

The digital node control registers can be accessed using configuration reads and writes (use write_node_config_reg(device, ...) and read_node_config_reg(device, ...) for reads and writes).

Number	Perm	Description	
0x00	RO	Device identification	
0x01	RO	System switch description	
0x04	RW	Switch configuration	
0x05	RW	Switch node identifier	
0x06	RW	PLL settings	
0x07	RW	System switch clock divider	
0x08	RW	Reference clock	
0x0C	RW	Directions 0-7	
0x0D	RW	Directions 8-15	
0x10	RW	DEBUG_N configuration	
0x1F	RO	Debug source	
0x20 0x27	RW	Link status, direction, and network	
0x40 0x43	RW	PLink status and network	
0x80 0x87	RW	Link configuration and initialization	
0xA0 0xA7	RW	Static link configuration	

Figure 30: Summary

D.1 Device identification: 0x00

This register contains version and revision identifiers and the mode-pins as sampled at boot-time.

	Bits	Perm	Init	Description
	31:24	RO	0x00	Chip identifier.
0×00:	23:16	RO		Sampled values of pins MODE0, MODE1, on reset.
Device	15:8	RO		SSwitch revision.
identification	7:0	RO		SSwitch version.

D.2 System switch description: 0x01

This register specifies the number of processors and links that are connected to this switch.

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Bits	Perm	Init	Description	
31:26	RO	-	Reserved	
25:23	RW		OD: Output divider value The initial value depends on pins MODE0 and MODE1.	
22:21	RO	-	Reserved	
20:8	RW		F: Feedback multiplication ratio The initial value depends on pins MODE0 and MODE1.	
7	RO	-	Reserved	
6:0	RW		R: Oscilator input divider value The initial value depends on pins MODE0 and MODE1.	

0x06: PLL settings

D.6 System switch clock divider: 0x07

Sets the ratio of the PLL clock and the switch clock.

0x07 System switch clock divider

7.	Bits	Perm	Init	Description
m.	31:16	RO	-	Reserved
ck er	15:0	RW	0	Switch clock divider. The PLL clock will be divided by this value plus one to derive the switch clock.

D.7 Reference clock: 0x08

Sets the ratio of the PLL clock and the reference clock used by the node.

0x08: Reference clock

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	3	Architecture reference clock divider. The PLL clock will be divided by this value plus one to derive the 100 MHz reference clock.

D.8 Directions 0-7: 0x0C

This register contains eight directions, for packets with a mismatch in bits 7..0 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

D.11 Debug source: 0x1F

Contains the source of the most recent debug event.

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RW		If set, the external DEBUG_N pin is the source of the most recent debug interrupt.
3:1	RO	-	Reserved
0	RW		If set, the xCORE Tile is the source of the most recent debug interrupt.

0x1F: Debug source

D.12 Link status, direction, and network: 0x20 .. 0x27

These registers contain status information for low level debugging (read-only), the network number that each link belongs to, and the direction that each link is part of. The registers control links C, D, A, B, G, H, E, and F in that order.

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to: 0: plink 1: external link 2: internal control link
23:16	RO	0	If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent.
15:12	RO	-	Reserved
11:8	RW	0	The direction that this this link is associated with; set for rout- ing.
7:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, set for quality of service.
3	RO	-	Reserved
2	RO	0	Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

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0x20 .. 0x27: Link status, direction, and network



	Bits	Perm	Init	Description
	31	RW	0	Write '1' to this bit to enable the link, write '0' to disable it. This bit controls the muxing of ports with overlapping links.
	30	RW	0	Set to 0 to operate in 2 wire mode or 1 to operate in 5 wire mode
	29:28	RO	-	Reserved
	27	RO	0	Set to 1 on error: an RX buffer overflow or illegal token encoding has been received. This bit clears on reading.
	26	RO	0	1 if this end of the link has issued credit to allow the remote end to transmit.
	25	RO	0	1 if this end of the link has credits to allow it to transmit.
	24	WO	0	Set to 1 to initialize a half-duplex link. This clears this end of the link's credit and issues a HELLO token; the other side of the link will reply with credits. This bit is self-clearing.
	23	WO	0	Set to 1 to reset the receiver. The next symbol that is detected will be assumed to be the first symbol in a token. This bit is self-clearing.
7.	22	RO	-	Reserved
nk on	21:11	RW	0	The number of system clocks between two subsequent transi- tions within a token
nd on	10:0	RW	0	The number of system clocks between two subsequent transmit tokens.

0x80 .. 0x87 Link configuration and initialization

D.15 Static link configuration: 0xA0 .. 0xA7

These registers are used for static (ie, non-routed) links. When a link is made static, all traffic is forwarded to the designated channel end and no routing is attempted. The registers control links C, D, A, B, G, H, E, and F in that order.

	Bits	Perm	Init	Description
	31	RW	0	Enable static forwarding.
:	30:5	RO	-	Reserved
	4:0	RW	0	The destination channel end on this node that packets received in static mode are forwarded to.

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0xA0 .. 0xA7 Static link configuration

G JTAG, xSCOPE and Debugging

If you intend to design a board that can be used with the XMOS toolchain and xTAG debugger, you will need an xSYS header on your board. Figure 32 shows a decision diagram which explains what type of xSYS connectivity you need. The three subsections below explain the options in detail.



G.1 No xSYS header

The use of an xSYS header is optional, and may not be required for volume production designs. However, the XMOS toolchain expects the xSYS header; if you do not have an xSYS header then you must provide your own method for writing to flash/OTP and for debugging.

G.2 JTAG-only xSYS header

The xSYS header connects to an xTAG debugger, which has a 20-pin 0.1" female IDC header. The design will hence need a male IDC header. We advise to use a boxed header to guard against incorrect plug-ins. If you use a 90 degree angled header, make sure that pins 2, 4, 6, ..., 20 are along the edge of the PCB.

Connect pins 4, 8, 12, 16, 20 of the xSYS header to ground, and then connect:

- ▶ TDI to pin 5 of the xSYS header
- TMS to pin 7 of the xSYS header
- TCK to pin 9 of the xSYS header
- DEBUG_N to pin 11 of the xSYS header

H Schematics Design Check List

✓ This section is a checklist for use by schematics designers using the XS1-L6A-64-LQ64. Each of the following sections contains items to check for each design.

H.1 Power supplies

- □ VDDIO supply is within specification before the VDD (core) supply is turned on. Specifically, the VDDIO supply is within specification before VDD (core) reaches 0.4V (Section 10).
- □ The VDD (core) supply ramps monotonically (rises constantly) from 0V to its final value (0.95V 1.05V) within 10ms (Section 10).
- The VDD (core) supply is capable of supplying 300mA (Section 10).
- PLL_AVDD is filtered with a low pass filter, for example an RC filter, see Section 10

H.2 Power supply decoupling

- The design has multiple decoupling capacitors per supply, for example at least four0402 or 0603 size surface mount capacitors of 100nF in value, per supply (Section 10).
- □ A bulk decoupling capacitor of at least 10uF is placed on each supply (Section 10).

H.3 Power on reset

The RST_N and TRST_N pins are asserted (low) during or after power up. The device is not used until these resets have taken place. As the errata in the datasheets show, the internal pull-ups on these two pins can occasionally provide stronger than normal pull-up currents. For this reason, an RC type reset circuit is discouraged as behavior would be unpredictable. A voltage supervisor type reset device is recommended to guarantee a good reset. This also has the benefit of resetting the system should the relevant supply go out of specification.

H.4 Clock

The CLK input pin is supplied with a clock with monotonic rising edges and low jitter.

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L Revision History

Date	Description
2013-01-30	New datasheet - revised part numbering
2013-02-26	New multicore microcontroller introduction
	Moved configuration sections to appendices
2013-07-19	Updated Features list with available ports and links - Section 2
	Simplified link bits in Signal Description - Section 4
	New JTAG, xSCOPE and Debugging appendix - Section G
	New Schematics Design Check List - Section H
	New PCB Layout Design Check List - Section I
2013-12-09	Added Industrial Ambient Temperature - Section 11.1
2014-04-25	Land pattern pad width updated to 1.6mm - Section 10
2015-04-14	Updated Introduction - Section 1; Pin Configuration - Section 3; Signal Descrip- tion - Section 4

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