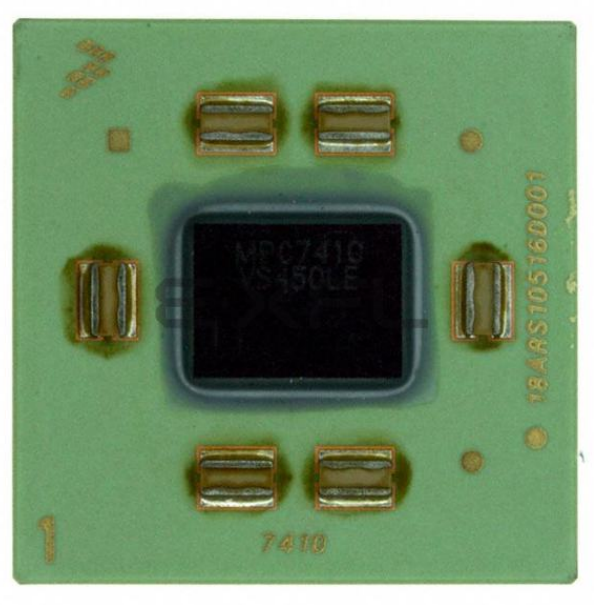

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Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7410vs500le

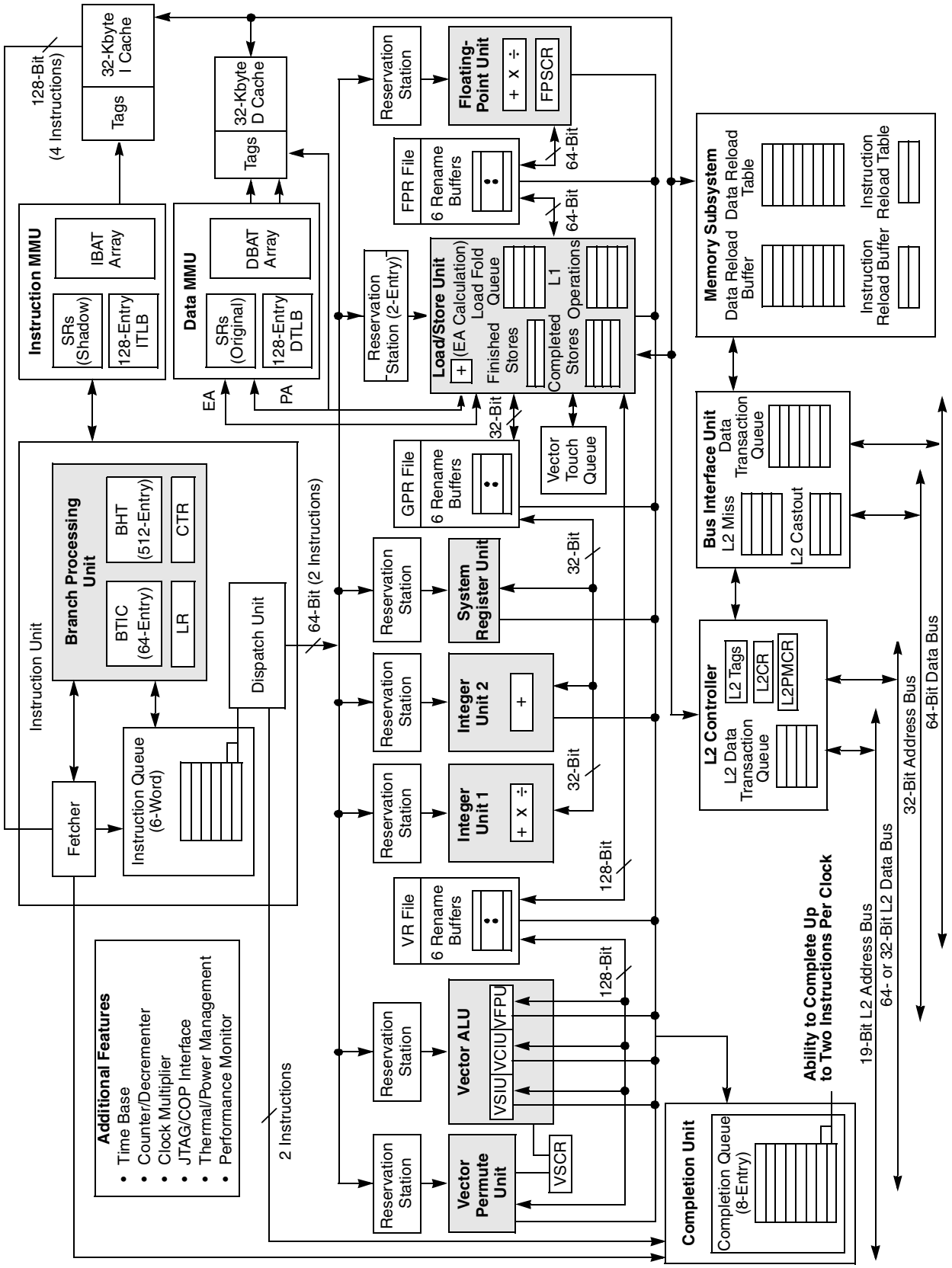


Figure 1. MPC7410 Block Diagram

- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754™ single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Maximum Value	Unit	Notes
Rework temperature	T_{rwk}	260	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.8 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

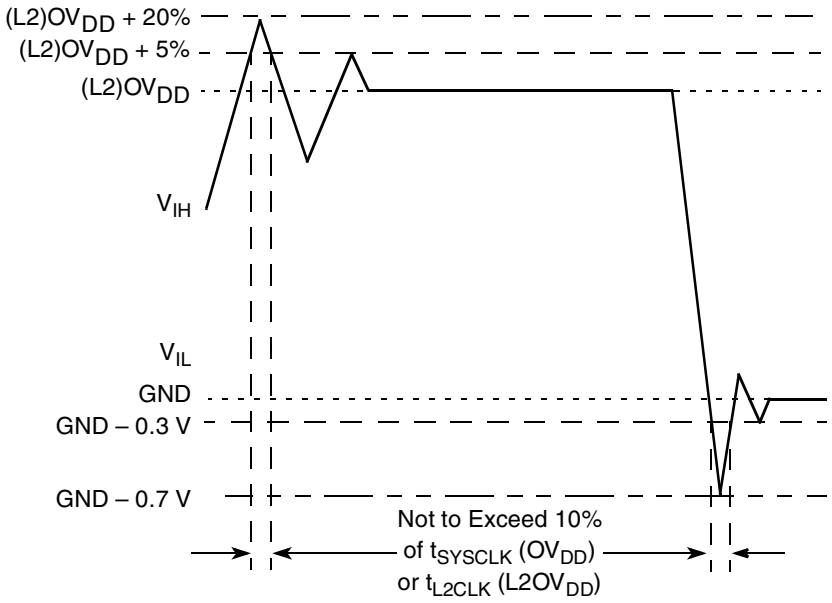


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 8. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
Input setup	t_{IVKH}	1.0	—	ns	4
Input hold	t_{IXKH}	0	—	ns	4
Output valid times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSV} t_{KHARV} t_{KHOV}	 — — —	 3.0 2.3 3.0	ns	5, 6
Output hold times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	5
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	9
SYSCLK to output high impedance (all except $\overline{ABB}$/$\overline{AMON}$(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/$\overline{DMON}$(0), $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{ABB}$/$\overline{AMON}$(0), $\overline{DBB}$/$\overline{DMON}$(0) high impedance after precharge	t_{KHABPZ}	—	1	t_{SYSCLK}	3, 7, 9
Maximum delay to $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 8, 9

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

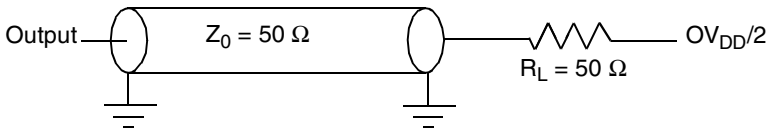


Figure 4. AC Test Load

4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 14 for example core and L2 frequencies at various divisors. Table 9 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC7410 to synchronize L2CLK_OUT at the SRAM with the processor's internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Freescale Application Note AN1794, *Backside L2 Timing Analysis for the PCB Design Engineer.*

The minimum L2CLK frequency in Table 9 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor that results in an L2 frequency below this minimum, or the L2CLK_OUT signals provided for SRAM clocking will not be phase-aligned with the MPC7410 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 9 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC7410 will be a function of the AC timings of the MPC7410, the AC timings for the SRAM, bus loading, and printed-circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies in Table 9. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of two or greater.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings in Table 10 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase-alignment with the internal L2CLK, the signals in Table 10 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	133	400	133	400	133	400	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	7.5	2.5	7.5	2.5	7.5	ns	—
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		50		%	2
Internal DLL-relock time	—	640	—	640	—	640	—	L2CLK	3
DLL capture window	—	0	10	0	10	0	10	ns	5
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	—	50	—	50	ps	6

Table 9. L2CLK Output AC Timing Specifications (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK_OUT output jitter	—	—	±150	—	±150	—	±150	ps	6

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2CLK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 7.

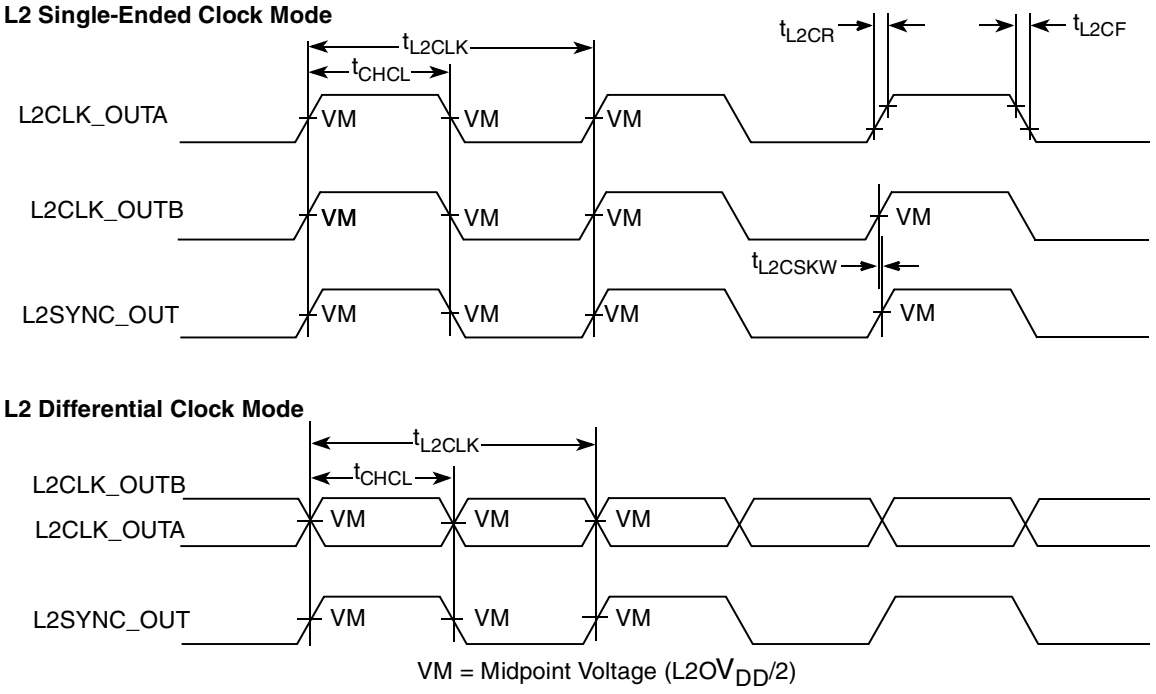


Figure 7. L2CLK_OUT Output Timing Diagram

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

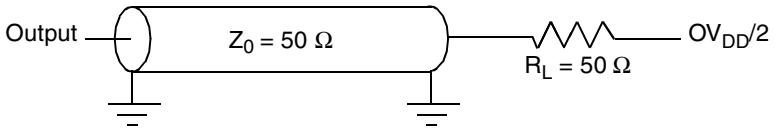


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

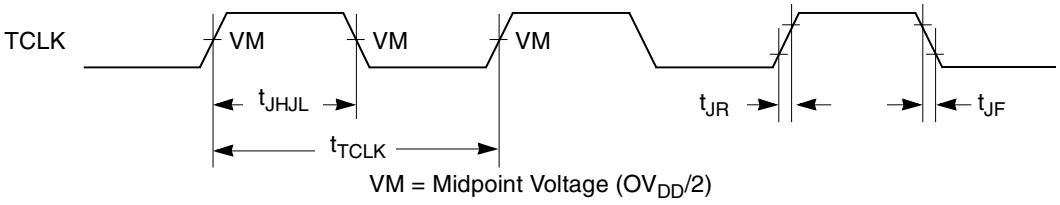


Figure 12. JTAG Clock Input Timing Diagram

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	BVSEL	—
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	BVSEL	—
$\overline{\text{DRDY}}$	K9	Low	Output	BVSEL	6, 8, 13
$\overline{\text{DBWO}}$ DTI[0]	D1	Low	Input	BVSEL	—
DTI[1:2]	H6, G1	High	Input	BVSEL	5, 10, 13
$\overline{\text{EMODE}}$	A3	Low	Input	BVSEL	7, 10
$\overline{\text{GBL}}$	B1	Low	I/O	BVSEL	—
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	N/A	—
$\overline{\text{HIT}}$	B5	Low	Output	BVSEL	6, 8
$\overline{\text{HRESET}}$	B6	Low	Input	BVSEL	—
$\overline{\text{INT}}$	C11	Low	Input	BVSEL	—
L1_TSTCLK	F8	High	Input	BVSEL	2
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	L2VSEL	—
L2ADDR[17:18]	K19,W19	High	Output	L2VSEL	8
$L2AV_{DD}$	L13	—	Input	V_{DD}	—
$\overline{\text{L2CE}}$	P17	Low	Output	L2VSEL	—
L2CLK_OUTA	N15	High	Output	L2VSEL	—
L2CLK_OUTB	L16	High	Output	L2VSEL	—
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	L2VSEL	—
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	L2VSEL	—
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15	—	—	N/A	11
L2SYNC_IN	L14	High	Input	L2VSEL	—
L2SYNC_OUT	M14	High	Output	L2VSEL	—
L2_TSTCLK	F7	High	Input	BVSEL	2

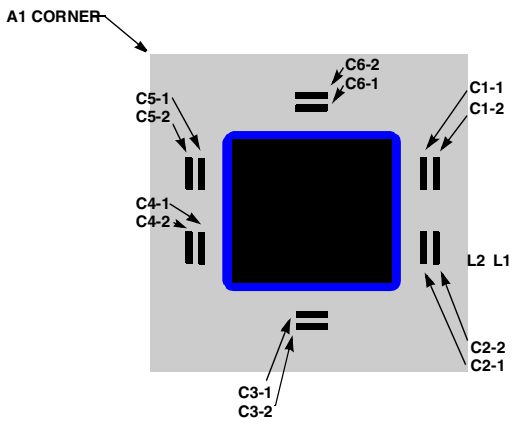
7.5 Package Parameters for the MPC7410, 360 HCTE_LGA

The package parameters are as listed here. The package type is the 25 × 25 mm, 360 high coefficient of thermal expansion LGA package (HCTE_LGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 land array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3ppm/°C

7.6 Substrate Capacitors for the MPC7410

Figure 20 shows the connectivity of the substrate capacitor pads for the MPC7410, 360 CBGA and 360 HCTE packages.



Package Caps	Value µF	Voltage Reference
C1-1	0.01	$L2OV_{DD}$
C1-2		GND
C2-1	0.01	$L2OV_{DD}$
C2-2		GND
C3-1	0.01	V_{DD}
C3-2		GND
C4-1	0.01	OV_{DD}
C4-2		GND
C5-1	0.01	OV_{DD}
C5-2		GND
C6-1	0.01	V_{DD}
C6-2		GND

Figure 20. Substrate Bypass Capacitors for the MPC7410

8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC7410.

8.1 PLL Configuration

The MPC7410 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7410 is shown in Table 13 for example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the minimum and maximum core frequencies listed in Table 8.

Table 13. MPC7410 Microprocessor PLL Configuration

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0100	2x	2x	—	—	—	—	—	—	—
0110	2.5x	2x	—	—	—	—	—	—	—
1000	3x	2x	—	—	—	—	—	—	400 (800)
1110	3.5x	2x	—	—	—	—	—	350 (700)	465 (930)
1010	4x	2x	—	—	—	—	—	400 (800)	—

the MPC7410 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode can be enabled (see the *MPC7410 RISC Microprocessor Family Users' Manual* for more information on this mode), or these signals may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

In systems where $\overline{\text{GBL}}$ is not connected and other devices may be asserting $\overline{\text{TS}}$ for a snoopable transaction while not driving $\overline{\text{GBL}}$ to the processor, we recommend that a strong (1 kΩ) pull-up resistor be used on $\overline{\text{GBL}}$. Note that the MPC7410 will only snoop transactions when $\overline{\text{GBL}}$ is asserted.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If parity checking is disabled through HID0, and parity generation is not required by the MPC7410 (note that the MPC7410 always generates parity), then all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

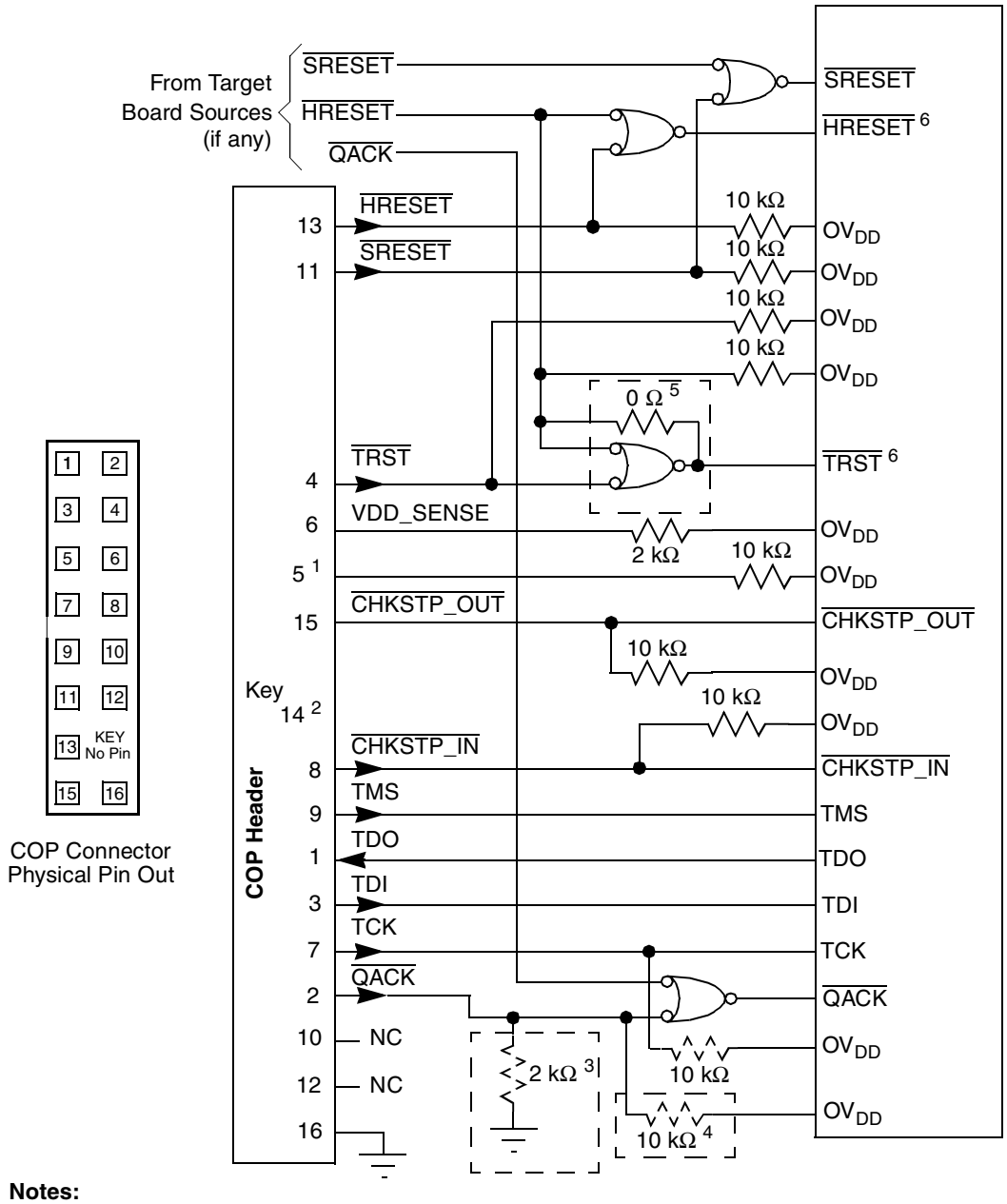
8.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 25 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 25, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 25 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7410. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 25. COP Connector Diagram

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 25; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 25 is usually connected to the PCI bridge chip in a system and is an input to the MPC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

8.8 Thermal Management Information

This section provides thermal management information for the MPC7410 for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods such as spring clip to holes in the printed circuit board or with screws and springs to the printed circuit board; see Figure 26 for the BGA package and Figure 27 for the LGA package. This spring force should not exceed 5.5 pounds of force. Note that care should be taken to avoid focused forces being applied to die corners and/or edges when mounting heat sinks.

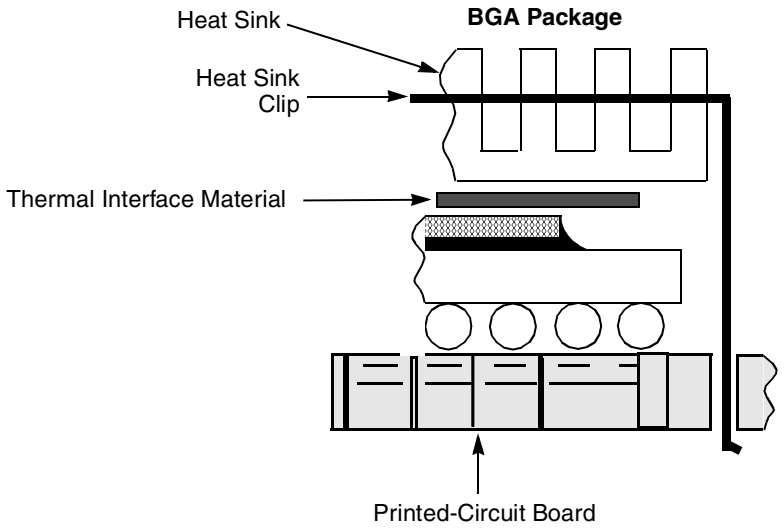


Figure 26. BGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

8.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
θ_{jc} is the junction-to-case thermal resistance
θ_{int} is the adhesive or interface material thermal resistance
θ_{sa} is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package θ_{jc} = 0.03, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 30.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.03°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 75°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

9 Document Revision History

Table 16 provides a revision history for this hardware specification.

Table 16. Document Revision History

Revision	Date	Substantive Change(s)
6.1	11/16/2007	Updated Table 17 and Table 19 to show the VU package is available as an MC prefix device compared to an MPC prefix for the other package types; this was done to match the specification documents with the device ordering and part marking information. Updated title of Table 19 to reflect correct name of referenced document and updated respective document order information below table. Updated notes in Table 1–Table 3 replacing references to MPC7410RX*nnn*LE with M*xx*7410*xxnnn*LE since notes to apply to all the available packages types.
6	8/14/2007	Updated Table 4 thermal information: • Deleted rows on single-layer (1s) boards. • CBGA package $R_{\theta JMA}$ for natural convection for four layer boards changed from 17 to 18 °C/W. • HCTE package $R_{\theta JMA}$ for natural convection for four layer boards changed from 22 to 20 °C/W. • HCTE package $R_{\theta JMA}$ for 200 ft./min airflow for four layer boards changed from 19 to 16 °C/W with airflow rate specification changed from 200 ft./min to 1 m/sec. • HCTE package $R_{\theta JMA}$ for 400 ft./min airflow for four layer boards changed from 18 to 15 °C/W with airflow rate specification changed from 400 ft./min to 2 m/sec. • CBGA package $R_{\theta JB}$ changed from 8 to 9°C/W. • HCTE package $R_{\theta JB}$ changed from 14 to 11°C/W. • Table 4 Notes 2 - 4 have been revised and updated; Note 5 is no longer used. Notes on table rows have been renumbered. Updated Figure 26 removing optional heat sink clip to package. Removed references in document to adhesive attached thermal solutions. Updated thermal solution vendor information in Section 8.8. Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information to document: • Added Section 7.2, “Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres). • Added Figure 18 for HCTE_CBGA Lead Free C5 Spheres package, similar to Figure 17 but with differences in dimensions A, A1, and b in the figure’s dimension table. • Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information in Table 17 and Table 19. • Changed part marking example in Figure 31 to an HCTE_CBGA device.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
0.3	—	Added 3.3 V support on the processor bus (BVSEL).
		Table 7—update typical and maximum power numbers for full-on mode in. Removed note 4. Reworded notes 2 and 3.
		Table 9, Note 2—removed reference to application note.
		Figure 17—corrected side view datum A to be datum C.
		Section 1.8.7—added $\overline{CI}$ and $\overline{WT}$ to transfer attribute signals requiring pull-ups.
		Section 1.8.7—added 1-kΩ pull-up recommendation to $\overline{GBL}$ when $\overline{GBL}$ is not connected.
		Table 2— added pull-down resistance necessary for internally pulled-up voltage select pins. Added 3.3-V support for BVSEL.
		Table 13—added note 14 for BVSEL, L2VSEL, and $\overline{TRST}$ pins to address pull-down resistance necessary for these internally pulled-up pins to recognize a low signal.
		Table 6—lowered 2.5 V CV_{IH} from 2.2 to 2.0 V to be compatible with V_{OH} of the MPC107. Added support for 3.3-V processor bus.
		Table 15—modified note 1, use L2CR[L2SL] for L2CLK frequency less than 150 MHz.
		Table 8—revised note 2 discussing for 3.3-V bus voltage support.
		Table 14—added note 5, do not use PL off during power-up sequence.
		Table 1—update output hold times (t_{L2CHOX}).
0.2	—	Corrected Section 1.3—technology from 0.13 µm to 0.18 µm.
		Updated Table 7—adds power consumption numbers; adds note on estimated decrease w/o AltiVec.
		Updated Table 8—adds minimum values for processor frequency and VCO frequency.
		Updated Table 9—input setup, output valid times, output hold times, SYSCLK to output high impedance.
		Updated Table 11—L2SYNC_IN to high impedance.
		Updated Figure 17—mechanical dimensions, adds capacitor pad dimensions.
0.1	—	Minor updates.
0	—	Initial release.

10 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 10.1, “Part Numbers Addressed by This Specification.” Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

10.1 Part Numbers Addressed by This Specification

Table 17 provides the Freescale part numbering nomenclature for the MPC7410 Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 17. Part Numbering Nomenclature

Mxx	**7410**	***xx***	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Package [1]**	**Processor Frequency [2]**	**Application Modifier**	**Revision Level**
MPC	7410	RX = CBGA	400 450 500	L: 1.8 V ± 100 mV 0° to 105°C	C: 1.2; PVR = 800C 1102 D: 1.3; PVR = 800C 1103 E: 1.4; PVR = 800C 1104
		HX = HCTE_CBGA			E: 1.4; PVR = 800C 1104
		VS = HCTE_LGA			
MC		VU = HCTE_CBGA (Lead Free C5 Solder Spheres)	400 500		

Notes:

1. See Section 7, “Package Description,” for more information on available package types and Table 4 for more information on thermal characteristics.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document, as described in the following tables.

Table 18. Part Numbers Addressed by MPC7410RXnnnPx Series Part Number Specifications

MPC	7410	RX	*nnn*	P	*x*

Product Code	Part Identifier	Package	Processor Frequency[1]	Application Modifier	Revision Level
MPC	7410	RX = CBGA	450 500 550	P: 2.0 V ± 50 mV 0° to 65°C	C: 1.2; PVR = 800C 1102 [1] D: 1.3; PVR = 800C 1103 [2] E: 1.4; PVR = 800C 1104 [3]

Notes: Document order numbers:
1. MPC7410PCPNS.
2. MPC7410PDPNS.
3. MPC7410PEPNS.

Table 19. Part Numbers Addressed by MPC7410 RISC Microprocessor HardwareSpecifications Addendum for the MPC7410xxnnnNE Series

Mxx	7410	xx	*nnn*	N	E

Product Code	Part Identifier	Package	Processor Frequency [1]	Application Modifier	Revision Level
MPC	7410	RX = CBGA	400 450 500	N: 1.5 V ± 50 mV	E: 1.4; PVR = 800C 1104
		HX = HCTE_CBGA VS = HCTE_LGA	400 450		
MC		VU = HCTE_CBGA (Lead Free C5 Solder Spheres)			

Note: Document order number: MPC7410ECS02AD

Table 20. Part Numbers Addressed by MPC7410TRXnnnNE Part Number Specification

MPC	7410	T	RX	*nnn*	N	E

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency[1]	Application Modifier	Revision Level
MPC	7410	T: –40° to 105°C	RX = CBGA	400 450	N: 1.5 V ±50 mV	E: 1.4; PVR = 800C 1104

Note: Document order number: MPC7410TRXNEPNS.

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