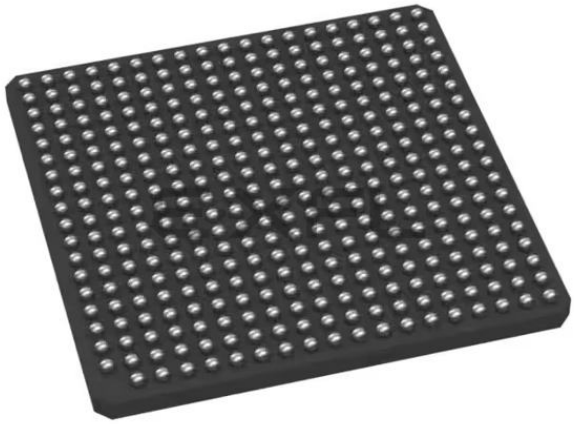

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	450MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7410vu450ne

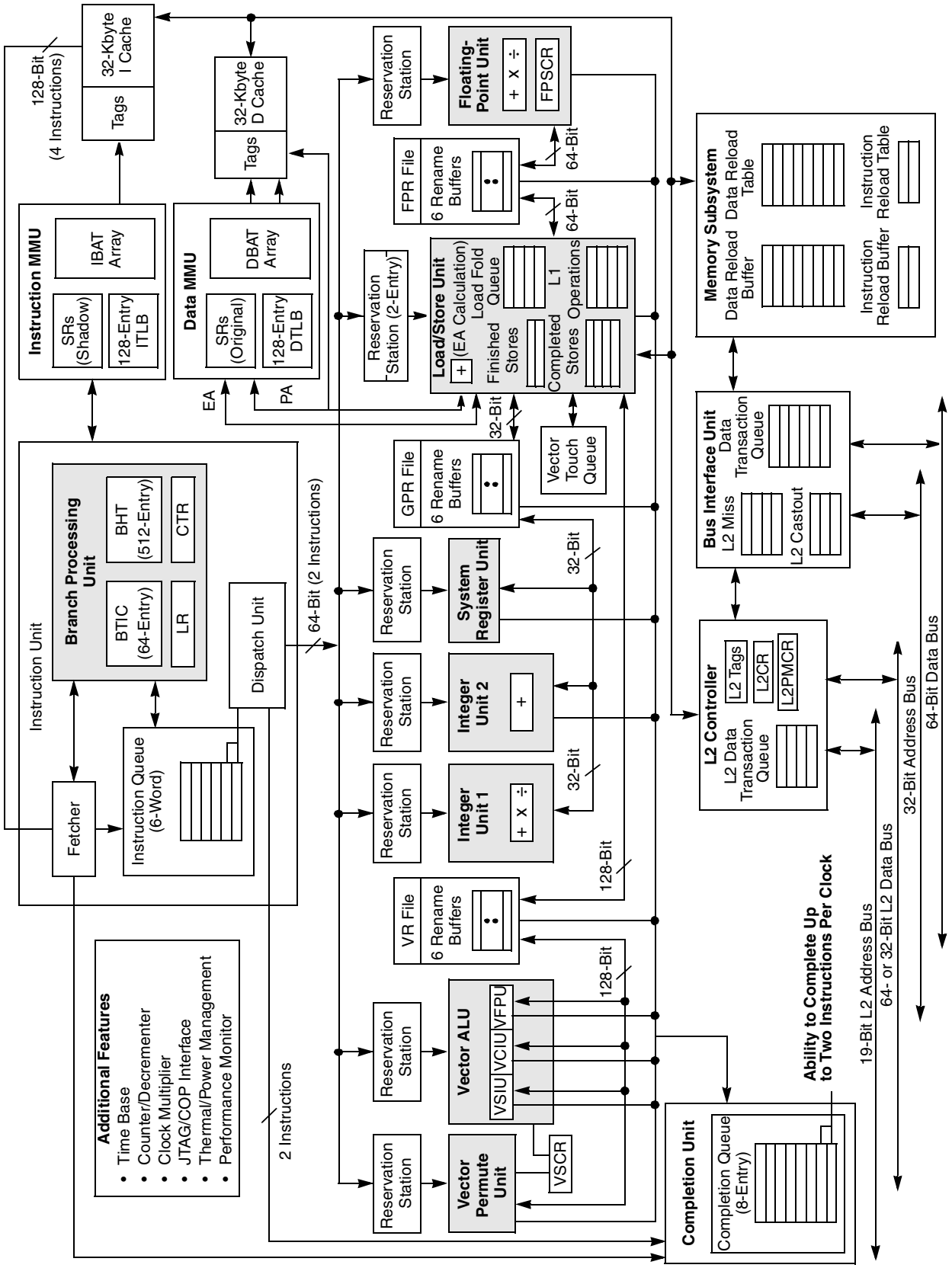


Figure 1. MPC7410 Block Diagram

3 General Parameters

The following list provides a summary of the general parameters of the MPC7410:

Technology	0.18 µm CMOS, six-layer metal
Die size	6.32 mm × 8.26 mm (52 mm^2)
Transistor count	10.5 million
Logic design	Fully static
Packages	Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array (HCTE_CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array with lead free C5 spheres (HCTE_CBGA Lead Free C5 Spheres) Surface mount 360 high coefficient of thermal expansion ceramic land grid array (HCTE_LGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 3 for recommended operating conditions)
I/O power supply	1.8 V ± 100 mV DC or 2.5 V ± 100 mV 3.3 V ± 165 mV (system bus only) (input thresholds are configuration pin selectable)

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7410.

4.1 DC Electrical Characteristics

The tables in this section describe the MPC7410 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.1	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.1	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.1	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3, 6
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 2.8	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.2 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	—
Storage temperature range		T_{stg}	–55 to 150	°C	—

Table 4. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	< 0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active portion of the die and the calculated case temperature at the top of the die. The actual value of R JC is less than 0.1 °C/W.

Note: Refer to Section 8.8, "Thermal Management Information," for details on thermal management.

Table 5 provides the DC electrical characteristics for the MPC7410.

Table 5. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8	V_{IH}	$0.65 \times (L2)OV_{DD}$	$(L2)OV_{DD} + 0.2$	V	2, 3, 8
	2.5	V_{IH}	1.7	$(L2)OV_{DD} + 0.2$		
	3.3	V_{IH}	2.0	$OV_{DD} + 0.3$		
Input low voltage (all inputs except SYSCLK)	1.8	V_{IL}	–0.3	$0.35 \times (L2)OV_{DD}$	V	8
	2.5	V_{IL}	–0.3	$0.2 \times (L2)OV_{DD}$		
	3.3	V_{IL}	–0.3	0.8		
SYSCLK input high voltage	1.8	CV_{IH}	1.5	$OV_{DD} + 0.2$	V	2, 8
	2.5	CV_{IH}	2.0	$OV_{DD} + 0.2$		
	3.3	CV_{IH}	2.4	$OV_{DD} + 0.3$		
SYSCLK input low voltage	1.8	CV_{IL}	–0.3	0.2	V	8
	2.5	CV_{IL}	–0.3	0.4		
	3.3	CV_{IL}	–0.3	0.4		
Input leakage current, $V_{in} = L2OV_{DD}/OV_{DD}$	1.8	I_{in}	—	20	µA	2, 3, 6, 7
	2.5	I_{in}	—	35		
	3.3	I_{in}	—	70		

4.2.1 Clock AC Specifications

Table 7 provides the clock AC timing specifications as defined in Figure 3.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		400 MHz		450 MHz		500 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	350	400	350	450	350	500	MHz	1
VCO frequency	f_{VCO}	700	800	700	900	700	1000	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	133	33	133	33	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	7.5	30	ns	—
SYSCLK rise and fall time	t_{KR} and t_{KF}	—	0.5	—	0.5	—	0.5	ns/V	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter	—	—	±150	—	±150	—	±150	ps	4
Internal PLL-relock time	—	—	100	—	100	—	100	µs	5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurement are determined by the slew rates of the bus interface, rather than by time. As a result, the 0.5 ns rise/fall time spec of the 1.8- and 2.5-V bus interfaces is equivalent to the 1 ns rise/fall time of the 3.3-V bus interface. Both interfaces required a 2 V/ns slew rate. The slew rate is measured as a 1-V change (from 0.2 to 1.2 V) in 0.5 ns for the 1.8- and 2.5-V bus interfaces, whereas the 3.3-V bus interface required a 2-V change (from 0.4 to 2.4 V) in 1 ns.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short- and long-term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

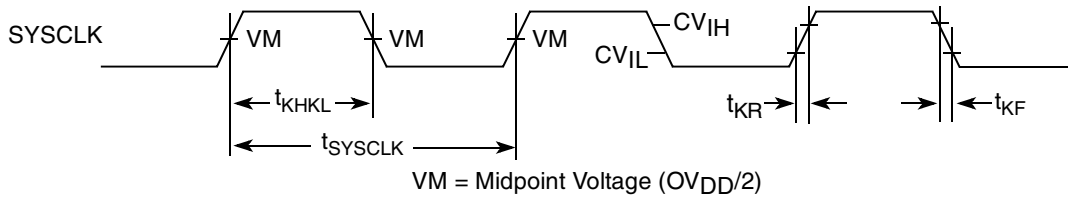


Figure 3. SYSCLK Input Timing Diagram

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

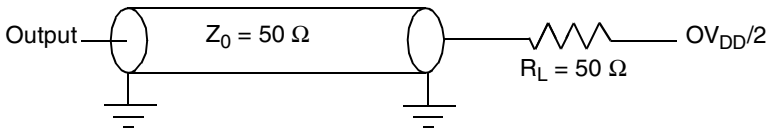


Figure 4. AC Test Load

Figure 8 shows the L2 bus input timing diagrams for the MPC7410.

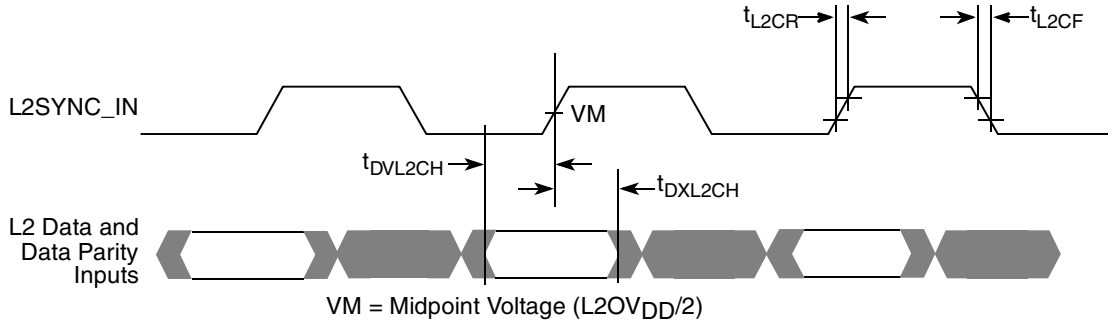


Figure 8. L2 Bus Input Timing Diagrams

Figure 9 shows the L2 bus output timing diagrams for the MPC7410.

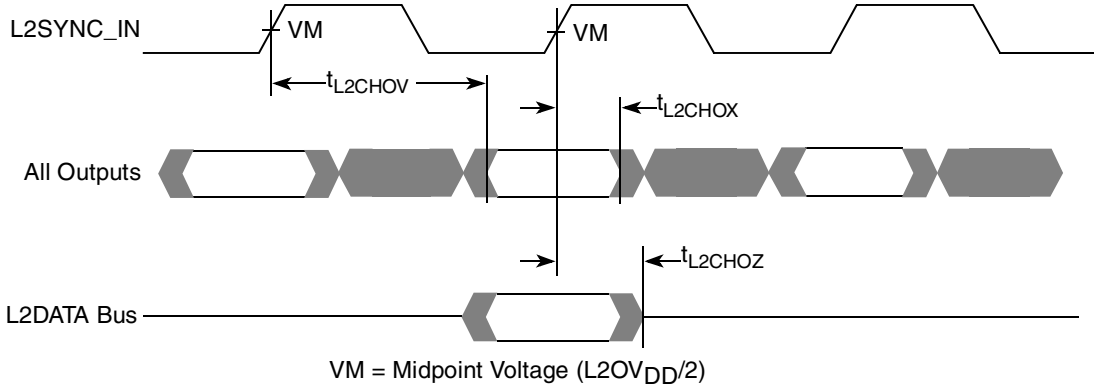


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC7410.

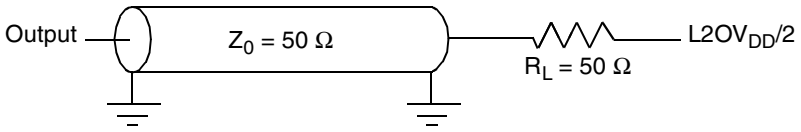


Figure 10. AC Test Load for the L2 Interface

4.2.5 IEEE 1149.1 AC Timing Specifications

Table 11 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	—
TCK cycle time	t_{TCLK}	30	—	ns	—
TCK clock pulse width measured at $OV_{DD}/2$	t_{JHJL}	15	—	ns	—
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	—

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

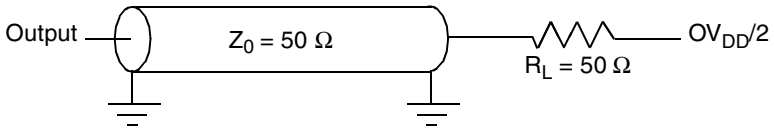


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

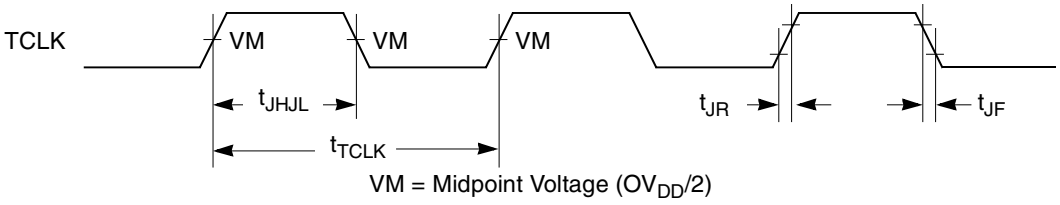


Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

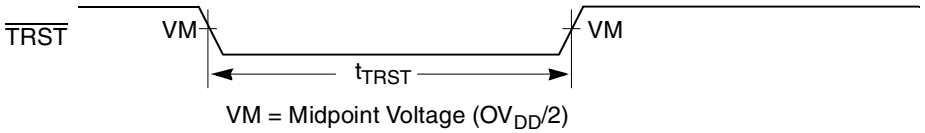


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

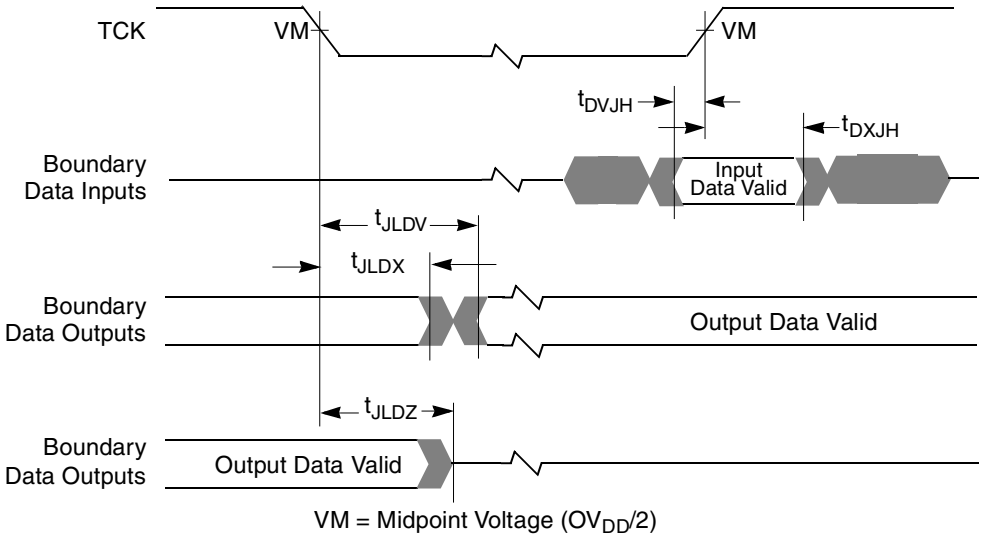


Figure 14. Boundary-Scan Timing Diagram

Figure 15 provides the test access port timing diagram.

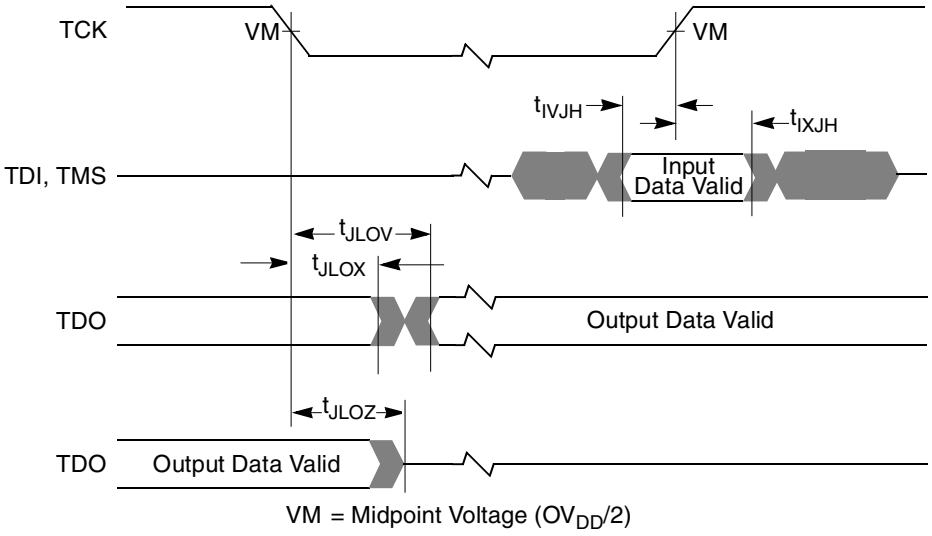


Figure 15. Test Access Port Timing Diagram

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
L2VSEL	A19	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{L2WE}}$	N16	Low	Output	L2VSEL	—
L2ZZ	G17	High	Output	L2VSEL	—
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	BVSEL	2
$\overline{\text{MCP}}$	B11	Low	Input	BVSEL	15
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	N/A	—
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	BVSEL	4
$\overline{\text{QACK}}$	B2	Low	Input	BVSEL	—
$\overline{\text{QREQ}}$	J3	Low	Output	BVSEL	—
$\overline{\text{RSRV}}$	D3	Low	Output	BVSEL	—
$\overline{\text{SHD0}}$	B3	Low	I/O	BVSEL	8
$\overline{\text{SHD1}}$	B4	Low	I/O	BVSEL	5, 8
$\overline{\text{SMI}}$	A12	Low	Input	BVSEL	—
$\overline{\text{SRESET}}$	E10	Low	Input	BVSEL	—
SYSCLK	H9	—	Input	BVSEL	—
$\overline{\text{TA}}$	F1	Low	Input	BVSEL	—
TBEN	A2	High	Input	BVSEL	—
$\overline{\text{TBST}}$	A11	Low	Output	BVSEL	—
TCK	B10	High	Input	BVSEL	—
TDI	B7	High	Input	BVSEL	9
TDO	D9	High	Output	BVSEL	—
$\overline{\text{TEA}}$	J1	Low	Input	BVSEL	—
TMS	C8	High	Input	BVSEL	9
$\overline{\text{TRST}}$	A10	Low	Input	BVSEL	9
$\overline{\text{TS}}$	K7	Low	I/O	BVSEL	—
TSIZ[0:2]	A9, B9, C9	High	Output	BVSEL	—
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	BVSEL	—
$\overline{\text{WT}}$	C3	Low	I/O	BVSEL	—

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7410, 360 CBGA and 360 HCTE packages.

7.1 Package Parameters for the MPC7410, 360 CBGA and 360 HCTE_CBGA

The package parameters are as provided in the following list. The package types are the 25 × 25 mm, 360-lead ceramic ball grid array package (CBGA) or the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package (HCTE_CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	6.8 ppm/°C (CBGA) 12.3ppm/°C (HCTE_CBGA)

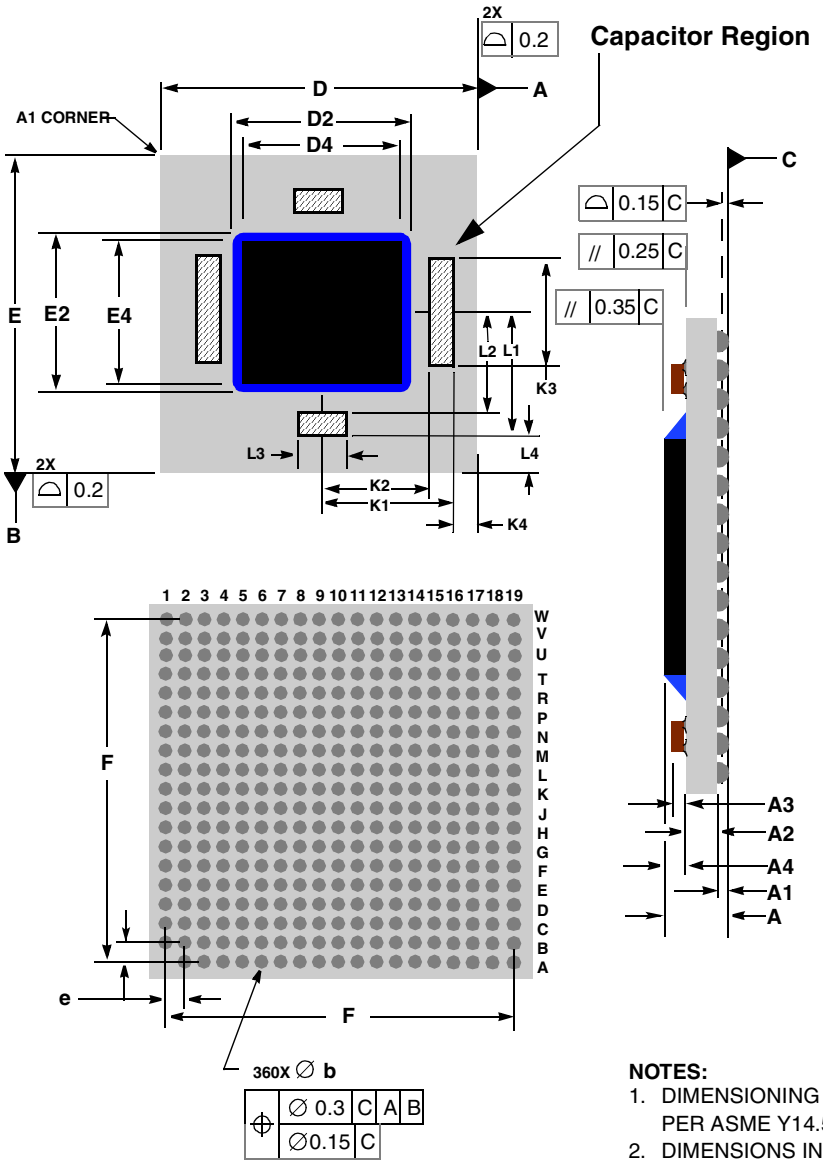
7.2 Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres)

The package parameters are as listed here. The package types are the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package with lead-free C5 spheres (HCTE_CBGA lead-free spheres).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.76 mm (30 mil)
Coefficient of thermal expansion	12.3ppm/°C

7.3 Mechanical Dimensions for the MPC7410, 360 CBGA and 360 HCTE_CBGA

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 CBGA and 360 HCTE_CBGA packages.



	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1.00
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.90
b	0.82	0.93
D	25.00 BSC	
D2	—	12.50
D4	6.00	9.00
e	1.27 BSC	
E	25.00 BSC	
E2	—	14.30
E4	8.00	11.00
F	22.86 BSC	
K1	—	9.75
K2	6.46	—
K3	8.20	8.60
K4	2.75	—
L1	—	9.50
L2	6.94	—
L3	3.10	3.30
L4	3.00	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410, 360 CBGA and 360 HCTE_CBGA Packages

Table 13. MPC7410 Microprocessor PLL Configuration (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0111	4.5x	2x	—	—	—	—	375 (750)	450 (900)	—
1011	5x	2x	—	—	—	375 (750)	416 (833)	500 (1000)	—
1001	5.5x	2x	—	—	366 (733)	412 (825)	458 (916)	—	—
1101	6x	2x	—	—	400 (800)	450 (900)	500 (1000)	—	—
0101	6.5x	2x	—	—	433 (866)	488 (967)	—	—	—
0010	7x	2x	—	350 (700)	466 (933)	—	—	—	—
0001	7.5x	2x	—	375 (750)	500 (1000)	—	—	—	—
1100	8x	2x	—	400 (800)	—	—	—	—	—
0000	9x	2x	—	450 (900)	—	—	—	—	—
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL off		PLL off, no core clocking occurs						

Notes:

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and third-party emulator tool development only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7410 regardless of the SYSCLK input.
5. PLL-off mode should not be used during chip power-up sequencing.

The MPC7410 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC7410. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC7410 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used; the remainder of the L2 interface may be left unterminated.

8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 23).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the driver impedance measurement circuit described above.

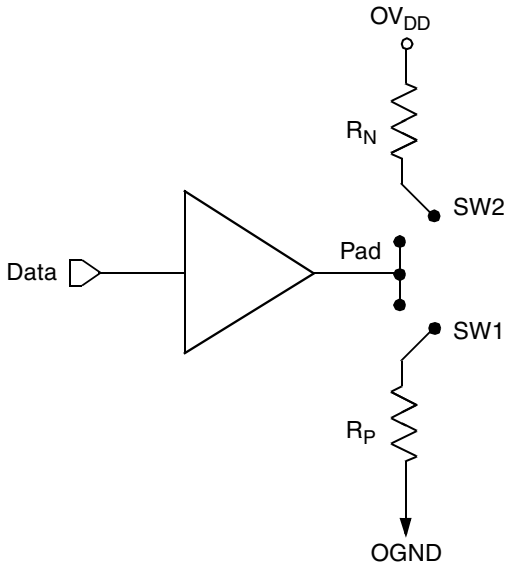


Figure 23. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 24. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 24 describes the alternate driver impedance measurement circuit.

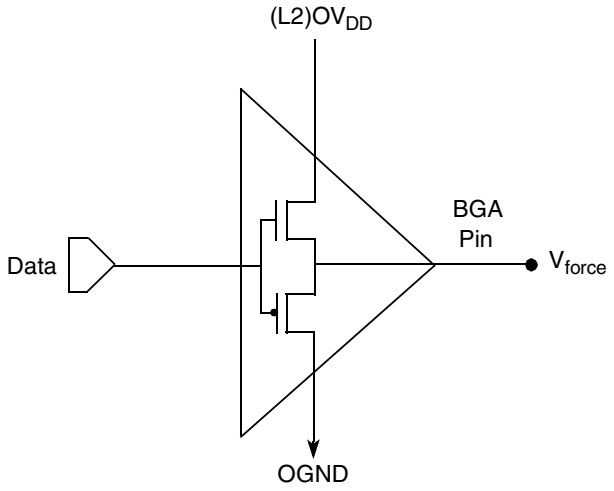


Figure 24. Alternate Driver Impedance Measurement Circuit

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.8 V, OV_{DD} = 2.5 V, T_j = 0° – 105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5–54.3	42.7–54.1	Z_0	Ω
R_P	37.3–55.3	39.3–50.0	Z_0	Ω

8.6 Pull-Up Resistor Requirements

The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 25; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 25 is usually connected to the PCI bridge chip in a system and is an input to the MPC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

8.8 Thermal Management Information

This section provides thermal management information for the MPC7410 for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods such as spring clip to holes in the printed circuit board or with screws and springs to the printed circuit board; see Figure 26 for the BGA package and Figure 27 for the LGA package. This spring force should not exceed 5.5 pounds of force. Note that care should be taken to avoid focused forces being applied to die corners and/or edges when mounting heat sinks.

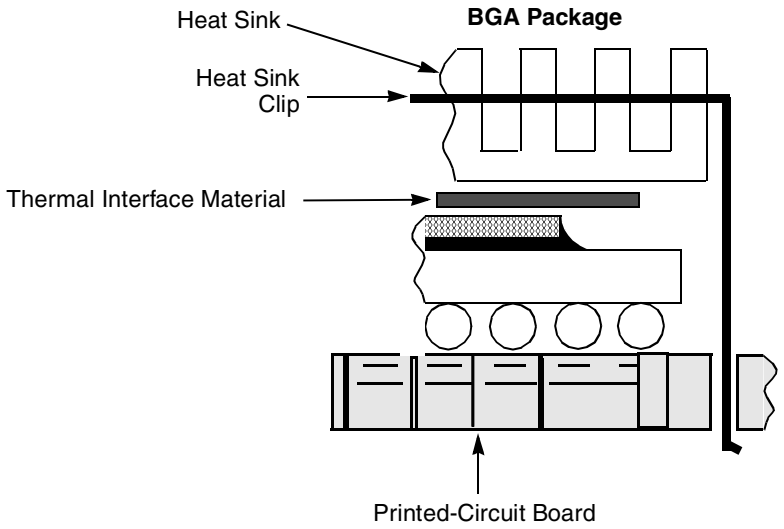


Figure 26. BGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1.1	—	Internal release.
		Table 12—added note 16 for $\overline{\text{ABB}}$/$\overline{\text{AMON}}$ and $\overline{\text{DBB}}$/$\overline{\text{DMON}}$ signal clarification.
		Table 12—changed $\overline{\text{CHK}}$ note 4 reference to note 2, signal is for factory test only. Changed previous note 4 ($\overline{\text{CHK}}$ related) to now provide additional PLL info.
		Table 1—modified maximum value for OV_{DD} from –0.3 to 3.465 to now be –0.3 to 3.6 and $L2OV_{DD}$ from –0.3 to 2.6 to now be –0.3 to 2.8. Modified note 6, OV_{DD} for revisions prior to Rev. 1.4 have maximum value for OV_{DD} of –0.3 to 2.8.
		Table 8—removed note 12. L2_TSTCLK is for factory use only (see Table 12, note 2).
		Section 1.10.2—revised section to include nomenclature tables for part markings not covered by this spec.
		Figure 2—added that under/overshoot for $L2OV_{DD}$ references t_{L2CLK} while OV_{DD} references t_{SYSCLK}.
		Table 4—added HCTE package (HX package descriptor) thermal characteristics.
		Section 1.5—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same pin assignments.
		Section 1.6—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same pinout listings.
		Section 1.7—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same package parameters and dimensions.
		Table 17—added HCTE package (HX package descriptor) to part numbering nomenclature.
		Table 21—added MPC7410THXnnnLE extended temperature HCTE package part numbers and part number specification document reference.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1.0	—	Section 1.3 and Table 3—revised OV_{DD} from 3.3 V ± 100 mV to 3.3 V ± 165 mV.
		Table 13—removed unsupported PLL configurations.
		Table 12—added note 15 for minimum $\overline{MCP}$ pulse width, correct note 3 for 3.3-V processor bus support.
		Table 13—revised note 3 to include emulator tool development.
		Table 14—removed unsupported Core-to-L2 example frequencies.
		Section 1.8.8—updated heat sink vendors list.
		Section 1.8.8.2—updated interface vendors list.
		Table 1—updated voltage sequencing requirements notes 3 and 4.
		Table 4—Updated/added thermal characteristics.
		Table 5—removed table and TAU related information, TAU is no longer supported.
		Table 6—updated I_{in} and I_{TSI} leakage current specs.
		Section 1.8.3—removed section.
		Section 1.10—reformatted section.
		Section 1.8.6—changed recommended pull-up resistor value to 1 kW–5 kW. Added $\overline{AACK}$, $\overline{TEA}$, and $\overline{TS}$ to control signals needing pull-ups. Added pull-up resistor value recommendation for L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$ factory test signals.
		Section 1.8.7—revised text regarding connection of $\overline{TRST}$. Combined Figure 22, Figure 23, and Table 17, into Figure 21.
		Table 7—corrected min VCO frequencies from 450 to 700 MHz to match min processor frequency of 350 MHz.
		Table 2—added note 3 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V OV_{DD}.
		Table 3—added notes 5 and 6 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V OV_{DD}.
		Table 5—added note 8 regarding DC voltage limits for JTAG signals.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
0.3	—	Added 3.3 V support on the processor bus (BVSEL).
		Table 7—update typical and maximum power numbers for full-on mode in. Removed note 4. Reworded notes 2 and 3.
		Table 9, Note 2—removed reference to application note.
		Figure 17—corrected side view datum A to be datum C.
		Section 1.8.7—added $\overline{CI}$ and $\overline{WT}$ to transfer attribute signals requiring pull-ups.
		Section 1.8.7—added 1-kΩ pull-up recommendation to $\overline{GBL}$ when $\overline{GBL}$ is not connected.
		Table 2— added pull-down resistance necessary for internally pulled-up voltage select pins. Added 3.3-V support for BVSEL.
		Table 13—added note 14 for BVSEL, L2VSEL, and $\overline{TRST}$ pins to address pull-down resistance necessary for these internally pulled-up pins to recognize a low signal.
		Table 6—lowered 2.5 V CV_{IH} from 2.2 to 2.0 V to be compatible with V_{OH} of the MPC107. Added support for 3.3-V processor bus.
		Table 15—modified note 1, use L2CR[L2SL] for L2CLK frequency less than 150 MHz.
		Table 8—revised note 2 discussing for 3.3-V bus voltage support.
		Table 14—added note 5, do not use PL off during power-up sequence.
		Table 1—update output hold times (t_{L2CHOX}).
0.2	—	Corrected Section 1.3—technology from 0.13 µm to 0.18 µm.
		Updated Table 7—adds power consumption numbers; adds note on estimated decrease w/o AltiVec.
		Updated Table 8—adds minimum values for processor frequency and VCO frequency.
		Updated Table 9—input setup, output valid times, output hold times, SYSCLK to output high impedance.
		Updated Table 11—L2SYNC_IN to high impedance.
		Updated Figure 17—mechanical dimensions, adds capacitor pad dimensions.
0.1	—	Minor updates.
0	—	Initial release.

10 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 10.1, “Part Numbers Addressed by This Specification.” Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

10.1 Part Numbers Addressed by This Specification

Table 17 provides the Freescale part numbering nomenclature for the MPC7410 Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 17. Part Numbering Nomenclature

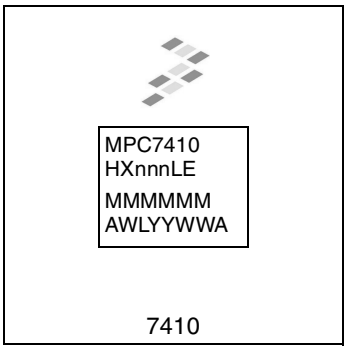
Mxx	**7410**	***xx***	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Package [1]**	**Processor Frequency [2]**	**Application Modifier**	**Revision Level**
MPC	7410	RX = CBGA	400 450 500	L: 1.8 V ± 100 mV 0° to 105°C	C: 1.2; PVR = 800C 1102 D: 1.3; PVR = 800C 1103 E: 1.4; PVR = 800C 1104
		HX = HCTE_CBGA			E: 1.4; PVR = 800C 1104
		VS = HCTE_LGA			
MC		VU = HCTE_CBGA (Lead Free C5 Solder Spheres)	400 500		

Notes:

1. See Section 7, “Package Description,” for more information on available package types and Table 4 for more information on thermal characteristics.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

10.3 Part Marking

Parts are marked as the example shown in Figure 31.



HCTE_CBGA

Notes:

MMMMMM is the 6-digit mask number.
AWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 31. Part Marking for HCTE_CBGA Device