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### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

### Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410hx400le

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- The MPC7410 is implemented in a next generation process technology for core frequency improvement.
- The MPC7410 floating-point unit has been improved to make latency equal for double- and single-precision operations involving multiplication.
- The completion queue has been extended to eight slots.
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750 four-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback).

Some comments on the MPC7410 with respect to the MPC7400:

- The MPC7410 adds configurable direct-mapped SRAM capability to the L2 cache interface.
- The MPC7410 adds 32-bit interface support to the L2 cache interface. The MPC7410 implements a 19th L2 address pin (L2ASPARE on the MPC7400) in order to support additional address range.
- The MPC7410 removes support for 3.3-V I/O on the L2 cache interface.

Figure 1 shows a block diagram of the MPC7410.

# 2 Features

This section summarizes features of the MPC7410 implementation of the PowerPC architecture. Major features of the MPC7410 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)



- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754<sup>™</sup> single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations



### **Electrical and Thermal Characteristics**

### Table 5. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage <sup>1</sup>	Symbol	Min	Мах	Unit	Notes
High-Z (off-state) leakage current,	1.8	I <sub>TSI</sub>	—	20 µA		2, 3,
$V_{in} = L2OV_{DD}/OV_{DD}$	2.5	I <sub>TSI</sub>	—	35		5, 7
	3.3	I <sub>TSI</sub>	_	70		
Output high voltage, I <sub>OH</sub> = -5 mA	1.8	V <sub>OH</sub>	(L2)OV <sub>DD</sub> - 0.45		V	8
	2.5	V <sub>OH</sub>	1.7			
	3.3	V <sub>OH</sub>	2.4			
Output low voltage, I <sub>OL</sub> = 5 mA	1.8	V <sub>OL</sub>	_	0.45	V	8
	2.5	V <sub>OL</sub>	_	0.4		
	3.3	V <sub>OL</sub>		0.4		
Capacitance, V <sub>in</sub> = 0 V, f = 1 MHz		C <sub>in</sub>		6.0	pF	3, 4, 7

### Notes:

- 1. Nominal voltages; see Table 3 for recommended operating conditions.
- 2. For processor bus signals, the reference is OV<sub>DD</sub> while L2OV<sub>DD</sub> is the reference for the L2 bus signals.
- 3. Excludes factory test signals.
- 4. Capacitance is periodically sampled rather than 100% tested.
- 5. The leakage is measured for nominal OV<sub>DD</sub> and L2OV<sub>DD</sub>, or both OV<sub>DD</sub> and L2OV<sub>DD</sub> must vary in the same direction (for example, both OV<sub>DD</sub> and L2OV<sub>DD</sub> vary by either +5% or -5%).
- 6. Measured at max OV<sub>DD</sub>/L2OV<sub>DD</sub>.
- 7. Excludes IEEE 1149.1 boundary scan (JTAG) signals.
- 8. For JTAG support: all signals controlled by BVSEL and L2VSEL will see V<sub>IL</sub>/V<sub>IH</sub>/V<sub>OL</sub>/V<sub>OH</sub>/CV<sub>IH</sub>/CV<sub>IL</sub> DC limits of 1.8 V mode while either the EXTEST or CLAMP instruction is loaded into the IEEE 1149.1 instruction register by the UpdateIR TAP state until a different instruction is loaded into the instruction register by either another UpdateIR or a Test-Logic-Reset TAP state. If only TSRT is asserted to the part, and then a SAMPLE instruction is executed, there is no way to control or predict what the DC voltage limits are. If HRESET is asserted before executing a SAMPLE instruction, the DC voltage limits will be controlled by the BVSEL/L2VSEL settings during HRESET. Anytime HRESET is not asserted (that is, just asserting TRST), the voltage mode is not known until either EXTEST or CLAMP is executed, at which time the voltage level will be at the DC limits of 1.8 V.



Table 6 provides the power consumption for the MPC7410.

	Proc	essor (CPU) Frequ	ency	11	Notes				
	400 MHz	450 MHz	500 MHz	Unit					
Full-On Mode									
Typical	4.2	4.7	5.3	W	1, 3				
Maximum	9.5	10.7 11.9 W		W	1, 2				
	Doze Mode								
Maximum	4.3	4.8	5.3	W	1				
	Nap	Mode							
Maximum	1.35	1.5	1.65	W	1				
	Slee	p Mode							
Maximum	1.3	1.45	1.6	W	1				
Sleep Mode—PLL and DLL Disabled									
Typical	600	600	600	mW	1				
Maximum	1.1	1.1	1.1	W	1				

### Table 6. Power Consumption for MPC7410

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power ( $OV_{DD}$  and  $L2OV_{DD}$ ) or PLL/DLL supply power ( $AV_{DD}$  and  $L2AV_{DD}$ ).  $OV_{DD}$  and  $L2OV_{DD}$  power is system dependent, but is typically <5% of  $V_{DD}$  power. Worst case power consumption for  $AV_{DD}$  = 15 mW and  $L2AV_{DD}$  = 15 mW.

2. Maximum power is measured at 105°C and V<sub>DD</sub> = 1.8 V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.

3. Typical power is an average value measured at 65°C and V<sub>DD</sub> = 1.8 V in a system while running typical benchmarks.

## 4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7410. After fabrication, functional parts are sorted by maximum processor core frequency, see Section 4.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL\_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, "Ordering Information."



### **Electrical and Thermal Characteristics**

## Table 8. Processor Bus AC Timing Specifications <sup>1</sup> (continued)

At recommended operating conditions (see Table 3)

Parameter		400, 450,	500 MHz	Unit	Notes
i araneter	Cymbol	Min	Max	Onit	Notes
SYSCLK to ARTRY, SHD0, SHD1 high impedance after precharge	t <sub>KHARPZ</sub>	_	2	t <sub>SYSCLK</sub>	3, 8, 9

### Notes:

- All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbology used for timing specifications herein follows the pattern of t<sub>(signal)(state)(reference)(state)</sub> for inputs and t<sub>(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>IVKH</sub> symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t<sub>KHOV</sub> symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
- 3. t<sub>SYSCLK</sub> is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- 4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to HRESET.
- 5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, TBST, TSIZ[0:2], GBL, WT, CI, DH[0:31], DL[0:31], DP[0:7], BR, CKSTP\_OUT, DRDY, HIT, QREQ, RSRV.
- 6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V<sub>DD</sub> to 0.8 V.
- 7. According to the 60x bus protocol, ABB and DBB are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for ABB or DBB is 0.5 × t<sub>SYSCLK</sub>, that is, less than the minimum t<sub>SYSCLK</sub> period, to ensure that another master asserting ABB, or DBB on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
- 8. According to the 60x bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue since any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of AACK. The nominal precharge width for ARTRY is 1.0 t<sub>SYSCLK</sub>; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
- 9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.



Figure 4. AC Test Load



**Electrical and Thermal Characteristics** 

## 4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 bus interface AC timing specifications for the MPC7410 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

## Table 10. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Baramatar	Symbol	400, 450,	500 MHz	Unit	Notoo
Farameter	Symbol	Min	Мах	Onit	Notes
L2SYNC_IN rise and fall time	$t_{\rm L2CR}$ and $t_{\rm L2CF}$	_	1.0	ns	1
Setup times: Data and parity	t <sub>DVL2CH</sub>	1.5	—	ns	2
Input hold times: Data and parity	t <sub>DXL2CH</sub>		0.0	ns	2
Valid times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	tl2CHOV		2.5 2.5 2.9 3.5	ns	3, 4
Output hold times All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t <sub>L2CHOX</sub>	0.4 0.8 1.2 1.6	 	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t <sub>L2CHOZ</sub>		2.0 2.5 3.0 3.5	ns	_

Notes:

1. Rise and fall times for the L2SYNC\_IN input are measured from 20% to 80% of L2OV\_DD.

2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC\_IN (see Figure 8). Input timings are measured at the pins.

3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC\_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive  $50-\Omega$  load (see Figure 10).

4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 00 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 10 is recommended.





Figure 8 shows the L2 bus input timing diagrams for the MPC7410.



Figure 9 shows the L2 bus output timing diagrams for the MPC7410.



Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC7410.



Figure 10. AC Test Load for the L2 Interface

## 4.2.5 IEEE 1149.1 AC Timing Specifications

Table 11 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

## Table 11. JTAG AC Timing Specifications (Independent of SYSCLK)<sup>1</sup>

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Мах	Unit	Notes
TCK frequency of operation	f <sub>TCLK</sub>	0	33.3	MHz	_
TCK cycle time	t <sub>TCLK</sub>	30	—	ns	—
TCK clock pulse width measured at $OV_{DD}/2$	t <sub>JHJL</sub>	15	—	ns	—
TCK rise and fall times	$t_{\mbox{\scriptsize JR}}$ and $t_{\mbox{\scriptsize JF}}$	0	2	ns	_



**Pin Assignments** 

# 5 Pin Assignments

Figure 16, part A shows the pinout for the MPC7410, 360 CBGA, 360 HCTE, and 360 HCTE Lead Free C5 Spheres packages as viewed from the top surface. Figure 16, part B shows the side profile of the CBGA and HCTE\_CBGA packages to indicate the direction of the top surface view. Figure 16, part C shows the side profile of the HCTE\_LGA package to indicate the direction of the top surface view.









Figure 16. Pinout of the MPC7410, 360 CBGA and 360 HCTE Packages as Viewed from the Top Surface

# 6 Pinout Listings

Table 12 provides the pinout listing for the MPC7410 360 CBGA, 360 HCTE packages.

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages

Signal Name	Pin Number	Active	I/O	I/F Select <sup>1</sup>	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	BVSEL	
AACK	N3	Low	Input	BVSEL	—
ABB	L7	Low	Output	BVSEL	12, 16
AP[0:3]	C4, C5, C6, C7	High	I/O	BVSEL	—
ARTRY	L6	Low	I/O	BVSEL	—
AV <sub>DD</sub>	A8	—	Input	V <sub>DD</sub>	—
BG	H1	Low	Input	BVSEL	—
BR	E7	Low	Output	BVSEL	—
BVSEL	W1	High	Input	N/A	1, 3, 8, 9, 14
СНК	K11	Low	Input	BVSEL	2, 8, 9
CI	C2	Low	I/O	BVSEL	—
CKSTP_IN	B8	Low	Input	BVSEL	_
CKSTP_OUT	D7	Low	Output	BVSEL	—
CLK_OUT	E3	High	Output	BVSEL	—
DBB	К5	Low	Output	BVSEL	12, 16
DBG	К1	Low	Input	BVSEL	—
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	BVSEL	



### **Pinout Listings**

### Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select <sup>1</sup>	Notes
V <sub>DD</sub>	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12			N/A	

Notes:

- 1. OV<sub>DD</sub> supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); L2OV<sub>DD</sub> supplies power to the L2 cache interface (L2ADDR[0:18], L2DATA[0:63], L2DP[0:7], and L2SYNC\_OUT) and the L2 control signals; and V<sub>DD</sub> supplies power to the processor core and the PLL and DLL (after filtering to become AV<sub>DD</sub> and L2AV<sub>DD</sub>, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V<sub>in</sub> or supply voltages, see Table 3.
- 2. These are test signals for factory use only and must be pulled up to OV<sub>DD</sub> for normal machine operation.
- 3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV<sub>DD</sub>, GND, HRESET, or ¬HRESET. For the MPC7410 the L2 bus only supports 2.5- and 1.8-V options. The default selection, if L2VSEL is left unconnected, is 2.5-V operation. For the MPC7410 the processor bus supports 3.3-, 2.5-, and 1.8-V options. The default selection, if BVSEL is left unconnected, is 3.3-V operation. Refer to Table 2 for supported BVSEL and L2VSEL settings.
- 4. PLL\_CFG[0:3] must remain stable during operation; should only be changed during the assertion of HRESET or during sleep mode and must adhere to the internal PLL-relock time requirement.
- 5. Ignored input in 60x bus mode.
- 6. Unused output in 60x bus mode. Signal is three-stated in 60x mode.
- 7. Deasserted (pulled high) at HRESET negation for 60x bus mode. Asserted (pulled low) at HRESET negation for MPX bus mode.
- 8. Uses one of nine existing no connects in the MPC750 360 BGA package.
- 9. Internal pull up on die. Pulled-up signals are  $V_{\text{DD}}$  based.
- 10.Reuses MPC750 DRTRY, DBDIS, and TLBISYNC pins (DTI1, DTI2, and EMODE, respectively).
- 11. The VOLTDET pin position on the MPC750 360 BGA package is now an L2OV<sub>DD</sub> pin on the MPC7410 360 package.
- 12.Output only for MPC7410, was I/O for MPC750.
- 13.MPX bus mode only.
- 14. If necessary, to overcome the internal pull-up resistance and ensure this input will recognize a low signal, a pull-down resistance less than 250  $\Omega$  should be used.
- 15.MCP minimum pulse width: asynchronous, falling-edge input needs to be held asserted for a minimum of 2 cycles to guarantee that it is latched by the processor.
- 16.In MPX bus mode the ABB signal is called AMON and the DBB signal is called DMON. These signals are not a requirement of the MPX bus protocol and may not be available on future products.



# 7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7410, 360 CBGA and 360 HCTE packages.

# 7.1 Package Parameters for the MPC7410, 360 CBGA and 360 HCTE\_CBGA

The package parameters are as provided in the following list. The package types are the  $25 \times 25$  mm, 360-lead ceramic ball grid array package (CBGA) or the  $25 \times 25$  mm, 360-lead high coefficient of thermal expansion CBGA package (HCTE\_CBGA).

Package outline	$25 \times 25 \text{ mm}$
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	6.8 ppm/°C (CBGA)
	12.3ppm/°C (HCTE_CBGA)

# 7.2 Package Parameters for the MPC7410, 360 HCTE\_CBGA (Lead Free C5 Spheres)

The package parameters are as listed here. The package types are the  $25 \times 25$  mm, 360-lead high coefficient of thermal expansion CBGA package with lead-free C5 spheres (HCTE\_CBGA lead-free spheres).

Package outline	$25 \times 25 \text{ mm}$
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.76 mm (30 mil)
Coefficient of thermal expansion	12.3ppm/°C



Millimeters

\_\_\_\_

MAX

2.80

0.60

1.30

0.60

0.90

0.90

12.50

9.00

14.30 11.00

9.75

8.60

\_

9.50

\_

3.30

\_

25.00 BSC

1.27 BSC

25.00 BSC

22.86 BSC

\_

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## Mechanical Dimensions for the MPC7410, 360 HCTE\_CBGA 7.4 (Lead Free C5 Spheres)

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 HCTE\_CBGA (lead-free C5 spheres) package.



Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410 360 HCTE\_CBGA (Lead-Free C5 Spheres) Package



**System Design Information** 

## 7.6 Substrate Capacitors for the MPC7410

Figure 20 shows the connectivity of the substrate capacitor pads for the MPC7410, 360 CBGA and 360 HCTE packages.



Package Caps	Value µF	Voltage Reference
C1-1	0.04	L2OV <sub>DD</sub>
C1-2	0.01	GND
C2-1	0.01	L2OV <sub>DD</sub>
C2-2	0.01	GND
C3-1	0.01	V <sub>DD</sub>
C3-2	0.01	GND
C4-1	0.01	OV <sub>DD</sub>
C4-2	0.01	GND
C5-1	0.01	OV <sub>DD</sub>
C5-2	0.01	GND
C6-1	0.01	V <sub>DD</sub>
C6-2	0.01	GND

Figure 20. Substrate Bypass Capacitors for the MPC7410

# 8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC7410.

# 8.1 PLL Configuration

The MPC7410 PLL is configured by the PLL\_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7410 is shown in Table 13 for example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the minimum and maximum core frequencies listed in Table 8.

	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
PLL_CFG [0:3]	Bus-to- Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0100	2x	2x	—	—	—	—	—	—	—
0110	2.5x	2x	—	—	—	—	—	—	—
1000	Зх	2x	-	—	-	—	-	—	400 (800)
1110	3.5x	2x	—	—	—	—	—	350 (700)	465 (930)
1010	4x	2x	—	—	—	—	—	400 (800)	—

Table 13. MPC7410 Microprocessor PLL Configuration



	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
PLL_CFG [0:3]	Bus-to- Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz	
0111	4.5x	2x	—	_	—	_	375 (750)	450 (900)	—	
1011	5x	2x	—		—	375 (750)	416 (833)	500 (1000)	—	
1001	5.5x	2x	_		366 (733)	412 (825)	458 (916)	_	_	
1101	6x	2x	—		400 (800)	450 (900)	500 (1000)	_	—	
0101	6.5x	2x	—	-	433 (866)	488 (967)	—			
0010	7x	2x	—	350 (700)	466 (933)	—	—	—	—	
0001	7.5x	2x	—	375 (750)	500 (1000)	—	—	—	—	
1100	8x	2x	—	400 (800)	—	—	—	—	—	
0000	9x	2x	—	450 (900)	—	—	—	—	—	
0011	PLL off	/bypass	PLL o	PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL	off	PLL off, no core clocking occurs							

### Table 13. MPC7410 Microprocessor PLL Configuration (continued)

Notes:

1. PLL\_CFG[0:3] settings not listed are reserved.

- The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
- 3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and third-party emulator tool development only.
- Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
- 4. In PLL-off mode, no clocking occurs inside the MPC7410 regardless of the SYSCLK input.
- 5. PLL-off mode should not be used during chip power-up sequencing.

The MPC7410 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC7410. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC7410 to the external RAMs. A separate clock output, L2SYNC\_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC\_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the







### Printed-Circuit Board

## Figure 27. LGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

The board designer can choose between several types of heat sinks to place on the MPC7410. There are several commercially-available heat sinks for the MPC7410 from the following vendors:

Aavid Thermalloy	603-224-9988
70 Commercial Street, Suite 200	
Concord, NH 03301	
Internet: www.aavidthermalloy.com	
Alpha Novatech	408-567-8082
473 Sapena Ct. #12	
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
The Bergquist Company	800-347-4572
18930 West 78th St.	
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
International Electronic Research Corporation (IERC)	818-842-7277
413 North Moss St.	
Burbank, CA 91502	
Internet: www.ctscorp.com	
Wakefield Engineering	603-635-2800
33 Bridge St.	
Pelham, NH 03076	
Internet: www.wakefield.com	

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.





Figure 29 describes the thermal performance of selected thermal interface materials.



The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Chomerics, Inc.	781-935-4850
77 Dragon Court	
Woburn, MA 01888-4014	
Internet: www.chomerics.com	
Dow-Corning Corporation	800-248-2481
Dow-Corning Electronic Materials	
2200 W. Salzburg Rd.	
Midland, MI 48686-0997	
Internet: www.dow.com	
Shin-Etsu MicroSi, Inc.	888-642-7674
10028 S. 51st St.	
Phoenix, AZ 85044	
Internet: www.microsi.com	



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888-246-9050

Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com

## 8.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_i = T_a + T_r + (\theta_{ic} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T<sub>i</sub> is the die-junction temperature

T<sub>a</sub> is the inlet cabinet ambient temperature

 $T_r$  is the air temperature rise within the computer cabinet

 $\theta_{ic}$  is the junction-to-case thermal resistance

 $\theta_{int}$  is the adhesive or interface material thermal resistance

 $\theta_{sa}$  is the heat sink base-to-ambient thermal resistance

P<sub>d</sub> is the power dissipated by the device

During operation the die-junction temperatures  $(T_j)$  should be maintained less than the value specified in Table 3. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature  $(T_a)$  may range from 30° to 40°C. The air temperature rise within a cabinet  $(T_r)$  may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ( $\theta_{int}$ ) is typically about 1°C/W. Assuming a T<sub>a</sub> of 30°C, a T<sub>r</sub> of 5°C, a CBGA package  $\theta_{jc} = 0.03$ , and a power consumption (P<sub>d</sub>) of 5.0 W, the following expression for T<sub>j</sub> is obtained:

Die-junction temperature:  $T_i = 30^{\circ}C + 5^{\circ}C + (0.03^{\circ}C/W + 1.0^{\circ}C/W + \theta_{sa}) \times 5.0 W$ 

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ( $\theta_{sa}$ ) versus airflow velocity is shown in Figure 30.

Assuming an air velocity of 0.5 m/s, we have an effective R<sub>sa</sub> of 7°C/W, thus

 $T_i = 30^{\circ}C + 5^{\circ}C + (0.03^{\circ}C/W + 1.0^{\circ}C/W + 7^{\circ}C/W) \times 5.0 W,$ 

resulting in a die-junction temperature of approximately 75°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.



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### **Document Revision History**

Revision	Date	Substantive Change(s)				
1.0	_	Section 1.3 and Table 3—revised $OV_{DD}$ from 3.3 V ± 100 mV to 3.3 V ± 165 mV.				
		Table 13—removed unsupported PLL configurations.				
		Table 12—added note 15 for minimum $\overline{\text{MCP}}$ pulse width, correct note 3 for 3.3-V processor bus support.				
		Table 13—revised note 3 to include emulator tool development.				
		Table 14—removed unsupported Core-to-L2 example frequencies.				
		Section 1.8.8—updated heat sink vendors list.				
		Section 1.8.8.2—updated interface vendors list.				
		Table 1—updated voltage sequencing requirements notes 3 and 4.				
		Table 4—Updated/added thermal characteristics.				
		Table 5—removed table and TAU related information, TAU is no longer supported.				
		Table 6—updated I <sub>in</sub> and I <sub>TSI</sub> leakage current specs.				
		Section 1.8.3—removed section.				
		Section 1.10—reformatted section.				
		Section 1.8.6—changed recommended pull-up resistor value to 1 kW–5 kW. Added $\overline{AACK}$ , $\overline{TEA}$ , and $\overline{TS}$ to control signals needing pull-ups. Added pull-up resistor value recommendation for L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD}$ _MODE factory test signals.				
		Section 1.8.7—revised text regarding connection of $\overline{\text{TRST}}$ . Combined Figure 22, Figure 23, and Table 17, into Figure 21.				
		Table 7—corrected min VCO frequencies from 450 to 700 MHz to match min processor frequency of 350 MHz.				
		Table 2—added note 3 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V $OV_{DD}$ .				
		Table 3—added notes 5 and 6 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V ${\rm OV}_{\rm DD}$				
		Table 5—added note 8 regarding DC voltage limits for JTAG signals.				

Table 16. Document Revision	History (continued)
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**Ordering Information** 

## **10.2 Part Numbers Not Fully Addressed by This Document**

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document, as described in the following tables.

Table 18. Part Numbers Addressed b	by MPC7410RXnnnPx Series	<b>Part Number Specifications</b>
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MPC	7410	RX	nnn	Р	X
Product Code	Part Identifier	Package	Processor Frequency <sup>1</sup>	Application Modifier	Revision Level
MPC	7410	RX = CBGA	450 500 550	P: 2.0 V ± 50 mV 0° to 65°C	C: 1.2; PVR = 800C 1102 <sup>1</sup> D: 1.3; PVR = 800C 1103 <sup>2</sup> E: 1.4; PVR = 800C 1104 <sup>3</sup>

**Notes:** Document order numbers:

1. MPC7410PCPNS.

2. MPC7410PDPNS.

3. MPC7410PEPNS.

## Table 19. Part Numbers Addressed by MPC7410 RISC Microprocessor HardwareSpecifications Addendum for the MPC7410xxnnnNE Series

Mxx	7410	XX	nnn	Ν	E
Product Code	Part Identifier	Package	Processor Frequency <sup>1</sup>	Application Modifier	Revision Level
MPC	7410	RX = CBGA	400 450 500	N: 1.5 V ± 50 mV	E: 1.4; PVR = 800C 1104
		HX = HCTE_CBGA VS = HCTE_LGA	400 450		
MC		VU = HCTE_CBGA (Lead Free C5 Solder Spheres)			

Note: Document order number: MPC7410ECS02AD

## Table 20. Part Numbers Addressed by MPC7410TRXnnnNE Part Number Specification

MPC	7410	Т	RX	nnn	Ν	E
Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency <sup>1</sup>	Application Modifier	Revision Level
MPC	7410	T: -40° to 105°C	RX = CBGA	400 450	N: 1.5 V ±50 mV	E: 1.4; PVR = 800C 1104

Note: Document order number: MPC7410TRXNEPNS.

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