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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410hx500le

- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754™ single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations

  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32 Kbyte, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32 Kbyte, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-Kbyte, 1-Mbyte, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-Kbyte), 64-byte (1-Mbyte), or 128-byte (2-Mbyte) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256 Kbytes, 512 Kbytes, 1 Mbyte, or 2 Mbytes of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

3 General Parameters

The following list provides a summary of the general parameters of the MPC7410:

Technology	0.18 µm CMOS, six-layer metal
Die size	6.32 mm × 8.26 mm (52 mm^2)
Transistor count	10.5 million
Logic design	Fully static
Packages	Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array (HCTE_CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array with lead free C5 spheres (HCTE_CBGA Lead Free C5 Spheres) Surface mount 360 high coefficient of thermal expansion ceramic land grid array (HCTE_LGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 3 for recommended operating conditions)
I/O power supply	1.8 V ± 100 mV DC or 2.5 V ± 100 mV 3.3 V ± 165 mV (system bus only) (input thresholds are configuration pin selectable)

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7410.

4.1 DC Electrical Characteristics

The tables in this section describe the MPC7410 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.1	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.1	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.1	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3, 6
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 2.8	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.2 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	—
Storage temperature range		T_{stg}	–55 to 150	°C	—

Table 4. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	< 0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active portion of the die and the calculated case temperature at the top of the die. The actual value of R JC is less than 0.1 °C/W.

Note: Refer to Section 8.8, "Thermal Management Information," for details on thermal management.

Table 5 provides the DC electrical characteristics for the MPC7410.

Table 5. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8	V_{IH}	$0.65 \times (L2)OV_{DD}$	$(L2)OV_{DD} + 0.2$	V	2, 3, 8
	2.5	V_{IH}	1.7	$(L2)OV_{DD} + 0.2$		
	3.3	V_{IH}	2.0	$OV_{DD} + 0.3$		
Input low voltage (all inputs except SYSCLK)	1.8	V_{IL}	–0.3	$0.35 \times (L2)OV_{DD}$	V	8
	2.5	V_{IL}	–0.3	$0.2 \times (L2)OV_{DD}$		
	3.3	V_{IL}	–0.3	0.8		
SYSCLK input high voltage	1.8	CV_{IH}	1.5	$OV_{DD} + 0.2$	V	2, 8
	2.5	CV_{IH}	2.0	$OV_{DD} + 0.2$		
	3.3	CV_{IH}	2.4	$OV_{DD} + 0.3$		
SYSCLK input low voltage	1.8	CV_{IL}	–0.3	0.2	V	8
	2.5	CV_{IL}	–0.3	0.4		
	3.3	CV_{IL}	–0.3	0.4		
Input leakage current, $V_{in} = L2OV_{DD}/OV_{DD}$	1.8	I_{in}	—	20	µA	2, 3, 6, 7
	2.5	I_{in}	—	35		
	3.3	I_{in}	—	70		

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

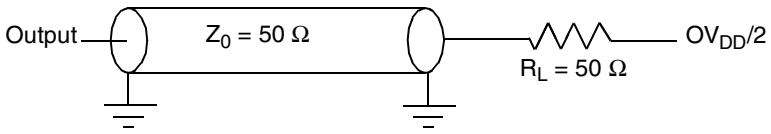


Figure 4. AC Test Load

Figure 8 shows the L2 bus input timing diagrams for the MPC7410.

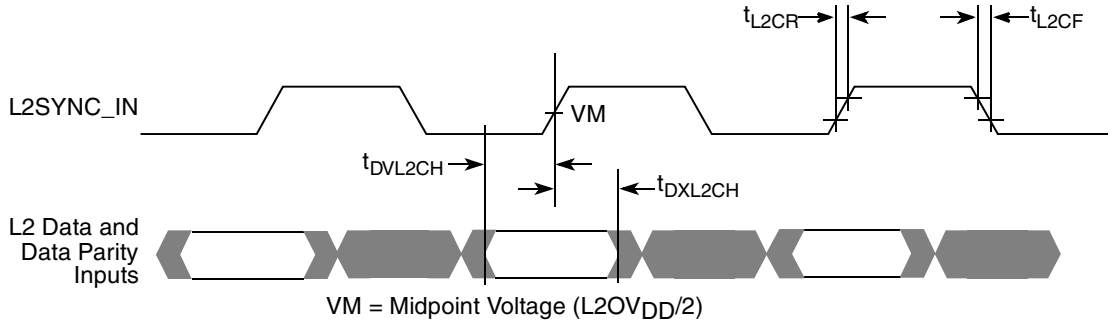


Figure 8. L2 Bus Input Timing Diagrams

Figure 9 shows the L2 bus output timing diagrams for the MPC7410.

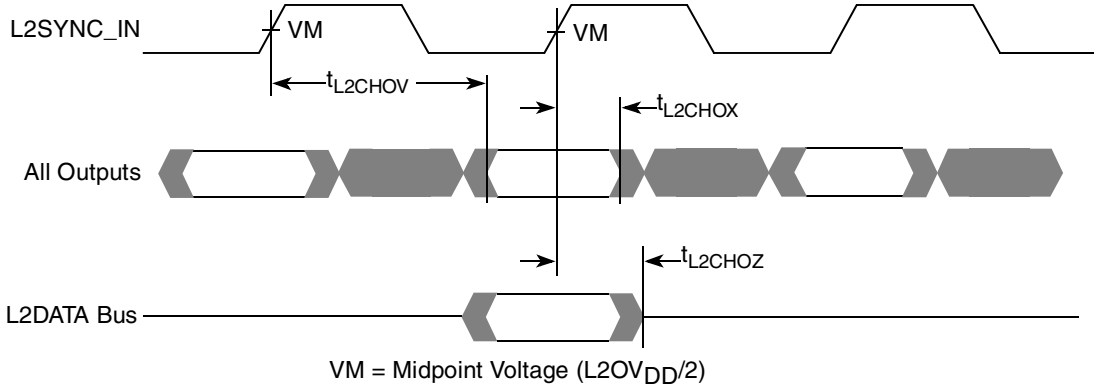


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC7410.

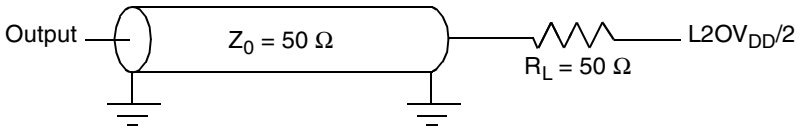


Figure 10. AC Test Load for the L2 Interface

4.2.5 IEEE 1149.1 AC Timing Specifications

Table 11 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	—
TCK cycle time	t_{TCLK}	30	—	ns	—
TCK clock pulse width measured at $OV_{DD}/2$	t_{JHJL}	15	—	ns	—
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	—

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

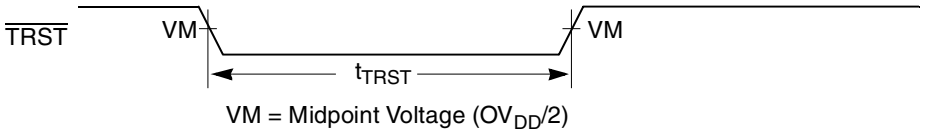


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

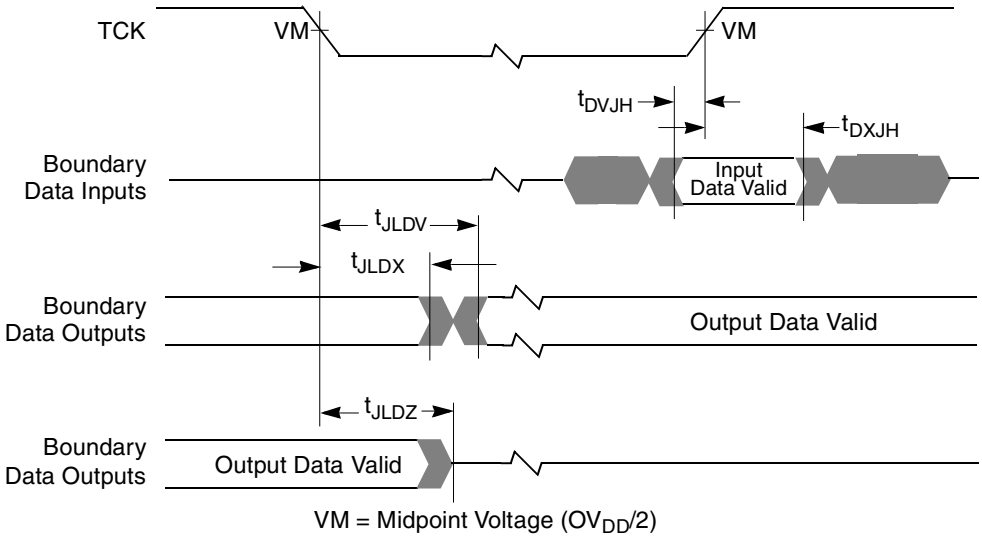


Figure 14. Boundary-Scan Timing Diagram

Figure 15 provides the test access port timing diagram.

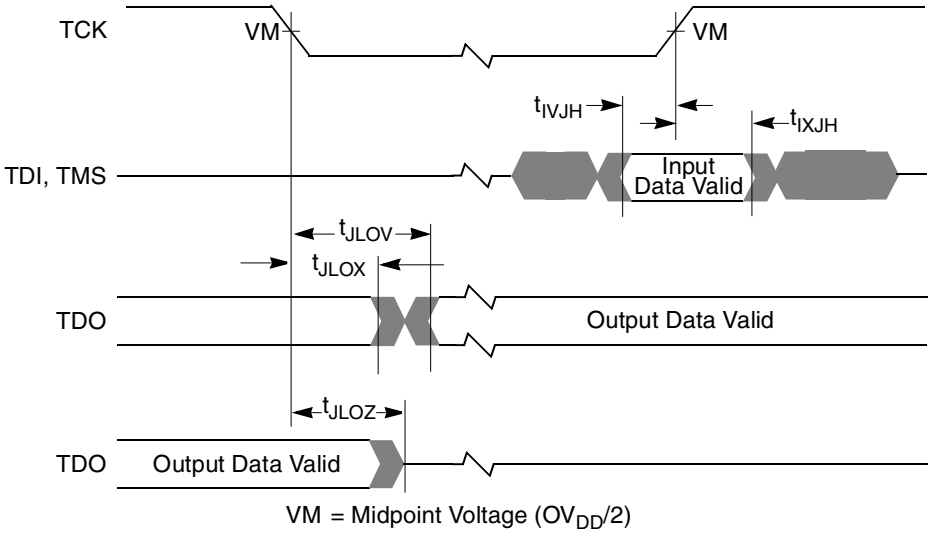
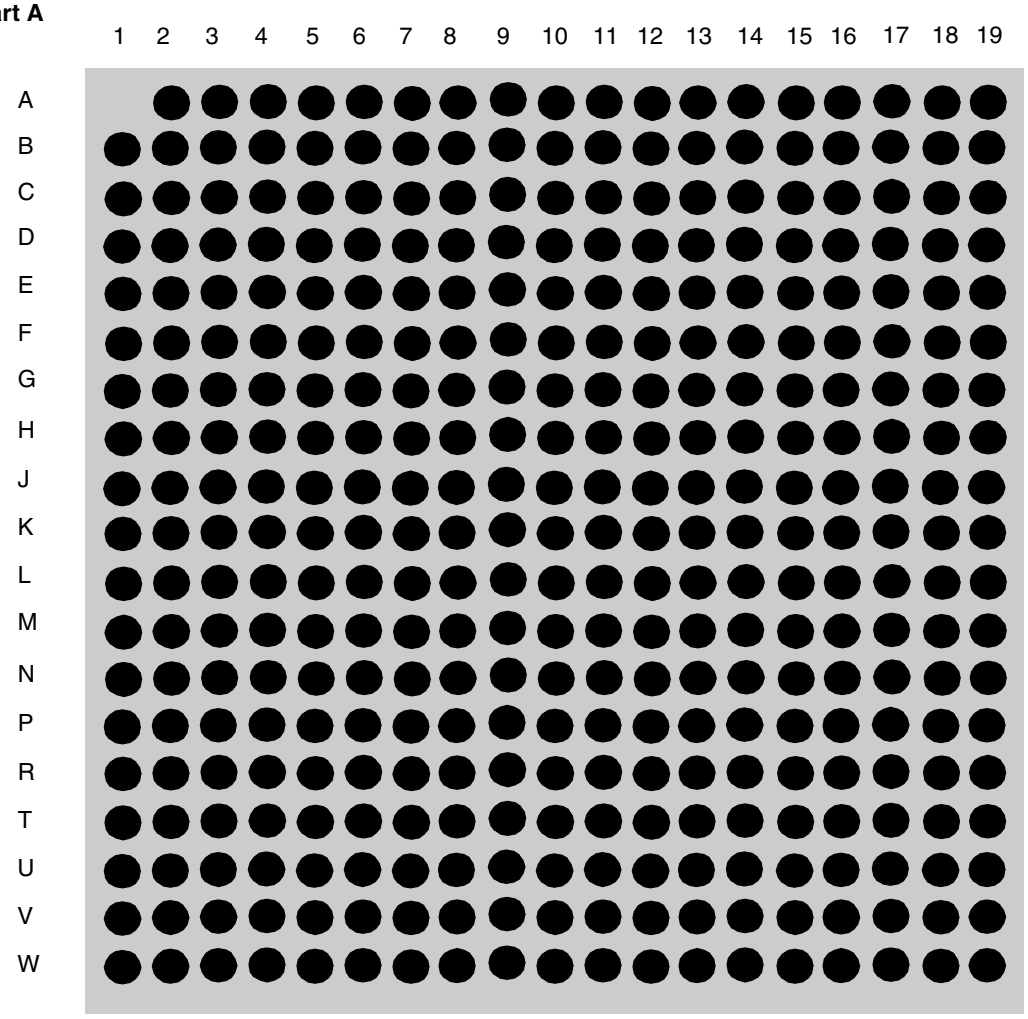


Figure 15. Test Access Port Timing Diagram

5 Pin Assignments

Figure 16, part A shows the pinout for the MPC7410, 360 CBGA, 360 HCTE, and 360 HCTE Lead Free C5 Spheres packages as viewed from the top surface. Figure 16, part B shows the side profile of the CBGA and HCTE_CBGA packages to indicate the direction of the top surface view. Figure 16, part C shows the side profile of the HCTE_LGA package to indicate the direction of the top surface view.

Part A



Not to Scale

Part B

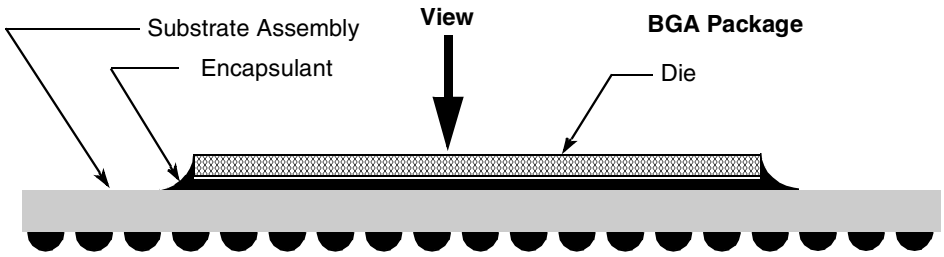
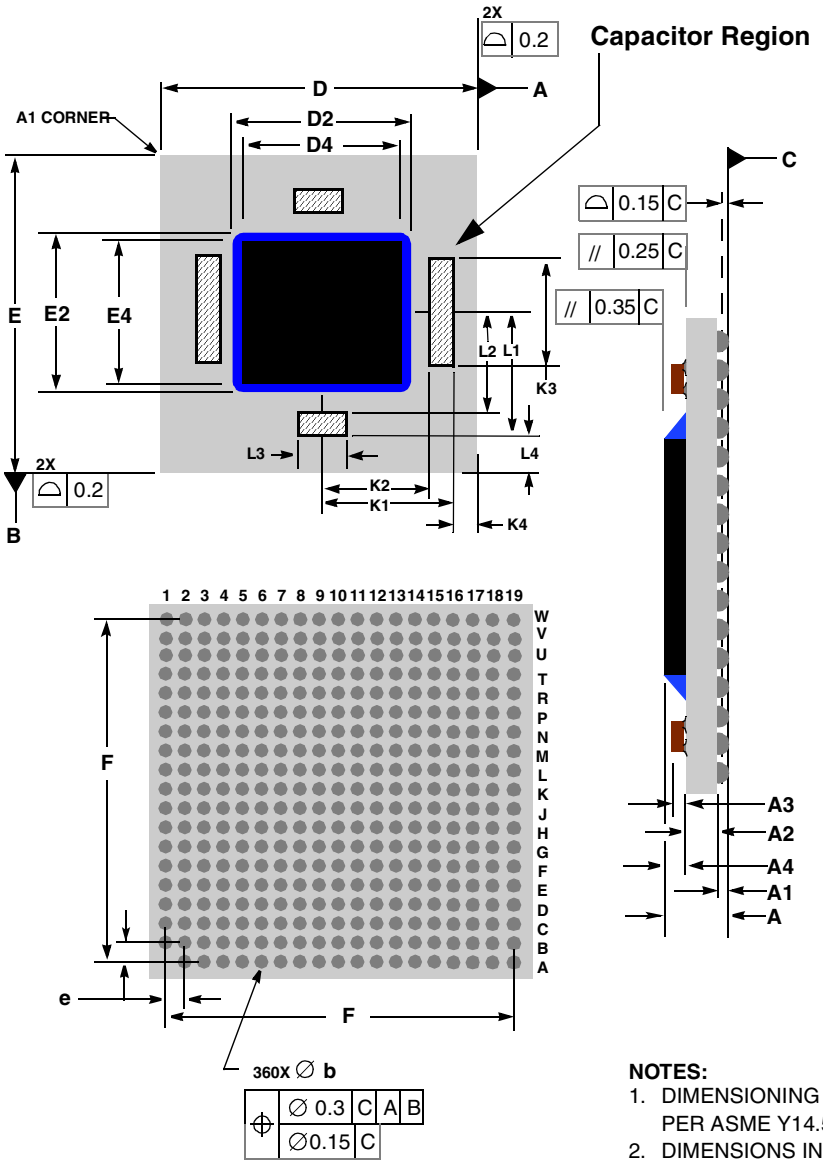


Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
L2VSEL	A19	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{L2WE}}$	N16	Low	Output	L2VSEL	—
L2ZZ	G17	High	Output	L2VSEL	—
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	BVSEL	2
$\overline{\text{MCP}}$	B11	Low	Input	BVSEL	15
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	N/A	—
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	BVSEL	4
$\overline{\text{QACK}}$	B2	Low	Input	BVSEL	—
$\overline{\text{QREQ}}$	J3	Low	Output	BVSEL	—
$\overline{\text{RSRV}}$	D3	Low	Output	BVSEL	—
$\overline{\text{SHD0}}$	B3	Low	I/O	BVSEL	8
$\overline{\text{SHD1}}$	B4	Low	I/O	BVSEL	5, 8
$\overline{\text{SMI}}$	A12	Low	Input	BVSEL	—
$\overline{\text{SRESET}}$	E10	Low	Input	BVSEL	—
SYSCLK	H9	—	Input	BVSEL	—
$\overline{\text{TA}}$	F1	Low	Input	BVSEL	—
TBEN	A2	High	Input	BVSEL	—
$\overline{\text{TBST}}$	A11	Low	Output	BVSEL	—
TCK	B10	High	Input	BVSEL	—
TDI	B7	High	Input	BVSEL	9
TDO	D9	High	Output	BVSEL	—
$\overline{\text{TEA}}$	J1	Low	Input	BVSEL	—
TMS	C8	High	Input	BVSEL	9
$\overline{\text{TRST}}$	A10	Low	Input	BVSEL	9
$\overline{\text{TS}}$	K7	Low	I/O	BVSEL	—
TSIZ[0:2]	A9, B9, C9	High	Output	BVSEL	—
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	BVSEL	—
$\overline{\text{WT}}$	C3	Low	I/O	BVSEL	—

7.3 Mechanical Dimensions for the MPC7410, 360 CBGA and 360 HCTE_CBGA

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 CBGA and 360 HCTE_CBGA packages.



	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1.00
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.90
b	0.82	0.93
D	25.00 BSC	
D2	—	12.50
D4	6.00	9.00
e	1.27 BSC	
E	25.00 BSC	
E2	—	14.30
E4	8.00	11.00
F	22.86 BSC	
K1	—	9.75
K2	6.46	—
K3	8.20	8.60
K4	2.75	—
L1	—	9.50
L2	6.94	—
L3	3.10	3.30
L4	3.00	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410, 360 CBGA and 360 HCTE_CBGA Packages

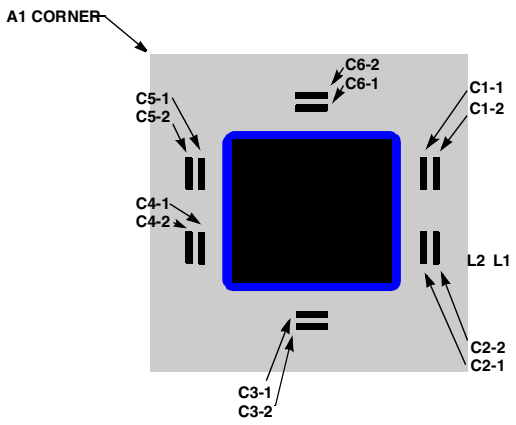
7.5 Package Parameters for the MPC7410, 360 HCTE_LGA

The package parameters are as listed here. The package type is the 25 × 25 mm, 360 high coefficient of thermal expansion LGA package (HCTE_LGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 land array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3ppm/°C

7.6 Substrate Capacitors for the MPC7410

Figure 20 shows the connectivity of the substrate capacitor pads for the MPC7410, 360 CBGA and 360 HCTE packages.



Package Caps	Value µF	Voltage Reference
C1-1	0.01	$L2OV_{DD}$
C1-2		GND
C2-1	0.01	$L2OV_{DD}$
C2-2		GND
C3-1	0.01	V_{DD}
C3-2		GND
C4-1	0.01	OV_{DD}
C4-2		GND
C5-1	0.01	OV_{DD}
C5-2		GND
C6-1	0.01	V_{DD}
C6-2		GND

Figure 20. Substrate Bypass Capacitors for the MPC7410

8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC7410.

8.1 PLL Configuration

The MPC7410 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7410 is shown in Table 13 for example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the minimum and maximum core frequencies listed in Table 8.

Table 13. MPC7410 Microprocessor PLL Configuration

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0100	2x	2x	—	—	—	—	—	—	—
0110	2.5x	2x	—	—	—	—	—	—	—
1000	3x	2x	—	—	—	—	—	—	400 (800)
1110	3.5x	2x	—	—	—	—	—	350 (700)	465 (930)
1010	4x	2x	—	—	—	—	—	400 (800)	—

existing designs should qualify both AV_{DD} filter solutions, and the filter providing the most robust margin should be implemented.

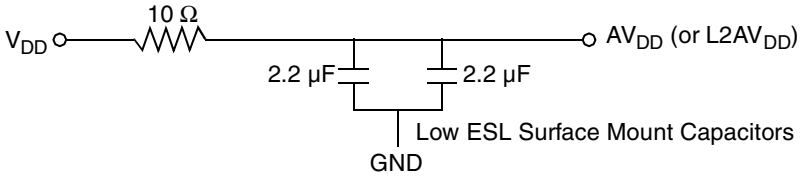


Figure 21. PLL Power Supply Filter Circuit No.1

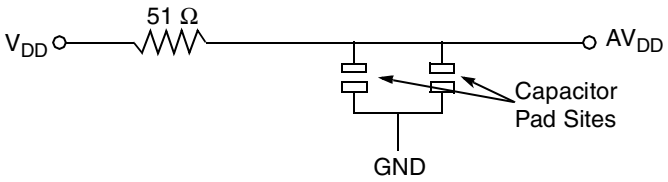


Figure 22. PLL Power Supply Filter Circuit No. 2

The filter circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. A separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

It is the recommendation of Freescale, that systems that implement the AV_{DD} filter shown in Figure 22 design in the pads for the removed capacitors (shown in Figure 21), to provide for the possible reintroduction of the filter in Figure 21. This would be necessary in case there is a planned transition from the CBGA package to the HCTE package of the MPC7410.

8.3 Decoupling Recommendations

Due to the MPC7410 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7410 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7410 system, and the MPC7410 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the MPC7410. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations, where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used; the remainder of the L2 interface may be left unterminated.

8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 23).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the driver impedance measurement circuit described above.

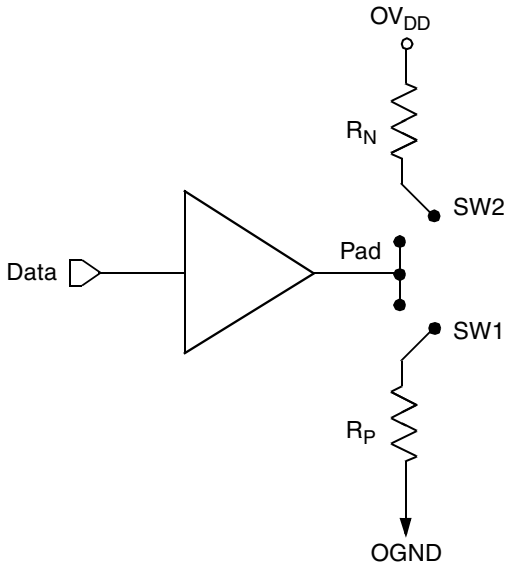


Figure 23. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 24. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 24 describes the alternate driver impedance measurement circuit.

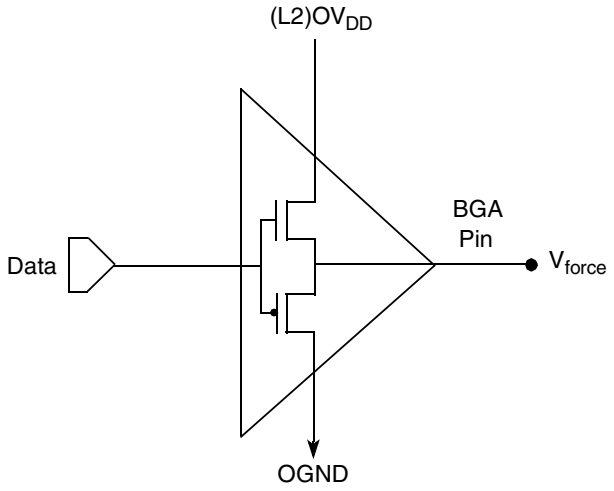


Figure 24. Alternate Driver Impedance Measurement Circuit

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.8 V, OV_{DD} = 2.5 V, T_j = 0° – 105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5–54.3	42.7–54.1	Z_0	Ω
R_P	37.3–55.3	39.3–50.0	Z_0	Ω

8.6 Pull-Up Resistor Requirements

The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on

the MPC7410 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode can be enabled (see the *MPC7410 RISC Microprocessor Family Users' Manual* for more information on this mode), or these signals may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

In systems where $\overline{\text{GBL}}$ is not connected and other devices may be asserting $\overline{\text{TS}}$ for a snoopable transaction while not driving $\overline{\text{GBL}}$ to the processor, we recommend that a strong (1 kΩ) pull-up resistor be used on $\overline{\text{GBL}}$. Note that the MPC7410 will only snoop transactions when $\overline{\text{GBL}}$ is asserted.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If parity checking is disabled through HID0, and parity generation is not required by the MPC7410 (note that the MPC7410 always generates parity), then all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

8.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 25 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 25, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 25 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

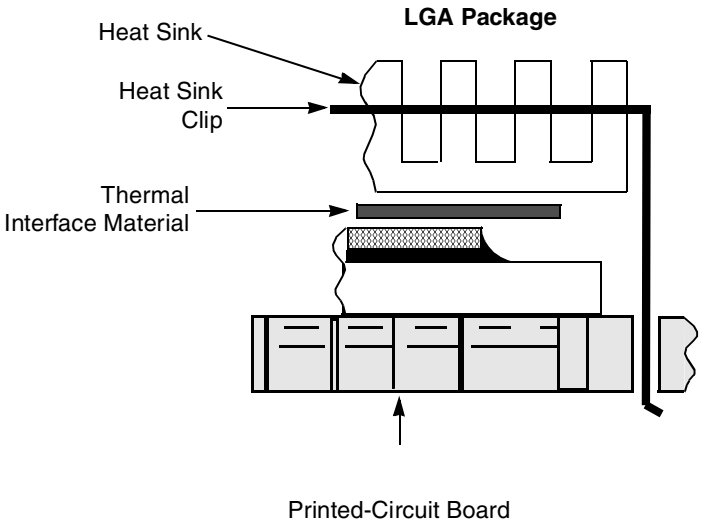


Figure 27. LGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

The board designer can choose between several types of heat sinks to place on the MPC7410. There are several commercially-available heat sinks for the MPC7410 from the following vendors:

Aavid Thermalloy 70 Commercial Street, Suite 200 Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

8.8.1 Internal Package Conduction Resistance

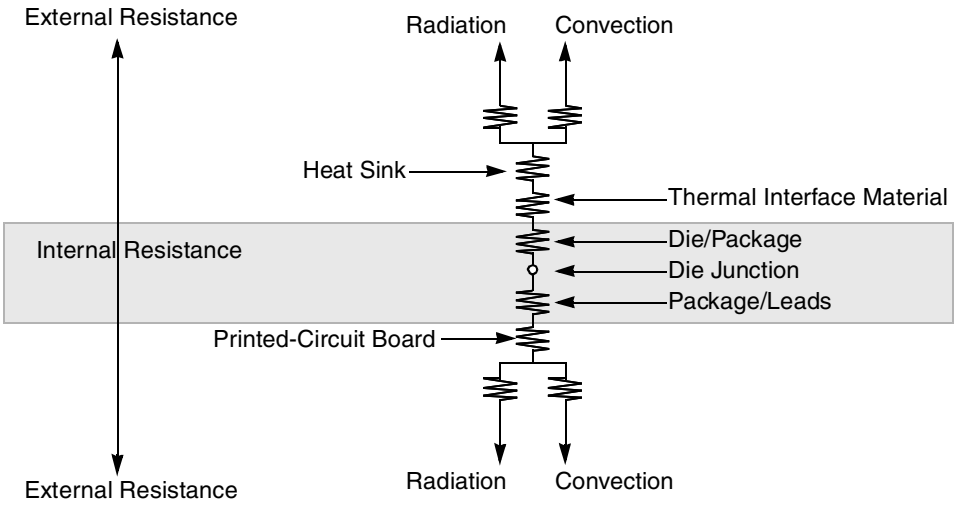
For the exposed-die packaging technology, shown in Table 3, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 28 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.



Note the internal versus external package resistance.

Figure 28. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

8.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 26). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

9 Document Revision History

Table 16 provides a revision history for this hardware specification.

Table 16. Document Revision History

Revision	Date	Substantive Change(s)
6.1	11/16/2007	Updated Table 17 and Table 19 to show the VU package is available as an MC prefix device compared to an MPC prefix for the other package types; this was done to match the specification documents with the device ordering and part marking information. Updated title of Table 19 to reflect correct name of referenced document and updated respective document order information below table. Updated notes in Table 1–Table 3 replacing references to MPC7410RX*nnn*LE with M*xx*7410*xxnnn*LE since notes to apply to all the available packages types.
6	8/14/2007	Updated Table 4 thermal information: • Deleted rows on single-layer (1s) boards. • CBGA package $R_{\theta JMA}$ for natural convection for four layer boards changed from 17 to 18 °C/W. • HCTE package $R_{\theta JMA}$ for natural convection for four layer boards changed from 22 to 20 °C/W. • HCTE package $R_{\theta JMA}$ for 200 ft./min airflow for four layer boards changed from 19 to 16 °C/W with airflow rate specification changed from 200 ft./min to 1 m/sec. • HCTE package $R_{\theta JMA}$ for 400 ft./min airflow for four layer boards changed from 18 to 15 °C/W with airflow rate specification changed from 400 ft./min to 2 m/sec. • CBGA package $R_{\theta JB}$ changed from 8 to 9°C/W. • HCTE package $R_{\theta JB}$ changed from 14 to 11°C/W. • Table 4 Notes 2 - 4 have been revised and updated; Note 5 is no longer used. Notes on table rows have been renumbered. Updated Figure 26 removing optional heat sink clip to package. Removed references in document to adhesive attached thermal solutions. Updated thermal solution vendor information in Section 8.8. Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information to document: • Added Section 7.2, “Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres). • Added Figure 18 for HCTE_CBGA Lead Free C5 Spheres package, similar to Figure 17 but with differences in dimensions A, A1, and b in the figure’s dimension table. • Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information in Table 17 and Table 19. • Changed part marking example in Figure 31 to an HCTE_CBGA device.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1.0	—	Section 1.3 and Table 3—revised OV_{DD} from 3.3 V ± 100 mV to 3.3 V ± 165 mV.
		Table 13—removed unsupported PLL configurations.
		Table 12—added note 15 for minimum $\overline{MCP}$ pulse width, correct note 3 for 3.3-V processor bus support.
		Table 13—revised note 3 to include emulator tool development.
		Table 14—removed unsupported Core-to-L2 example frequencies.
		Section 1.8.8—updated heat sink vendors list.
		Section 1.8.8.2—updated interface vendors list.
		Table 1—updated voltage sequencing requirements notes 3 and 4.
		Table 4—Updated/added thermal characteristics.
		Table 5—removed table and TAU related information, TAU is no longer supported.
		Table 6—updated I_{in} and I_{TSI} leakage current specs.
		Section 1.8.3—removed section.
		Section 1.10—reformatted section.
		Section 1.8.6—changed recommended pull-up resistor value to 1 kW–5 kW. Added $\overline{AACK}$, $\overline{TEA}$, and $\overline{TS}$ to control signals needing pull-ups. Added pull-up resistor value recommendation for L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$ factory test signals.
		Section 1.8.7—revised text regarding connection of $\overline{TRST}$. Combined Figure 22, Figure 23, and Table 17, into Figure 21.
		Table 7—corrected min VCO frequencies from 450 to 700 MHz to match min processor frequency of 350 MHz.
		Table 2—added note 3 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V OV_{DD}.
		Table 3—added notes 5 and 6 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V OV_{DD}.
		Table 5—added note 8 regarding DC voltage limits for JTAG signals.