Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410rx500le

- The MPC7410 is implemented in a next generation process technology for core frequency improvement.
- The MPC7410 floating-point unit has been improved to make latency equal for double- and single-precision operations involving multiplication.
- The completion queue has been extended to eight slots.
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750 four-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback).

Some comments on the MPC7410 with respect to the MPC7400:

- The MPC7410 adds configurable direct-mapped SRAM capability to the L2 cache interface.
- The MPC7410 adds 32-bit interface support to the L2 cache interface. The MPC7410 implements a 19th L2 address pin (L2ASPARE on the MPC7400) in order to support additional address range.
- The MPC7410 removes support for 3.3-V I/O on the L2 cache interface.

Figure 1 shows a block diagram of the MPC7410.

2 Features

This section summarizes features of the MPC7410 implementation of the PowerPC architecture. Major features of the MPC7410 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)

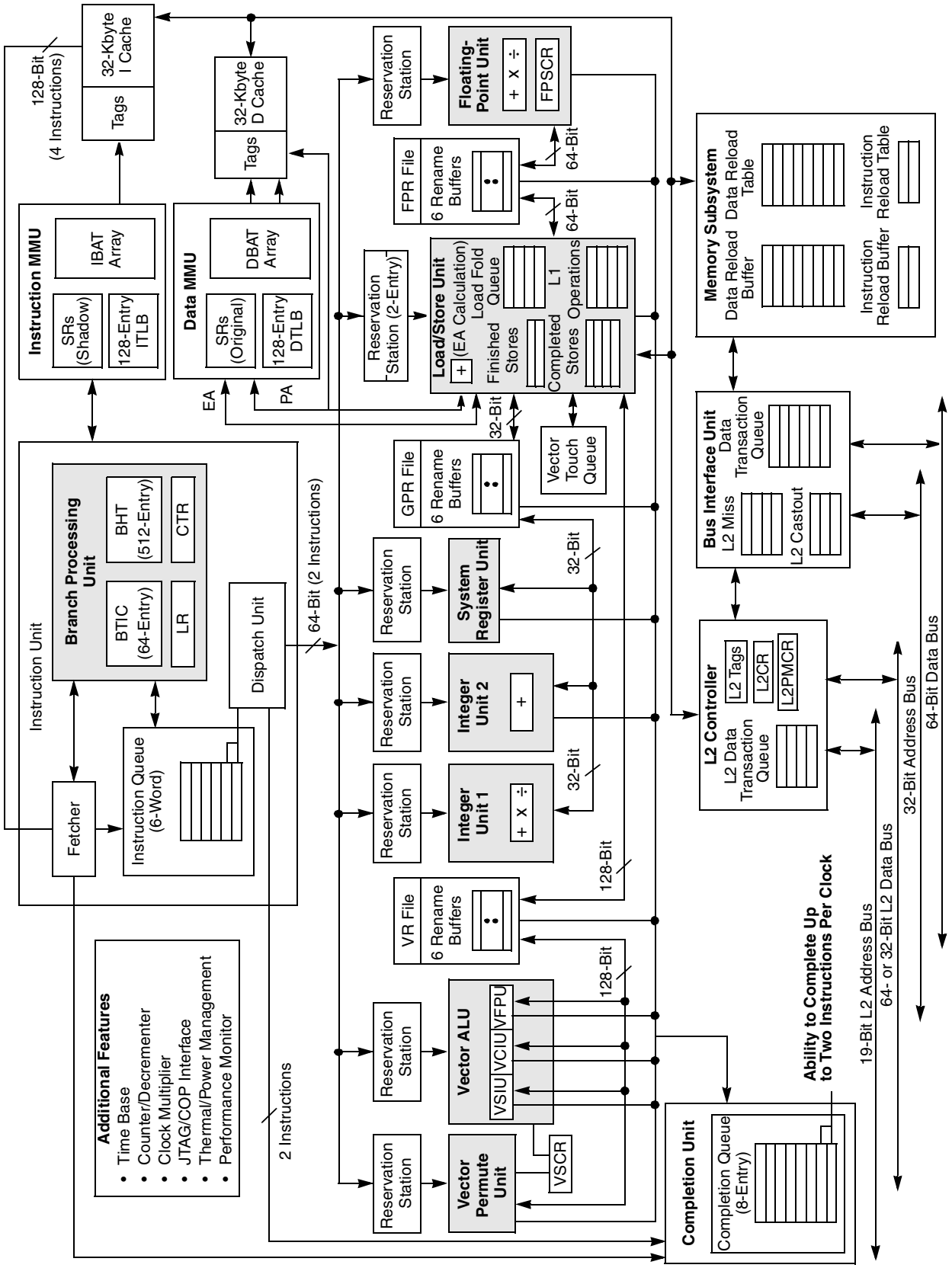


Figure 1. MPC7410 Block Diagram

- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754™ single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Maximum Value	Unit	Notes
Rework temperature	T_{rwk}	260	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.8 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

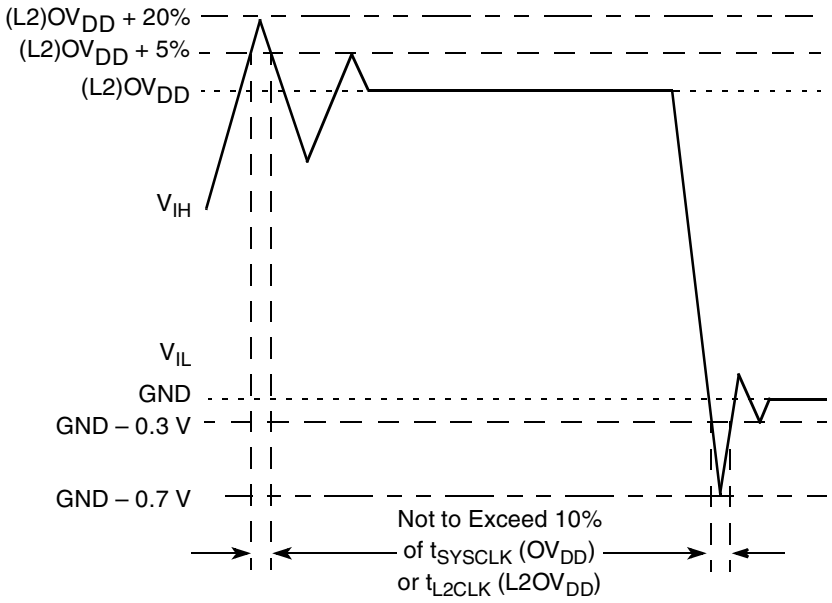


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 4. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	< 0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active portion of the die and the calculated case temperature at the top of the die. The actual value of R JC is less than 0.1 °C/W.

Note: Refer to Section 8.8, "Thermal Management Information," for details on thermal management.

Table 5 provides the DC electrical characteristics for the MPC7410.

Table 5. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8	V_{IH}	$0.65 \times (L2)OV_{DD}$	$(L2)OV_{DD} + 0.2$	V	2, 3, 8
	2.5	V_{IH}	1.7	$(L2)OV_{DD} + 0.2$		
	3.3	V_{IH}	2.0	$OV_{DD} + 0.3$		
Input low voltage (all inputs except SYSCLK)	1.8	V_{IL}	–0.3	$0.35 \times (L2)OV_{DD}$	V	8
	2.5	V_{IL}	–0.3	$0.2 \times (L2)OV_{DD}$		
	3.3	V_{IL}	–0.3	0.8		
SYSCLK input high voltage	1.8	CV_{IH}	1.5	$OV_{DD} + 0.2$	V	2, 8
	2.5	CV_{IH}	2.0	$OV_{DD} + 0.2$		
	3.3	CV_{IH}	2.4	$OV_{DD} + 0.3$		
SYSCLK input low voltage	1.8	CV_{IL}	–0.3	0.2	V	8
	2.5	CV_{IL}	–0.3	0.4		
	3.3	CV_{IL}	–0.3	0.4		
Input leakage current, $V_{in} = L2OV_{DD}/OV_{DD}$	1.8	I_{in}	—	20	µA	2, 3, 6, 7
	2.5	I_{in}	—	35		
	3.3	I_{in}	—	70		

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

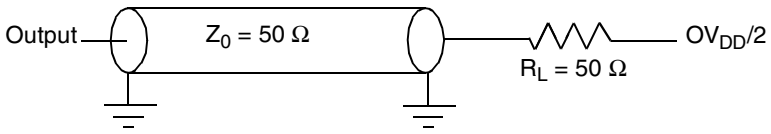


Figure 4. AC Test Load

Figure 5 provides the mode select input timing diagram for the MPC7410. The mode select inputs are sampled twice, once before and once after $\overline{\text{HRESET}}$ negation.

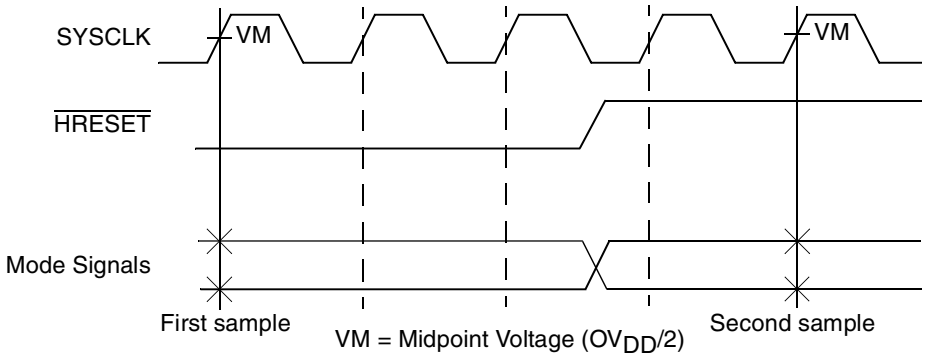


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7410.

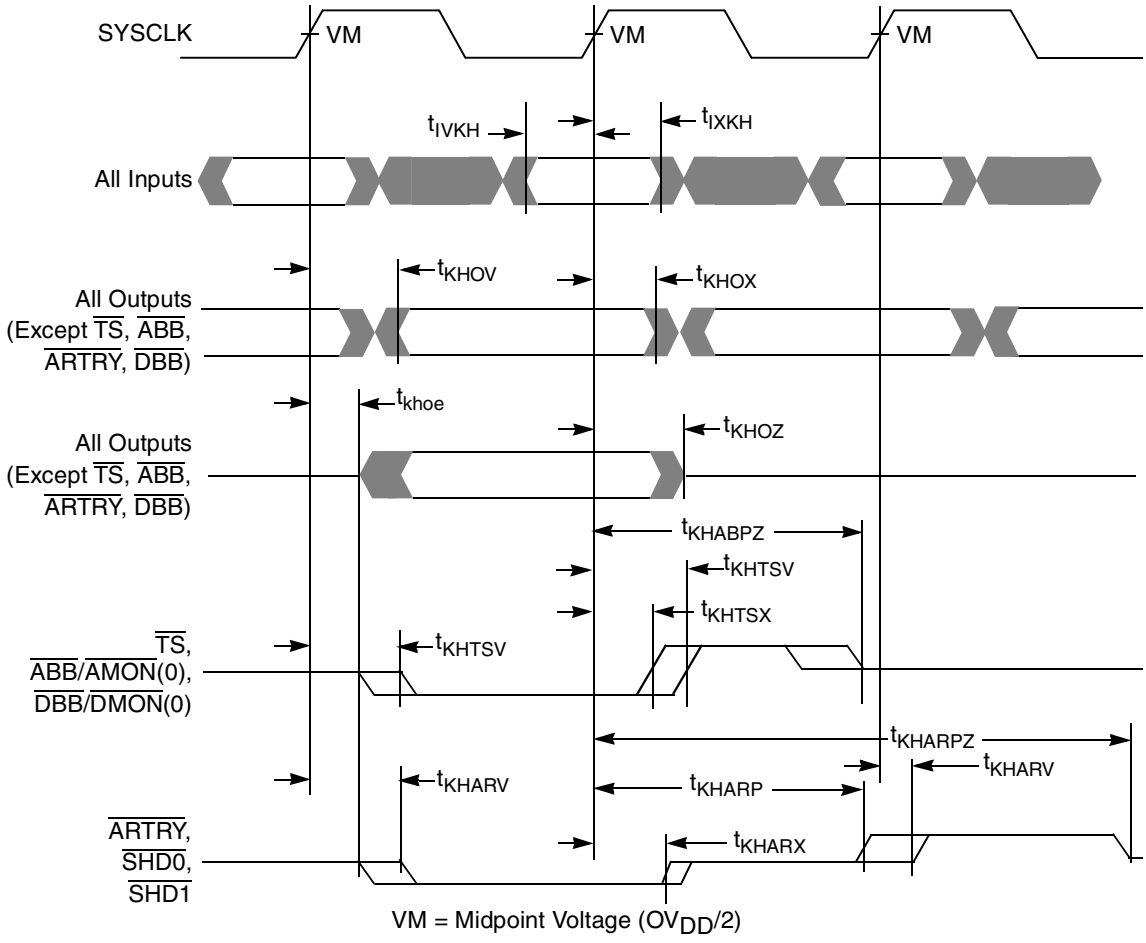


Figure 6. Input/Output Timing Diagram

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

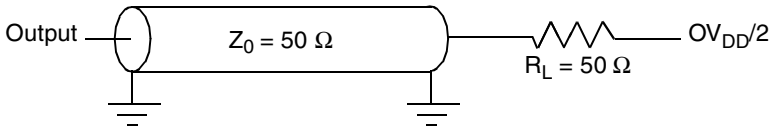


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

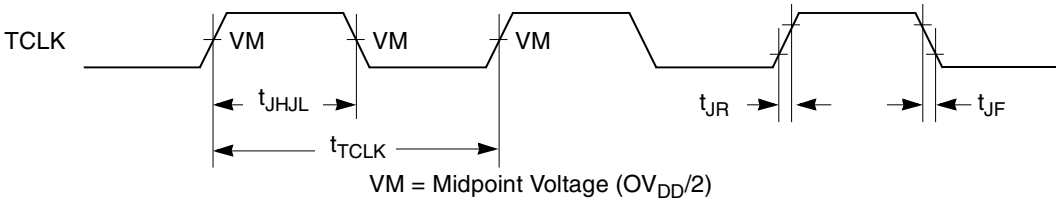
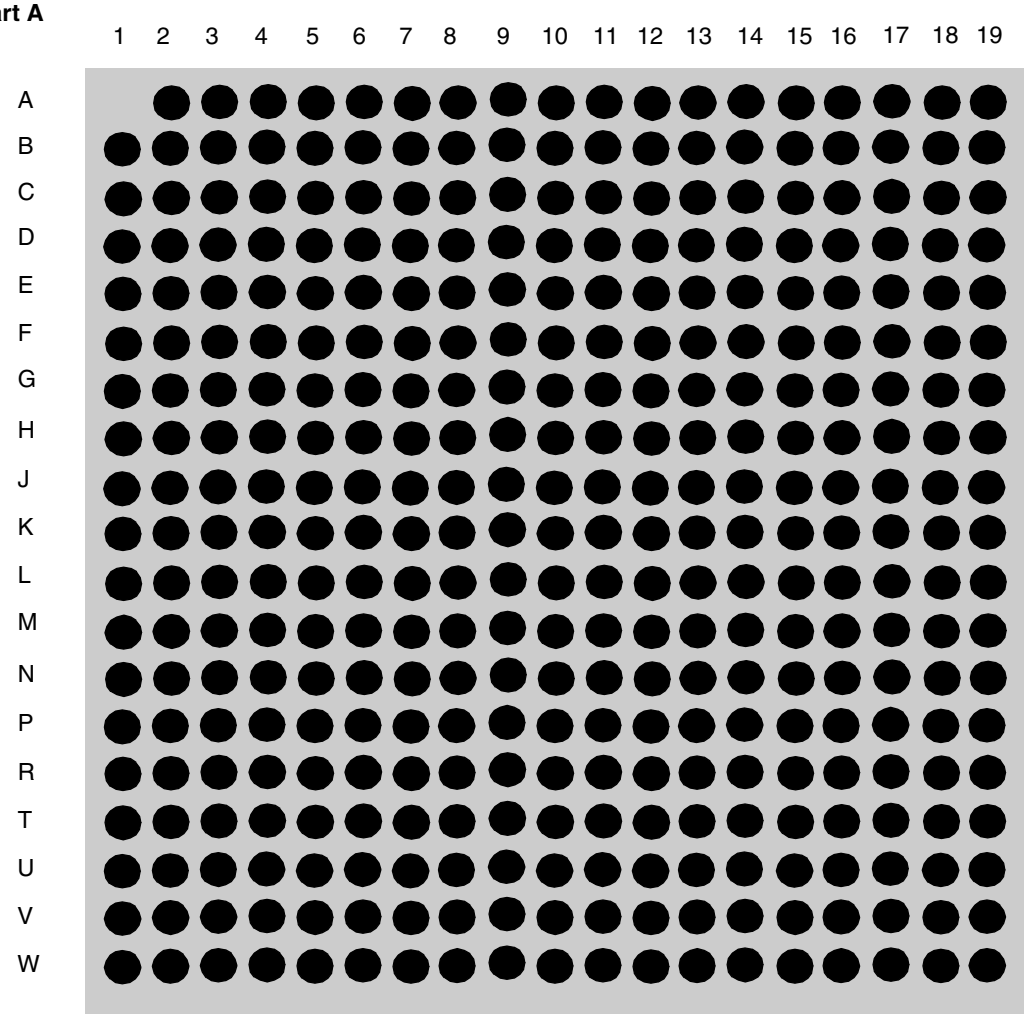


Figure 12. JTAG Clock Input Timing Diagram

5 Pin Assignments

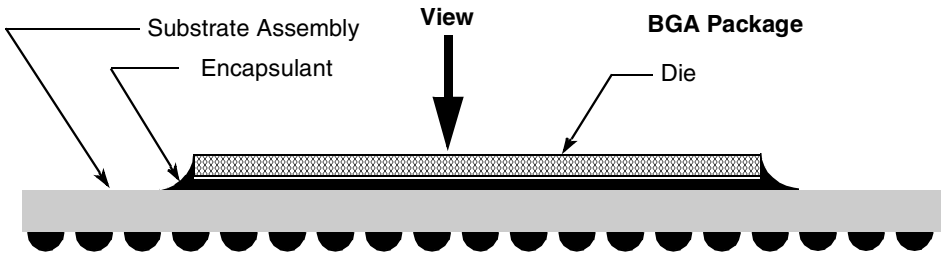
Figure 16, part A shows the pinout for the MPC7410, 360 CBGA, 360 HCTE, and 360 HCTE Lead Free C5 Spheres packages as viewed from the top surface. Figure 16, part B shows the side profile of the CBGA and HCTE_CBGA packages to indicate the direction of the top surface view. Figure 16, part C shows the side profile of the HCTE_LGA package to indicate the direction of the top surface view.

Part A



Not to Scale

Part B



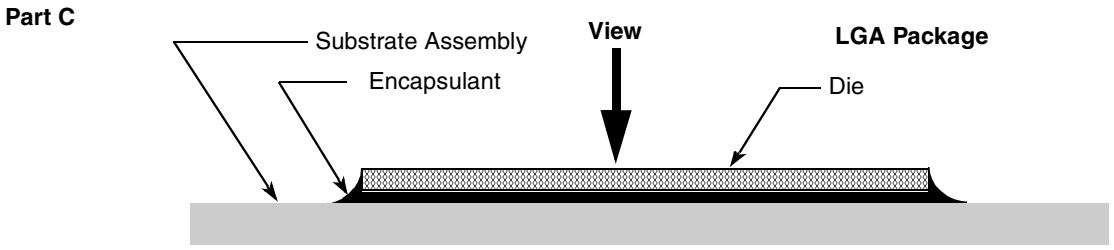


Figure 16. Pinout of the MPC7410, 360 CBGA and 360 HCTE Packages as Viewed from the Top Surface

6 Pinout Listings

Table 12 provides the pinout listing for the MPC7410 360 CBGA, 360 HCTE packages.

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	BVSEL	
$\overline{\text{AACK}}$	N3	Low	Input	BVSEL	—
$\overline{\text{ABB}}$	L7	Low	Output	BVSEL	12, 16
AP[0:3]	C4, C5, C6, C7	High	I/O	BVSEL	—
$\overline{\text{ARTRY}}$	L6	Low	I/O	BVSEL	—
AV_{DD}	A8	—	Input	V_{DD}	—
$\overline{\text{BG}}$	H1	Low	Input	BVSEL	—
$\overline{\text{BR}}$	E7	Low	Output	BVSEL	—
BVSEL	W1	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{CHK}}$	K11	Low	Input	BVSEL	2, 8, 9
$\overline{\text{CI}}$	C2	Low	I/O	BVSEL	—
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	BVSEL	—
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	BVSEL	—
CLK_OUT	E3	High	Output	BVSEL	—
$\overline{\text{DBB}}$	K5	Low	Output	BVSEL	12, 16
$\overline{\text{DBG}}$	K1	Low	Input	BVSEL	—
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	BVSEL	—

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	BVSEL	—
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	BVSEL	—
$\overline{\text{DRDY}}$	K9	Low	Output	BVSEL	6, 8, 13
$\overline{\text{DBWO}}$ DTI[0]	D1	Low	Input	BVSEL	—
DTI[1:2]	H6, G1	High	Input	BVSEL	5, 10, 13
$\overline{\text{EMODE}}$	A3	Low	Input	BVSEL	7, 10
$\overline{\text{GBL}}$	B1	Low	I/O	BVSEL	—
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	N/A	—
$\overline{\text{HIT}}$	B5	Low	Output	BVSEL	6, 8
$\overline{\text{HRESET}}$	B6	Low	Input	BVSEL	—
$\overline{\text{INT}}$	C11	Low	Input	BVSEL	—
L1_TSTCLK	F8	High	Input	BVSEL	2
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	L2VSEL	—
L2ADDR[17:18]	K19,W19	High	Output	L2VSEL	8
$L2AV_{DD}$	L13	—	Input	V_{DD}	—
$\overline{\text{L2CE}}$	P17	Low	Output	L2VSEL	—
L2CLK_OUTA	N15	High	Output	L2VSEL	—
L2CLK_OUTB	L16	High	Output	L2VSEL	—
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	L2VSEL	—
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	L2VSEL	—
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15	—	—	N/A	11
L2SYNC_IN	L14	High	Input	L2VSEL	—
L2SYNC_OUT	M14	High	Output	L2VSEL	—
L2_TSTCLK	F7	High	Input	BVSEL	2

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	N/A	—

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{\text{L2CE}}$, $\overline{\text{L2WE}}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:18], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD}, GND, $\overline{\text{HRESET}}$, or ¬$\overline{\text{HRESET}}$. For the MPC7410 the L2 bus only supports 2.5- and 1.8-V options. The default selection, if L2VSEL is left unconnected, is 2.5-V operation. For the MPC7410 the processor bus supports 3.3-, 2.5-, and 1.8-V options. The default selection, if BVSEL is left unconnected, is 3.3-V operation. Refer to Table 2 for supported BVSEL and L2VSEL settings.
4. PLL_CFG[0:3] must remain stable during operation; should only be changed during the assertion of $\overline{\text{HRESET}}$ or during sleep mode and must adhere to the internal PLL-relock time requirement.
5. Ignored input in 60x bus mode.
6. Unused output in 60x bus mode. Signal is three-stated in 60x mode.
7. Deasserted (pulled high) at $\overline{\text{HRESET}}$ negation for 60x bus mode. Asserted (pulled low) at $\overline{\text{HRESET}}$ negation for MPX bus mode.
8. Uses one of nine existing no connects in the MPC750 360 BGA package.
9. Internal pull up on die. Pulled-up signals are V_{DD} based.
10. Reuses MPC750 $\overline{\text{DRTRY}}$, $\overline{\text{DBDIS}}$, and TLBISYNC pins (DTI1, DTI2, and $\overline{\text{EMODE}}$, respectively).
11. The VOLTDET pin position on the MPC750 360 BGA package is now an $L2OV_{DD}$ pin on the MPC7410 360 package.
12. Output only for MPC7410, was I/O for MPC750.
13. MPX bus mode only.
14. If necessary, to overcome the internal pull-up resistance and ensure this input will recognize a low signal, a pull-down resistance less than 250 Ω should be used.
15. $\overline{\text{MCP}}$ minimum pulse width: asynchronous, falling-edge input needs to be held asserted for a minimum of 2 cycles to guarantee that it is latched by the processor.
16. In MPX bus mode the $\overline{\text{ABB}}$ signal is called $\overline{\text{AMON}}$ and the $\overline{\text{DBB}}$ signal is called $\overline{\text{DMON}}$. These signals are not a requirement of the MPX bus protocol and may not be available on future products.

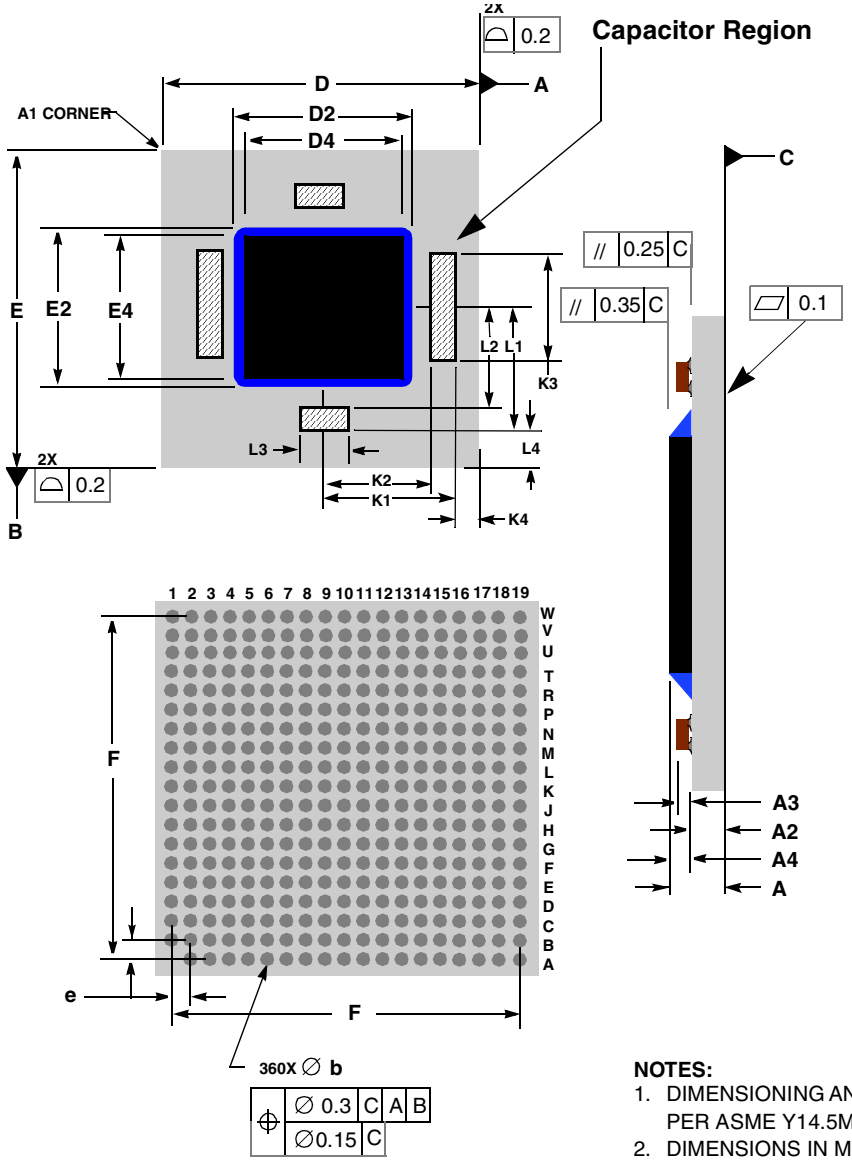
7.5 Package Parameters for the MPC7410, 360 HCTE_LGA

The package parameters are as listed here. The package type is the 25 × 25 mm, 360 high coefficient of thermal expansion LGA package (HCTE_LGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 land array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3ppm/°C

7.5.1 Mechanical Dimensions for the MPC7410, 360 HCTE_LGA

Figure 19 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 HCTE_LGA package.



	Millimeters	
DIM	MIN	MAX
A	1.92	2.20
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.90
b	0.79	0.99
D	25.00 BSC	
D2	—	12.50
D4	6.00	9.00
e	1.27 BSC	
E	25.00 BSC	
E2	—	14.30
E4	8.00	11.00
F	22.86 BSC	
K1	—	9.75
K2	6.46	—
K3	8.20	8.60
K4	2.75	—
L1	—	9.50
L2	6.94	—
L3	3.10	3.30
L4	3.00	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A PAD MISSING FROM THE ARRAY.

Figure 19. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410, 360 HCTE_LGA Package

MPC7410 core, and the phase adjustment range that the L2 DLL supports. Table 14 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 133 MHz. Sample core-to-L2 frequencies for the MPC7410 is shown in Table 14. In this example, shaded cells represent settings that, for a given core frequency, result in L2 frequencies that do not comply with the minimum and maximum L2 frequencies listed in Table 10.

Table 14. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3	÷3.5	÷4
350	350	233	175	140	—	—	—
366	366	244	183	147	—	—	—
400	400	266	200	160	133	—	—
433	—	288	216	173	144	—	—
450	—	300	225	180	150	—	—
466	—	311	233	186	155	133	—
500	—	333	250	200	166	143	—

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz.

8.2 PLL and DLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC7410 to supply power to the PLL and DLL, respectively. Both AV_{DD} and $L2AV_{DD}$ can be supplied power from the V_{DD} power plane. High frequency noise in the 500 kHz to 10 MHz resonant frequency range of the PLL on the V_{DD} power plane could affect the stability of the internal clocks.

On systems that use the MPC7410 HCTE device, the AV_{DD} and $L2AV_{DD}$ input signals should both implement the circuit shown in Figure 21.

On systems that use the MPC7410 CBGA device, the $L2AV_{DD}$ input should implement the circuit shown in Figure 21.

When selecting which filter to use on the AV_{DD} input of the MPC7410 CBGA device specifically, system designers should refer to Erratum No. 18 in the *MPC7410 RISC Microprocessor Chip Errata* (MPC7410CE). The AV_{DD} input of the MPC7410 CBGA device is sensitive to system noise on both the V_{DD} power plane, as described above, and the OV_{DD} power plane as described in the Erratum No. 18. With these AV_{DD} sensitivities to OV_{DD} and V_{DD} noise, care must be taken when selecting the filter circuit for the AV_{DD} input of the MPC7410 CBGA device. Erratum No. 18 does not apply to the AV_{DD} input of the MPC7401 HCTE device, nor does it affect the $L2AV_{DD}$ input of either the HCTE or the CBGA device.

As described in Erratum No. 18, when there is a high amount of noise on the OV_{DD} power plane due to I/O switching rates, it is possible for the OV_{DD} noise to couple into the PLL supply voltage (AV_{DD}) internal to the MPC7410 CBGA package. It is the recommendation of Freescale, that new designs using the MPC7410 CBGA package provide the ability to implement either filter shown in Figure 21 and Figure 22 at the AV_{DD} input. Existing designs that implemented Figure 21 on AV_{DD} may never experience the error described in Erratum No. 18. Both new and

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used; the remainder of the L2 interface may be left unterminated.

8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 23).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the driver impedance measurement circuit described above.

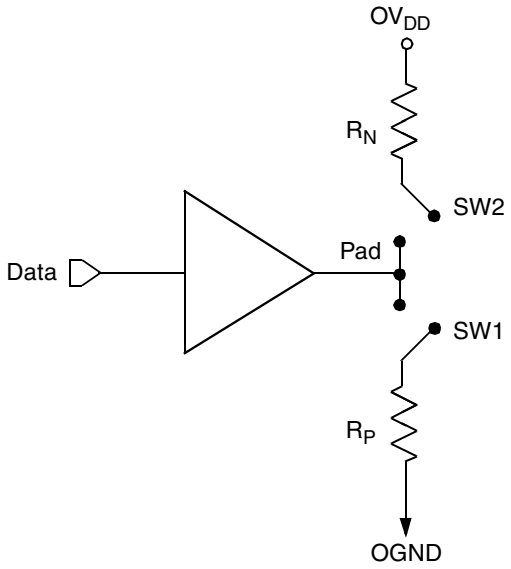


Figure 23. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 24. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

Table 16. Document Revision History (continued)

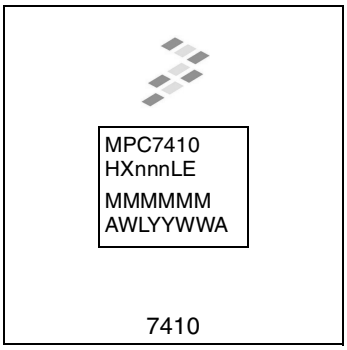
Revision	Date	Substantive Change(s)
5	4/13/2005	Section numbering revised. In all previous versions, section numbering began with '1.' These extra '1's' were deleted. For example, previously numbered section 1.8.2 changed to 8.2.
		Section 7.1—added CTE value for HCTE package. Corrected minimum module height from 2.65 mm to 2.72 mm per Figure 17.
		Section 3—added HCTE_LGA (VS package descriptor) package description which is the HCTE_CBGA (HX package descriptor) with the spheres removed.
		Table 4—generalized 'HCTE CBGA' column to 'HCTE' to include both HCTE_CBGA and HCTE_LGA package thermal characteristics.
		Section 5—added HCTE_LGA package. The HCTE_LGA has the same pin assignments as the CBGA and HCTE_CBGA packages. Added side view Part C for HCTE_LGA.
		Section 6—added HCTE_LGA package (VS package descriptor). The HCTE_LGA has the same pinout listing as the CBGA and HCTE packages.
		Section 7.3—added HCTE_LGA package parameters.
		Section 7.4—added HCTE_LGA package mechanical dimensions.
		Table 17—added HCTE_LGA package (VS package descriptor) to part numbering nomenclature.
4	—	Table 5—Changed measurement test condition I_{OH} from -6mA to –5 mA for V_{OH} and I_{OL} from 6 mA to 5 mA for V_{OL} per Product Bulletin.
		Section 1.8.2—revised text regarding AV_{DD} filter selection for the CBGA package.
3	—	Table 6—Changed note 1 to specify that OV_{DD} and $L2OV_{DD}$ power is typically <5% of V_{DD} power.
		Figure 17—revised diagram and dimensions to specify 'cap regions' versus individual cap measurements. Moved individual capacitor placement to separate figure.
		Figure 18—Added this figure to show each individual capacitor placement and value.
		Figure 22—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK.
2	—	Public release, includes Rev 1.1 changes.
		Section 1.7.2—added package capacitor values.
		Section 1.8.6—added recommendation that strong pull-up/down resistors be used on the PLL_CFG[0:3] signals.
		Table 8—removed mode input setup and hold times. These inputs adhere to the general input setup and hold specifications.
		Figure 5—revised mode input diagram to show sample points around $\overline{\text{HRESET}}$ negation.
		Section 1.3—added HCTE package description.
		Figure 22—added note 6 to emphasize that COP emulator and target board need to be able to drive $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ independently to the CPU.
		Section 1.8.2—revised section for HCTE package. Added text and figure for AV_{DD} filter for the CBGA package.
		Section 1.8.6—removed $\overline{\text{AACK}}$, $\overline{\text{TEA}}$, and $\overline{\text{TS}}$ from control signals requiring pull-ups. Removed $\overline{\text{TBST}}$ from snooped transfer attribute list. $\overline{\text{TBST}}$ is an output and is not snooped.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1.0	—	Section 1.3 and Table 3—revised OV_{DD} from 3.3 V ± 100 mV to 3.3 V ± 165 mV.
		Table 13—removed unsupported PLL configurations.
		Table 12—added note 15 for minimum $\overline{MCP}$ pulse width, correct note 3 for 3.3-V processor bus support.
		Table 13—revised note 3 to include emulator tool development.
		Table 14—removed unsupported Core-to-L2 example frequencies.
		Section 1.8.8—updated heat sink vendors list.
		Section 1.8.8.2—updated interface vendors list.
		Table 1—updated voltage sequencing requirements notes 3 and 4.
		Table 4—Updated/added thermal characteristics.
		Table 5—removed table and TAU related information, TAU is no longer supported.
		Table 6—updated I_{in} and I_{TSI} leakage current specs.
		Section 1.8.3—removed section.
		Section 1.10—reformatted section.
		Section 1.8.6—changed recommended pull-up resistor value to 1 kW–5 kW. Added $\overline{AACK}$, $\overline{TEA}$, and $\overline{TS}$ to control signals needing pull-ups. Added pull-up resistor value recommendation for L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$ factory test signals.
		Section 1.8.7—revised text regarding connection of $\overline{TRST}$. Combined Figure 22, Figure 23, and Table 17, into Figure 21.
		Table 7—corrected min VCO frequencies from 450 to 700 MHz to match min processor frequency of 350 MHz.
		Table 2—added note 3 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V OV_{DD}.
		Table 3—added notes 5 and 6 to clarify BVSEL for revisions prior to Rev. E which do not support 3.3 V OV_{DD}.
		Table 5—added note 8 regarding DC voltage limits for JTAG signals.

10.3 Part Marking

Parts are marked as the example shown in Figure 31.



HCTE_CBGA

Notes:

MMMMMM is the 6-digit mask number.
AWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 31. Part Marking for HCTE_CBGA Device

How to Reach Us:

Home Page:
www.freescale.com

email:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-0047 Japan
0120 191014
+81 3 3440 3569
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@
hibbertgroup.com

MPC7410EC
Rev. 6.1
11/2007

freescale™
semiconductor