Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410thx400le

  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32 Kbyte, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32 Kbyte, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-Kbyte, 1-Mbyte, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-Kbyte), 64-byte (1-Mbyte), or 128-byte (2-Mbyte) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256 Kbytes, 512 Kbytes, 1 Mbyte, or 2 Mbytes of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Maximum Value	Unit	Notes
Rework temperature	T_{rwk}	260	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.8 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

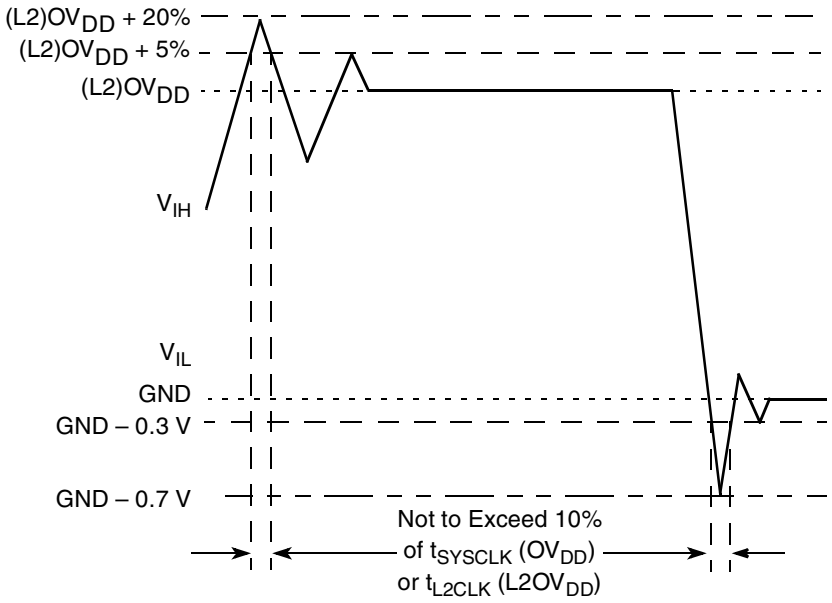


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.8 V ± 100 mV	V	—
PLL supply voltage		AV_{DD}	1.8 V ± 100 mV	V	—
L2 DLL supply voltage		$L2AV_{DD}$	1.8 V ± 100 mV	V	—
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 100 mV	V	—
	BVSEL = $\overline{\text{HRESET}}$	OV_{DD}	2.5 V ± 100 mV	V	—
	BVSEL = ¬$\overline{\text{HRESET}}$ or BVSEL = 1	OV_{DD}	3.3 V ± 165 mV	V	2, 3
L2 bus supply voltage	L2VSEL = 0	$L2OV_{DD}$	1.8 V ± 100 mV	V	—
	L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1	$L2OV_{DD}$	2.5 V ± 100 mV	V	—
Input voltage	Processor bus and JTAG signals	V_{in}	GND to OV_{DD}	V	—
	L2 bus	V_{in}	GND to $L2OV_{DD}$	V	—
Die-junction temperature		T_j	0 to 105	°C	—

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a recommended OV_{DD} value of 2.5 V ± 100 mV for BVSEL = 1.
3. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support BVSEL = ¬$\overline{\text{HRESET}}$.

Table 4 provides the package thermal characteristics for the MPC7410.

Table 4. Package Thermal Characteristics

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	18	20	°C/W	1, 2
Junction-to-ambient thermal resistance, 1m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	16	°C/W	1, 2
Junction-to-ambient thermal resistance, 2m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	13	15	°C/W	1, 2
Junction-to-board thermal resistance	$R_{\theta JB}$	9	11	°C/W	3

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 8. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
Input setup	t_{IVKH}	1.0	—	ns	4
Input hold	t_{IXKH}	0	—	ns	4
Output valid times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSV} t_{KHARV} t_{KHOV}	 — — —	 3.0 2.3 3.0	ns	5, 6
Output hold times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	5
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	9
SYSCLK to output high impedance (all except $\overline{ABB}$/$\overline{AMON}$(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/$\overline{DMON}$(0), $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{ABB}$/$\overline{AMON}$(0), $\overline{DBB}$/$\overline{DMON}$(0) high impedance after precharge	t_{KHABPZ}	—	1	t_{SYSCLK}	3, 7, 9
Maximum delay to $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 8, 9

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

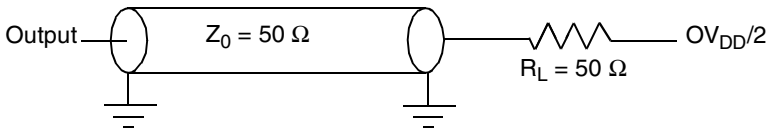


Figure 4. AC Test Load

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

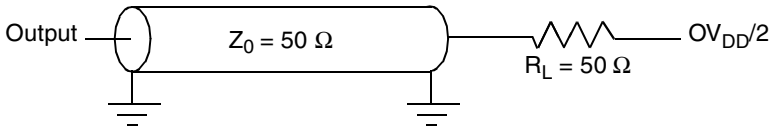


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

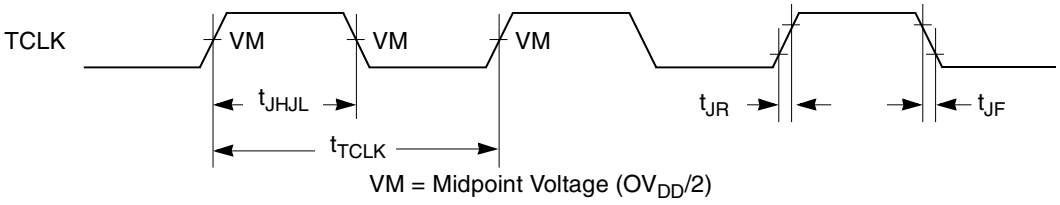


Figure 12. JTAG Clock Input Timing Diagram

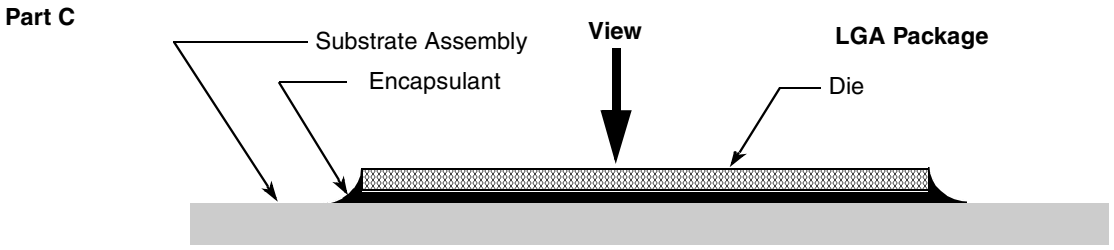


Figure 16. Pinout of the MPC7410, 360 CBGA and 360 HCTE Packages as Viewed from the Top Surface

6 Pinout Listings

Table 12 provides the pinout listing for the MPC7410 360 CBGA, 360 HCTE packages.

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	BVSEL	
$\overline{\text{AACK}}$	N3	Low	Input	BVSEL	—
$\overline{\text{ABB}}$	L7	Low	Output	BVSEL	12, 16
AP[0:3]	C4, C5, C6, C7	High	I/O	BVSEL	—
$\overline{\text{ARTRY}}$	L6	Low	I/O	BVSEL	—
AV_{DD}	A8	—	Input	V_{DD}	—
$\overline{\text{BG}}$	H1	Low	Input	BVSEL	—
$\overline{\text{BR}}$	E7	Low	Output	BVSEL	—
BVSEL	W1	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{CHK}}$	K11	Low	Input	BVSEL	2, 8, 9
$\overline{\text{CI}}$	C2	Low	I/O	BVSEL	—
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	BVSEL	—
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	BVSEL	—
CLK_OUT	E3	High	Output	BVSEL	—
$\overline{\text{DBB}}$	K5	Low	Output	BVSEL	12, 16
$\overline{\text{DBG}}$	K1	Low	Input	BVSEL	—
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	BVSEL	—

Table 13. MPC7410 Microprocessor PLL Configuration (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0111	4.5x	2x	—	—	—	—	375 (750)	450 (900)	—
1011	5x	2x	—	—	—	375 (750)	416 (833)	500 (1000)	—
1001	5.5x	2x	—	—	366 (733)	412 (825)	458 (916)	—	—
1101	6x	2x	—	—	400 (800)	450 (900)	500 (1000)	—	—
0101	6.5x	2x	—	—	433 (866)	488 (967)	—	—	—
0010	7x	2x	—	350 (700)	466 (933)	—	—	—	—
0001	7.5x	2x	—	375 (750)	500 (1000)	—	—	—	—
1100	8x	2x	—	400 (800)	—	—	—	—	—
0000	9x	2x	—	450 (900)	—	—	—	—	—
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL off		PLL off, no core clocking occurs						

Notes:

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and third-party emulator tool development only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7410 regardless of the SYSCLK input.
5. PLL-off mode should not be used during chip power-up sequencing.

The MPC7410 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC7410. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC7410 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the

existing designs should qualify both AV_{DD} filter solutions, and the filter providing the most robust margin should be implemented.

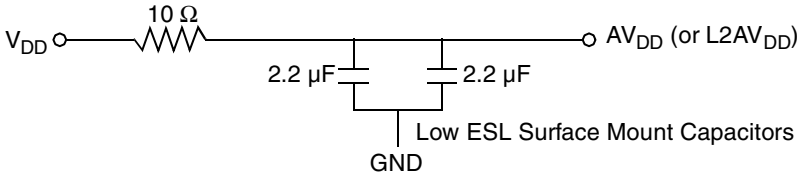


Figure 21. PLL Power Supply Filter Circuit No.1

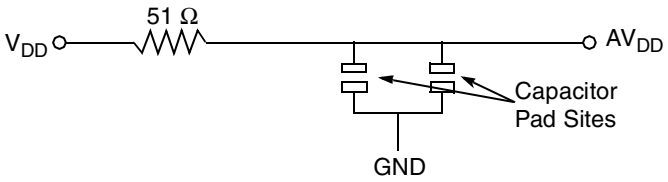


Figure 22. PLL Power Supply Filter Circuit No. 2

The filter circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. A separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

It is the recommendation of Freescale, that systems that implement the AV_{DD} filter shown in Figure 22 design in the pads for the removed capacitors (shown in Figure 21), to provide for the possible reintroduction of the filter in Figure 21. This would be necessary in case there is a planned transition from the CBGA package to the HCTE package of the MPC7410.

8.3 Decoupling Recommendations

Due to the MPC7410 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7410 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7410 system, and the MPC7410 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the MPC7410. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations, where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used; the remainder of the L2 interface may be left unterminated.

8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 23).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the driver impedance measurement circuit described above.

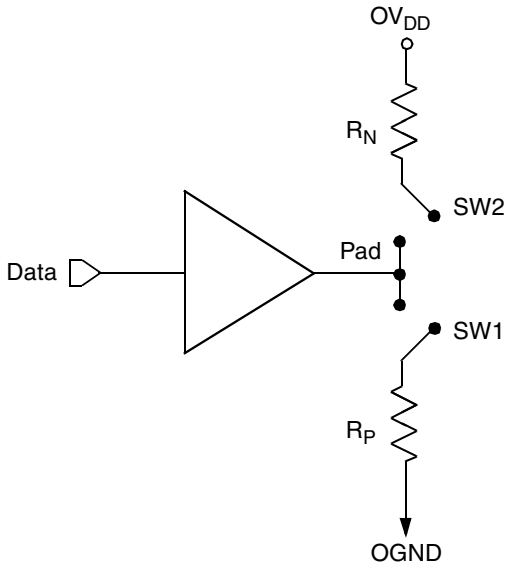


Figure 23. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 24. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 24 describes the alternate driver impedance measurement circuit.

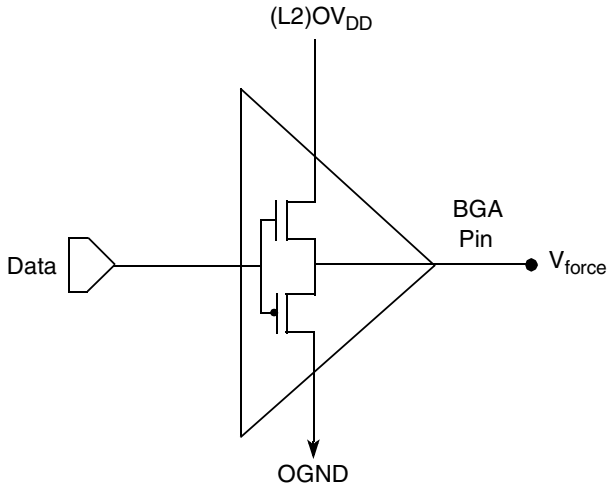


Figure 24. Alternate Driver Impedance Measurement Circuit

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.8 V, OV_{DD} = 2.5 V, T_j = 0° – 105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5–54.3	42.7–54.1	Z_0	Ω
R_P	37.3–55.3	39.3–50.0	Z_0	Ω

8.6 Pull-Up Resistor Requirements

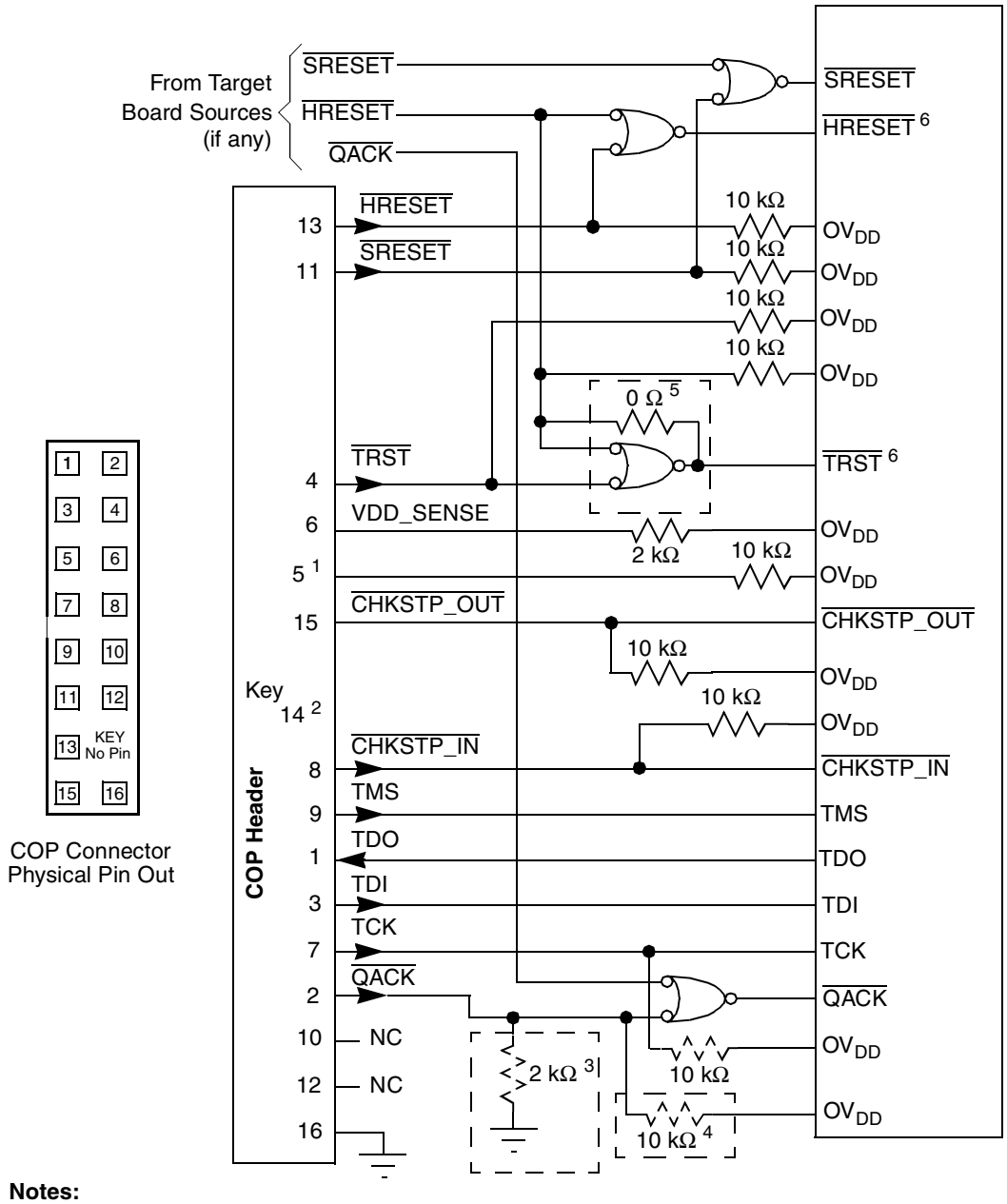
The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7410. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 25. COP Connector Diagram

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 25; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 25 is usually connected to the PCI bridge chip in a system and is an input to the MPC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

8.8 Thermal Management Information

This section provides thermal management information for the MPC7410 for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods such as spring clip to holes in the printed circuit board or with screws and springs to the printed circuit board; see Figure 26 for the BGA package and Figure 27 for the LGA package. This spring force should not exceed 5.5 pounds of force. Note that care should be taken to avoid focused forces being applied to die corners and/or edges when mounting heat sinks.

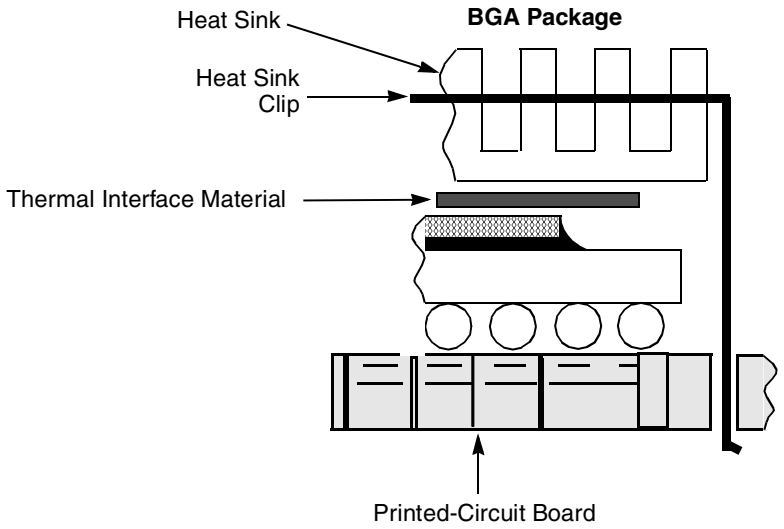


Figure 26. BGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

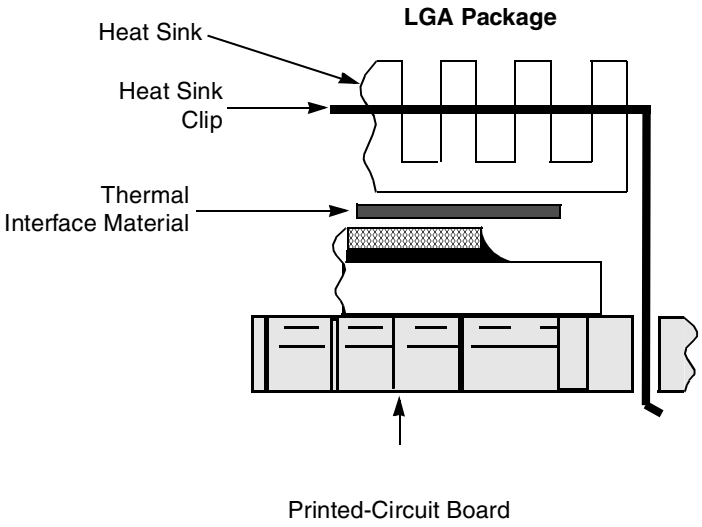


Figure 27. LGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

The board designer can choose between several types of heat sinks to place on the MPC7410. There are several commercially-available heat sinks for the MPC7410 from the following vendors:

Aavid Thermalloy 70 Commercial Street, Suite 200 Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

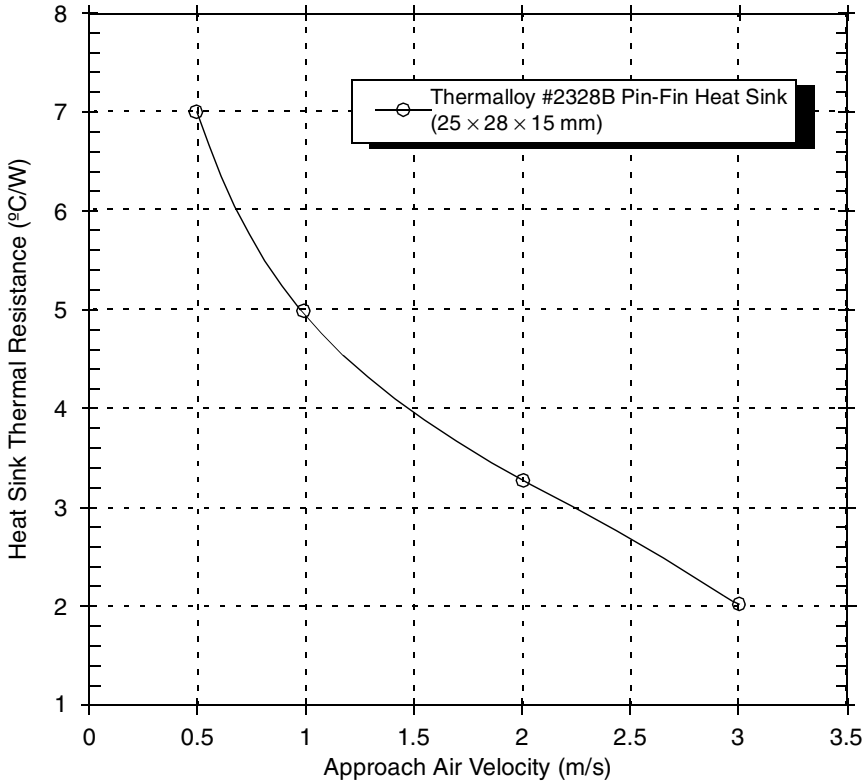


Figure 30. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

9 Document Revision History

Table 16 provides a revision history for this hardware specification.

Table 16. Document Revision History

Revision	Date	Substantive Change(s)
6.1	11/16/2007	Updated Table 17 and Table 19 to show the VU package is available as an MC prefix device compared to an MPC prefix for the other package types; this was done to match the specification documents with the device ordering and part marking information. Updated title of Table 19 to reflect correct name of referenced document and updated respective document order information below table. Updated notes in Table 1–Table 3 replacing references to MPC7410RX*nnn*LE with M*xx*7410*xxnnn*LE since notes to apply to all the available packages types.
6	8/14/2007	Updated Table 4 thermal information: • Deleted rows on single-layer (1s) boards. • CBGA package $R_{\theta JMA}$ for natural convection for four layer boards changed from 17 to 18 °C/W. • HCTE package $R_{\theta JMA}$ for natural convection for four layer boards changed from 22 to 20 °C/W. • HCTE package $R_{\theta JMA}$ for 200 ft./min airflow for four layer boards changed from 19 to 16 °C/W with airflow rate specification changed from 200 ft./min to 1 m/sec. • HCTE package $R_{\theta JMA}$ for 400 ft./min airflow for four layer boards changed from 18 to 15 °C/W with airflow rate specification changed from 400 ft./min to 2 m/sec. • CBGA package $R_{\theta JB}$ changed from 8 to 9°C/W. • HCTE package $R_{\theta JB}$ changed from 14 to 11°C/W. • Table 4 Notes 2 - 4 have been revised and updated; Note 5 is no longer used. Notes on table rows have been renumbered. Updated Figure 26 removing optional heat sink clip to package. Removed references in document to adhesive attached thermal solutions. Updated thermal solution vendor information in Section 8.8. Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information to document: • Added Section 7.2, “Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres). • Added Figure 18 for HCTE_CBGA Lead Free C5 Spheres package, similar to Figure 17 but with differences in dimensions A, A1, and b in the figure’s dimension table. • Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information in Table 17 and Table 19. • Changed part marking example in Figure 31 to an HCTE_CBGA device.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
5	4/13/2005	Section numbering revised. In all previous versions, section numbering began with '1.' These extra '1's' were deleted. For example, previously numbered section 1.8.2 changed to 8.2.
		Section 7.1—added CTE value for HCTE package. Corrected minimum module height from 2.65 mm to 2.72 mm per Figure 17.
		Section 3—added HCTE_LGA (VS package descriptor) package description which is the HCTE_CBGA (HX package descriptor) with the spheres removed.
		Table 4—generalized 'HCTE CBGA' column to 'HCTE' to include both HCTE_CBGA and HCTE_LGA package thermal characteristics.
		Section 5—added HCTE_LGA package. The HCTE_LGA has the same pin assignments as the CBGA and HCTE_CBGA packages. Added side view Part C for HCTE_LGA.
		Section 6—added HCTE_LGA package (VS package descriptor). The HCTE_LGA has the same pinout listing as the CBGA and HCTE packages.
		Section 7.3—added HCTE_LGA package parameters.
		Section 7.4—added HCTE_LGA package mechanical dimensions.
		Table 17—added HCTE_LGA package (VS package descriptor) to part numbering nomenclature.
4	—	Table 5—Changed measurement test condition I_{OH} from -6mA to –5 mA for V_{OH} and I_{OL} from 6 mA to 5 mA for V_{OL} per Product Bulletin.
		Section 1.8.2—revised text regarding AV_{DD} filter selection for the CBGA package.
3	—	Table 6—Changed note 1 to specify that OV_{DD} and $L2OV_{DD}$ power is typically <5% of V_{DD} power.
		Figure 17—revised diagram and dimensions to specify 'cap regions' versus individual cap measurements. Moved individual capacitor placement to separate figure.
		Figure 18—Added this figure to show each individual capacitor placement and value.
		Figure 22—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK.
2	—	Public release, includes Rev 1.1 changes.
		Section 1.7.2—added package capacitor values.
		Section 1.8.6—added recommendation that strong pull-up/down resistors be used on the PLL_CFG[0:3] signals.
		Table 8—removed mode input setup and hold times. These inputs adhere to the general input setup and hold specifications.
		Figure 5—revised mode input diagram to show sample points around $\overline{\text{HRESET}}$ negation.
		Section 1.3—added HCTE package description.
		Figure 22—added note 6 to emphasize that COP emulator and target board need to be able to drive $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ independently to the CPU.
		Section 1.8.2—revised section for HCTE package. Added text and figure for AV_{DD} filter for the CBGA package.
		Section 1.8.6—removed $\overline{\text{AACK}}$, $\overline{\text{TEA}}$, and $\overline{\text{TS}}$ from control signals requiring pull-ups. Removed $\overline{\text{TBST}}$ from snooped transfer attribute list. $\overline{\text{TBST}}$ is an output and is not snooped.

Table 16. Document Revision History (continued)

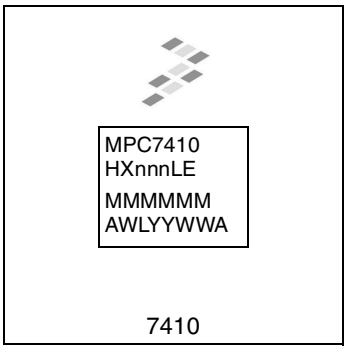
Revision	Date	Substantive Change(s)
1.1	—	Internal release.
		Table 12—added note 16 for $\overline{\text{ABB}}$/$\overline{\text{AMON}}$ and $\overline{\text{DBB}}$/$\overline{\text{DMON}}$ signal clarification.
		Table 12—changed $\overline{\text{CHK}}$ note 4 reference to note 2, signal is for factory test only. Changed previous note 4 ($\overline{\text{CHK}}$ related) to now provide additional PLL info.
		Table 1—modified maximum value for OV_{DD} from –0.3 to 3.465 to now be –0.3 to 3.6 and $L2OV_{DD}$ from –0.3 to 2.6 to now be –0.3 to 2.8. Modified note 6, OV_{DD} for revisions prior to Rev. 1.4 have maximum value for OV_{DD} of –0.3 to 2.8.
		Table 8—removed note 12. L2_TSTCLK is for factory use only (see Table 12, note 2).
		Section 1.10.2—revised section to include nomenclature tables for part markings not covered by this spec.
		Figure 2—added that under/overshoot for $L2OV_{DD}$ references t_{L2CLK} while OV_{DD} references t_{SYSCLK}.
		Table 4—added HCTE package (HX package descriptor) thermal characteristics.
		Section 1.5—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same pin assignments.
		Section 1.6—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same pinout listings.
		Section 1.7—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same package parameters and dimensions.
		Table 17—added HCTE package (HX package descriptor) to part numbering nomenclature.
		Table 21—added MPC7410THXnnnLE extended temperature HCTE package part numbers and part number specification document reference.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
0.3	—	Added 3.3 V support on the processor bus (BVSEL).
		Table 7—update typical and maximum power numbers for full-on mode in. Removed note 4. Reworded notes 2 and 3.
		Table 9, Note 2—removed reference to application note.
		Figure 17—corrected side view datum A to be datum C.
		Section 1.8.7—added $\overline{CI}$ and $\overline{WT}$ to transfer attribute signals requiring pull-ups.
		Section 1.8.7—added 1-kΩ pull-up recommendation to $\overline{GBL}$ when $\overline{GBL}$ is not connected.
		Table 2— added pull-down resistance necessary for internally pulled-up voltage select pins. Added 3.3-V support for BVSEL.
		Table 13—added note 14 for BVSEL, L2VSEL, and $\overline{TRST}$ pins to address pull-down resistance necessary for these internally pulled-up pins to recognize a low signal.
		Table 6—lowered 2.5 V CV_{IH} from 2.2 to 2.0 V to be compatible with V_{OH} of the MPC107. Added support for 3.3-V processor bus.
		Table 15—modified note 1, use L2CR[L2SL] for L2CLK frequency less than 150 MHz.
		Table 8—revised note 2 discussing for 3.3-V bus voltage support.
		Table 14—added note 5, do not use PL off during power-up sequence.
		Table 1—update output hold times (t_{L2CHOX}).
0.2	—	Corrected Section 1.3—technology from 0.13 µm to 0.18 µm.
		Updated Table 7—adds power consumption numbers; adds note on estimated decrease w/o AltiVec.
		Updated Table 8—adds minimum values for processor frequency and VCO frequency.
		Updated Table 9—input setup, output valid times, output hold times, SYSCLK to output high impedance.
		Updated Table 11—L2SYNC_IN to high impedance.
		Updated Figure 17—mechanical dimensions, adds capacitor pad dimensions.
0.1	—	Minor updates.
0	—	Initial release.

10.3 Part Marking

Parts are marked as the example shown in Figure 31.



HCTE_CBGA

Notes:

MMMMMM is the 6-digit mask number.
AWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 31. Part Marking for HCTE_CBGA Device