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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410thx500le

- The MPC7410 is implemented in a next generation process technology for core frequency improvement.
- The MPC7410 floating-point unit has been improved to make latency equal for double- and single-precision operations involving multiplication.
- The completion queue has been extended to eight slots.
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750 four-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback).

Some comments on the MPC7410 with respect to the MPC7400:

- The MPC7410 adds configurable direct-mapped SRAM capability to the L2 cache interface.
- The MPC7410 adds 32-bit interface support to the L2 cache interface. The MPC7410 implements a 19th L2 address pin (L2ASPARE on the MPC7400) in order to support additional address range.
- The MPC7410 removes support for 3.3-V I/O on the L2 cache interface.

Figure 1 shows a block diagram of the MPC7410.

2 Features

This section summarizes features of the MPC7410 implementation of the PowerPC architecture. Major features of the MPC7410 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)

- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754™ single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations

  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32 Kbyte, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32 Kbyte, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-Kbyte, 1-Mbyte, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-Kbyte), 64-byte (1-Mbyte), or 128-byte (2-Mbyte) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256 Kbytes, 512 Kbytes, 1 Mbyte, or 2 Mbytes of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Maximum Value	Unit	Notes
Rework temperature	T_{rwk}	260	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.8 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

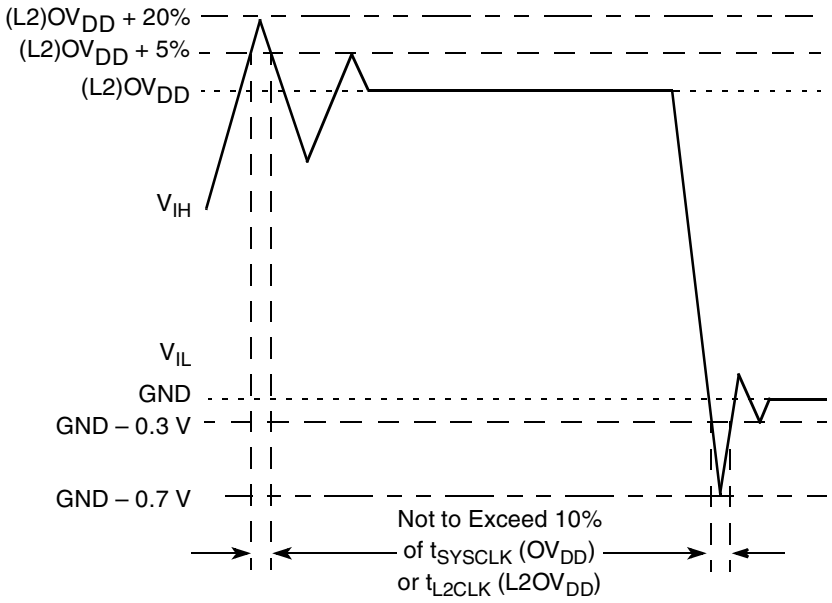


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

4.2.1 Clock AC Specifications

Table 7 provides the clock AC timing specifications as defined in Figure 3.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		400 MHz		450 MHz		500 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	350	400	350	450	350	500	MHz	1
VCO frequency	f_{VCO}	700	800	700	900	700	1000	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	133	33	133	33	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	7.5	30	ns	—
SYSCLK rise and fall time	t_{KR} and t_{KF}	—	0.5	—	0.5	—	0.5	ns/V	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter	—	—	±150	—	±150	—	±150	ps	4
Internal PLL-relock time	—	—	100	—	100	—	100	µs	5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurement are determined by the slew rates of the bus interface, rather than by time. As a result, the 0.5 ns rise/fall time spec of the 1.8- and 2.5-V bus interfaces is equivalent to the 1 ns rise/fall time of the 3.3-V bus interface. Both interfaces required a 2 V/ns slew rate. The slew rate is measured as a 1-V change (from 0.2 to 1.2 V) in 0.5 ns for the 1.8- and 2.5-V bus interfaces, whereas the 3.3-V bus interface required a 2-V change (from 0.4 to 2.4 V) in 1 ns.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short- and long-term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

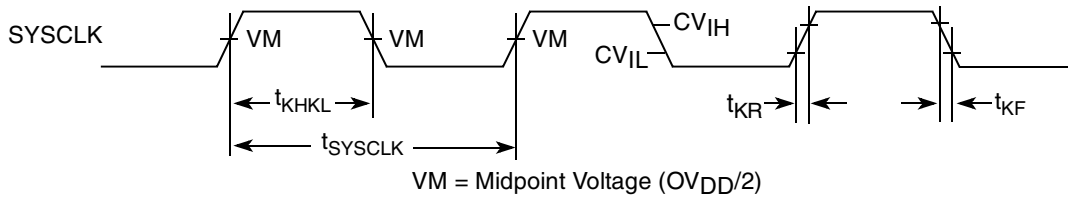


Figure 3. SYSCLK Input Timing Diagram

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

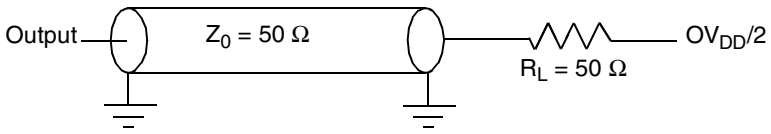


Figure 4. AC Test Load

4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 bus interface AC timing specifications for the MPC7410 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 10. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400, 450, 500 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} and t_{L2CF}	—	1.0	ns	1
Setup times: Data and parity	t_{DVL2CH}	1.5	—	ns	2
Input hold times: Data and parity	t_{DXL2CH}	—	0.0	ns	2
Valid times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOV}	 — — — —	 2.5 2.5 2.9 3.5	ns	3, 4
Output hold times All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOX}	 0.4 0.8 1.2 1.6	 — — — —	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOZ}	 — — — —	 2.0 2.5 3.0 3.5	ns	—

Notes:

1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 00 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 10 is recommended.

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

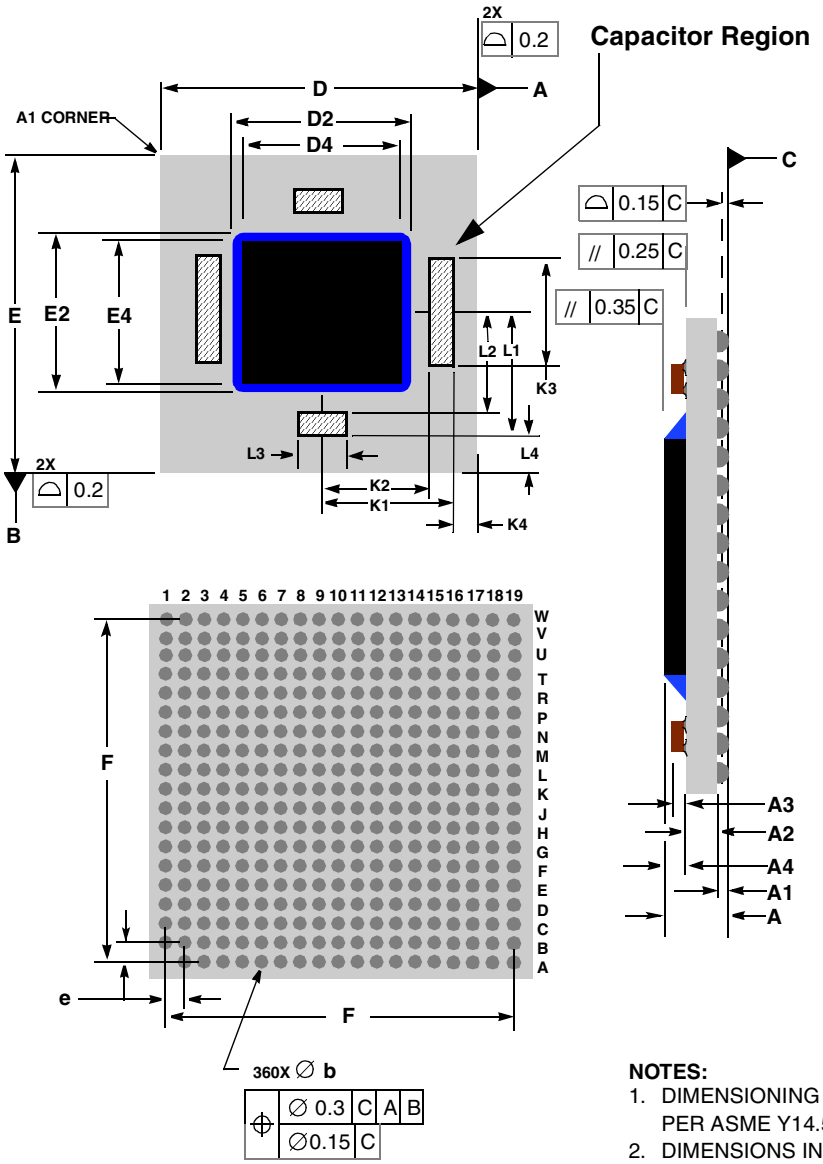
Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	BVSEL	—
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	BVSEL	—
$\overline{\text{DRDY}}$	K9	Low	Output	BVSEL	6, 8, 13
$\overline{\text{DBWO}}$ DTI[0]	D1	Low	Input	BVSEL	—
DTI[1:2]	H6, G1	High	Input	BVSEL	5, 10, 13
$\overline{\text{EMODE}}$	A3	Low	Input	BVSEL	7, 10
$\overline{\text{GBL}}$	B1	Low	I/O	BVSEL	—
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	N/A	—
$\overline{\text{HIT}}$	B5	Low	Output	BVSEL	6, 8
$\overline{\text{HRESET}}$	B6	Low	Input	BVSEL	—
$\overline{\text{INT}}$	C11	Low	Input	BVSEL	—
L1_TSTCLK	F8	High	Input	BVSEL	2
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	L2VSEL	—
L2ADDR[17:18]	K19,W19	High	Output	L2VSEL	8
$L2AV_{DD}$	L13	—	Input	V_{DD}	—
$\overline{\text{L2CE}}$	P17	Low	Output	L2VSEL	—
L2CLK_OUTA	N15	High	Output	L2VSEL	—
L2CLK_OUTB	L16	High	Output	L2VSEL	—
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	L2VSEL	—
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	L2VSEL	—
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15	—	—	N/A	11
L2SYNC_IN	L14	High	Input	L2VSEL	—
L2SYNC_OUT	M14	High	Output	L2VSEL	—
L2_TSTCLK	F7	High	Input	BVSEL	2

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
L2VSEL	A19	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{L2WE}}$	N16	Low	Output	L2VSEL	—
L2ZZ	G17	High	Output	L2VSEL	—
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	BVSEL	2
$\overline{\text{MCP}}$	B11	Low	Input	BVSEL	15
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	N/A	—
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	BVSEL	4
$\overline{\text{QACK}}$	B2	Low	Input	BVSEL	—
$\overline{\text{QREQ}}$	J3	Low	Output	BVSEL	—
$\overline{\text{RSRV}}$	D3	Low	Output	BVSEL	—
$\overline{\text{SHD0}}$	B3	Low	I/O	BVSEL	8
$\overline{\text{SHD1}}$	B4	Low	I/O	BVSEL	5, 8
$\overline{\text{SMI}}$	A12	Low	Input	BVSEL	—
$\overline{\text{SRESET}}$	E10	Low	Input	BVSEL	—
SYSCLK	H9	—	Input	BVSEL	—
$\overline{\text{TA}}$	F1	Low	Input	BVSEL	—
TBEN	A2	High	Input	BVSEL	—
$\overline{\text{TBST}}$	A11	Low	Output	BVSEL	—
TCK	B10	High	Input	BVSEL	—
TDI	B7	High	Input	BVSEL	9
TDO	D9	High	Output	BVSEL	—
$\overline{\text{TEA}}$	J1	Low	Input	BVSEL	—
TMS	C8	High	Input	BVSEL	9
$\overline{\text{TRST}}$	A10	Low	Input	BVSEL	9
$\overline{\text{TS}}$	K7	Low	I/O	BVSEL	—
TSIZ[0:2]	A9, B9, C9	High	Output	BVSEL	—
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	BVSEL	—
$\overline{\text{WT}}$	C3	Low	I/O	BVSEL	—

7.3 Mechanical Dimensions for the MPC7410, 360 CBGA and 360 HCTE_CBGA

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 CBGA and 360 HCTE_CBGA packages.



	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1.00
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.90
b	0.82	0.93
D	25.00 BSC	
D2	—	12.50
D4	6.00	9.00
e	1.27 BSC	
E	25.00 BSC	
E2	—	14.30
E4	8.00	11.00
F	22.86 BSC	
K1	—	9.75
K2	6.46	—
K3	8.20	8.60
K4	2.75	—
L1	—	9.50
L2	6.94	—
L3	3.10	3.30
L4	3.00	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410, 360 CBGA and 360 HCTE_CBGA Packages

7.5 Package Parameters for the MPC7410, 360 HCTE_LGA

The package parameters are as listed here. The package type is the 25 × 25 mm, 360 high coefficient of thermal expansion LGA package (HCTE_LGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 land array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3ppm/°C

MPC7410 core, and the phase adjustment range that the L2 DLL supports. Table 14 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 133 MHz. Sample core-to-L2 frequencies for the MPC7410 is shown in Table 14. In this example, shaded cells represent settings that, for a given core frequency, result in L2 frequencies that do not comply with the minimum and maximum L2 frequencies listed in Table 10.

Table 14. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3	÷3.5	÷4
350	350	233	175	140	—	—	—
366	366	244	183	147	—	—	—
400	400	266	200	160	133	—	—
433	—	288	216	173	144	—	—
450	—	300	225	180	150	—	—
466	—	311	233	186	155	133	—
500	—	333	250	200	166	143	—

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz.

8.2 PLL and DLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC7410 to supply power to the PLL and DLL, respectively. Both AV_{DD} and $L2AV_{DD}$ can be supplied power from the V_{DD} power plane. High frequency noise in the 500 kHz to 10 MHz resonant frequency range of the PLL on the V_{DD} power plane could affect the stability of the internal clocks.

On systems that use the MPC7410 HCTE device, the AV_{DD} and $L2AV_{DD}$ input signals should both implement the circuit shown in Figure 21.

On systems that use the MPC7410 CBGA device, the $L2AV_{DD}$ input should implement the circuit shown in Figure 21.

When selecting which filter to use on the AV_{DD} input of the MPC7410 CBGA device specifically, system designers should refer to Erratum No. 18 in the *MPC7410 RISC Microprocessor Chip Errata* (MPC7410CE). The AV_{DD} input of the MPC7410 CBGA device is sensitive to system noise on both the V_{DD} power plane, as described above, and the OV_{DD} power plane as described in the Erratum No. 18. With these AV_{DD} sensitivities to OV_{DD} and V_{DD} noise, care must be taken when selecting the filter circuit for the AV_{DD} input of the MPC7410 CBGA device. Erratum No. 18 does not apply to the AV_{DD} input of the MPC7401 HCTE device, nor does it affect the $L2AV_{DD}$ input of either the HCTE or the CBGA device.

As described in Erratum No. 18, when there is a high amount of noise on the OV_{DD} power plane due to I/O switching rates, it is possible for the OV_{DD} noise to couple into the PLL supply voltage (AV_{DD}) internal to the MPC7410 CBGA package. It is the recommendation of Freescale, that new designs using the MPC7410 CBGA package provide the ability to implement either filter shown in Figure 21 and Figure 22 at the AV_{DD} input. Existing designs that implemented Figure 21 on AV_{DD} may never experience the error described in Erratum No. 18. Both new and

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used; the remainder of the L2 interface may be left unterminated.

8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 23).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the driver impedance measurement circuit described above.

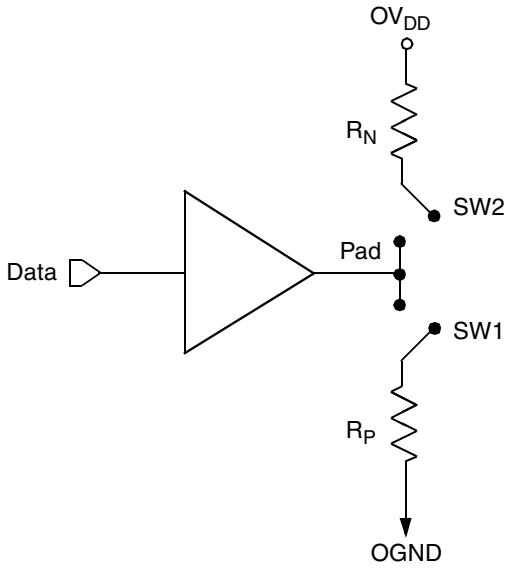


Figure 23. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 24. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 24 describes the alternate driver impedance measurement circuit.

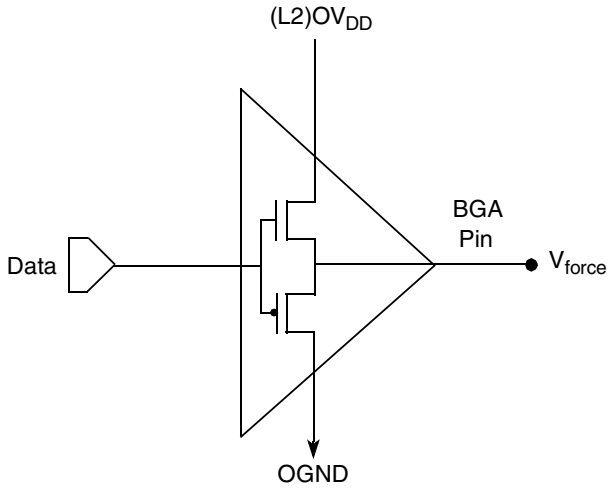


Figure 24. Alternate Driver Impedance Measurement Circuit

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.8 V, OV_{DD} = 2.5 V, T_j = 0° – 105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5–54.3	42.7–54.1	Z_0	Ω
R_P	37.3–55.3	39.3–50.0	Z_0	Ω

8.6 Pull-Up Resistor Requirements

The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on

the MPC7410 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode can be enabled (see the *MPC7410 RISC Microprocessor Family Users' Manual* for more information on this mode), or these signals may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

In systems where $\overline{\text{GBL}}$ is not connected and other devices may be asserting $\overline{\text{TS}}$ for a snoopable transaction while not driving $\overline{\text{GBL}}$ to the processor, we recommend that a strong (1 kΩ) pull-up resistor be used on $\overline{\text{GBL}}$. Note that the MPC7410 will only snoop transactions when $\overline{\text{GBL}}$ is asserted.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If parity checking is disabled through HID0, and parity generation is not required by the MPC7410 (note that the MPC7410 always generates parity), then all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

8.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 25 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 25, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 25 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

Figure 29 describes the thermal performance of selected thermal interface materials.

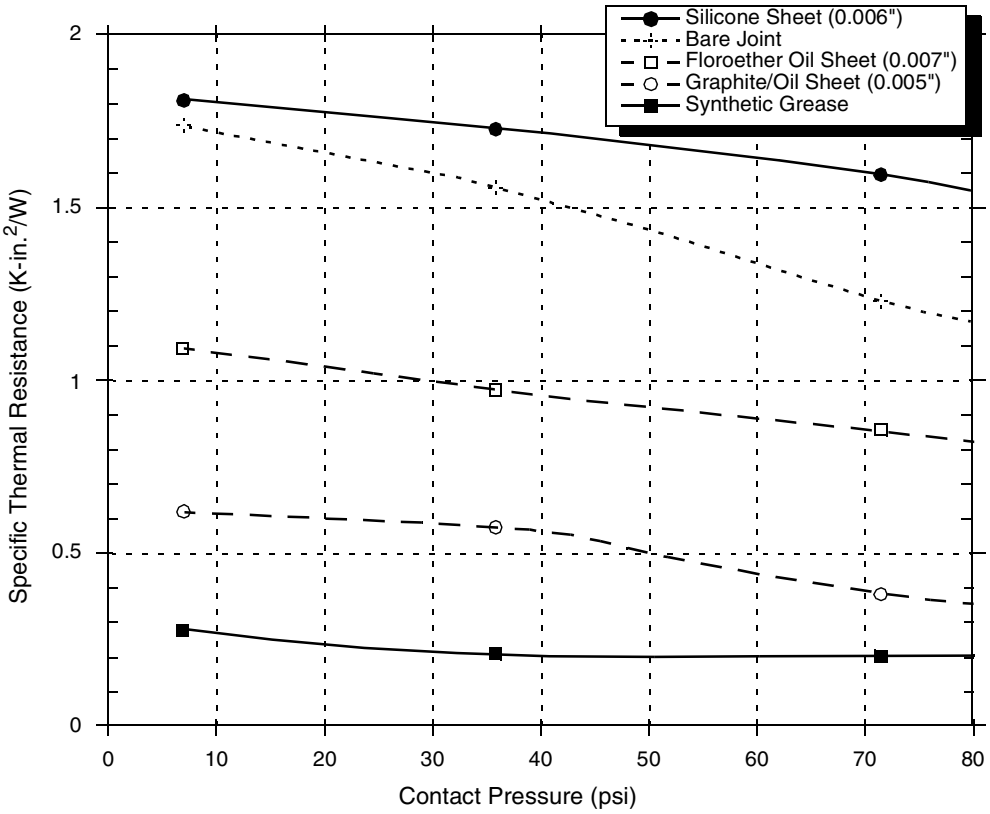


Figure 29. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674

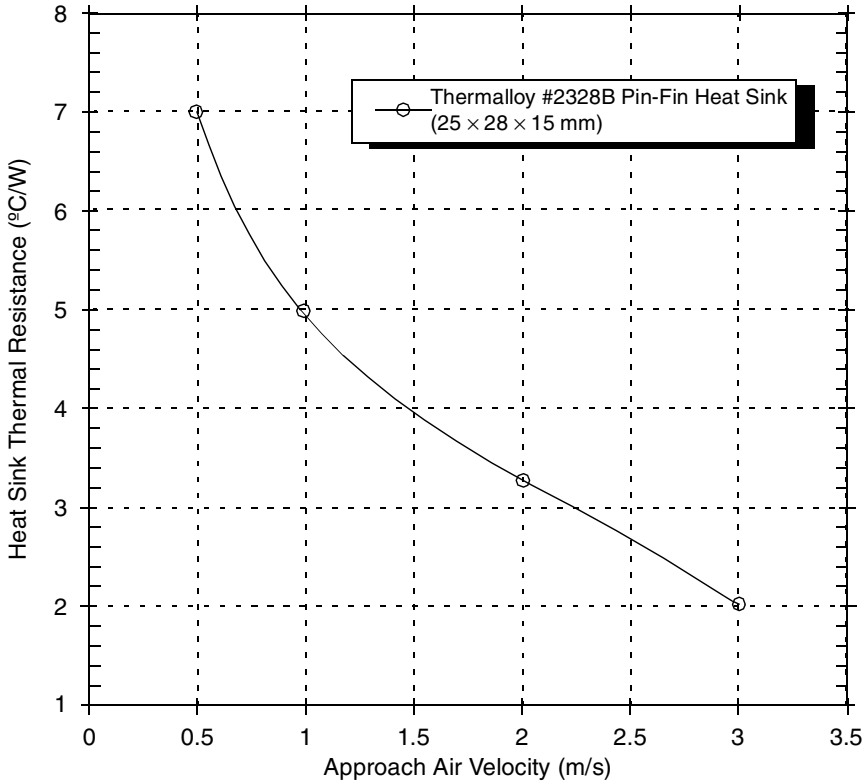


Figure 30. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

9 Document Revision History

Table 16 provides a revision history for this hardware specification.

Table 16. Document Revision History

Revision	Date	Substantive Change(s)
6.1	11/16/2007	Updated Table 17 and Table 19 to show the VU package is available as an MC prefix device compared to an MPC prefix for the other package types; this was done to match the specification documents with the device ordering and part marking information. Updated title of Table 19 to reflect correct name of referenced document and updated respective document order information below table. Updated notes in Table 1–Table 3 replacing references to MPC7410RX*nnn*LE with M*xx*7410*xxnnn*LE since notes to apply to all the available packages types.
6	8/14/2007	Updated Table 4 thermal information: • Deleted rows on single-layer (1s) boards. • CBGA package $R_{\theta JMA}$ for natural convection for four layer boards changed from 17 to 18 °C/W. • HCTE package $R_{\theta JMA}$ for natural convection for four layer boards changed from 22 to 20 °C/W. • HCTE package $R_{\theta JMA}$ for 200 ft./min airflow for four layer boards changed from 19 to 16 °C/W with airflow rate specification changed from 200 ft./min to 1 m/sec. • HCTE package $R_{\theta JMA}$ for 400 ft./min airflow for four layer boards changed from 18 to 15 °C/W with airflow rate specification changed from 400 ft./min to 2 m/sec. • CBGA package $R_{\theta JB}$ changed from 8 to 9°C/W. • HCTE package $R_{\theta JB}$ changed from 14 to 11°C/W. • Table 4 Notes 2 - 4 have been revised and updated; Note 5 is no longer used. Notes on table rows have been renumbered. Updated Figure 26 removing optional heat sink clip to package. Removed references in document to adhesive attached thermal solutions. Updated thermal solution vendor information in Section 8.8. Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information to document: • Added Section 7.2, “Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres). • Added Figure 18 for HCTE_CBGA Lead Free C5 Spheres package, similar to Figure 17 but with differences in dimensions A, A1, and b in the figure’s dimension table. • Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information in Table 17 and Table 19. • Changed part marking example in Figure 31 to an HCTE_CBGA device.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
5	4/13/2005	Section numbering revised. In all previous versions, section numbering began with '1.' These extra '1's' were deleted. For example, previously numbered section 1.8.2 changed to 8.2.
		Section 7.1—added CTE value for HCTE package. Corrected minimum module height from 2.65 mm to 2.72 mm per Figure 17.
		Section 3—added HCTE_LGA (VS package descriptor) package description which is the HCTE_CBGA (HX package descriptor) with the spheres removed.
		Table 4—generalized 'HCTE CBGA' column to 'HCTE' to include both HCTE_CBGA and HCTE_LGA package thermal characteristics.
		Section 5—added HCTE_LGA package. The HCTE_LGA has the same pin assignments as the CBGA and HCTE_CBGA packages. Added side view Part C for HCTE_LGA.
		Section 6—added HCTE_LGA package (VS package descriptor). The HCTE_LGA has the same pinout listing as the CBGA and HCTE packages.
		Section 7.3—added HCTE_LGA package parameters.
		Section 7.4—added HCTE_LGA package mechanical dimensions.
		Table 17—added HCTE_LGA package (VS package descriptor) to part numbering nomenclature.
4	—	Table 5—Changed measurement test condition I_{OH} from -6mA to –5 mA for V_{OH} and I_{OL} from 6 mA to 5 mA for V_{OL} per Product Bulletin.
		Section 1.8.2—revised text regarding AV_{DD} filter selection for the CBGA package.
3	—	Table 6—Changed note 1 to specify that OV_{DD} and $L2OV_{DD}$ power is typically <5% of V_{DD} power.
		Figure 17—revised diagram and dimensions to specify 'cap regions' versus individual cap measurements. Moved individual capacitor placement to separate figure.
		Figure 18—Added this figure to show each individual capacitor placement and value.
		Figure 22—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK.
2	—	Public release, includes Rev 1.1 changes.
		Section 1.7.2—added package capacitor values.
		Section 1.8.6—added recommendation that strong pull-up/down resistors be used on the PLL_CFG[0:3] signals.
		Table 8—removed mode input setup and hold times. These inputs adhere to the general input setup and hold specifications.
		Figure 5—revised mode input diagram to show sample points around $\overline{\text{HRESET}}$ negation.
		Section 1.3—added HCTE package description.
		Figure 22—added note 6 to emphasize that COP emulator and target board need to be able to drive $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ independently to the CPU.
		Section 1.8.2—revised section for HCTE package. Added text and figure for AV_{DD} filter for the CBGA package.
		Section 1.8.6—removed $\overline{\text{AACK}}$, $\overline{\text{TEA}}$, and $\overline{\text{TS}}$ from control signals requiring pull-ups. Removed $\overline{\text{TBST}}$ from snooped transfer attribute list. $\overline{\text{TBST}}$ is an output and is not snooped.

10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document, as described in the following tables.

Table 18. Part Numbers Addressed by MPC7410RXnnnPx Series Part Number Specifications

MPC	7410	RX	*nnn*	P	*x*

Product Code	Part Identifier	Package	Processor Frequency[1]	Application Modifier	Revision Level
MPC	7410	RX = CBGA	450 500 550	P: 2.0 V ± 50 mV 0° to 65°C	C: 1.2; PVR = 800C 1102 [1] D: 1.3; PVR = 800C 1103 [2] E: 1.4; PVR = 800C 1104 [3]

Notes: Document order numbers:
1. MPC7410PCPNS.
2. MPC7410PDPNS.
3. MPC7410PEPNS.

Table 19. Part Numbers Addressed by MPC7410 RISC Microprocessor HardwareSpecifications Addendum for the MPC7410xxnnnNE Series

Mxx	7410	xx	*nnn*	N	E

Product Code	Part Identifier	Package	Processor Frequency [1]	Application Modifier	Revision Level
MPC	7410	RX = CBGA	400 450 500	N: 1.5 V ± 50 mV	E: 1.4; PVR = 800C 1104
		HX = HCTE_CBGA VS = HCTE_LGA	400 450		
MC		VU = HCTE_CBGA (Lead Free C5 Solder Spheres)			

Note: Document order number: MPC7410ECS02AD

Table 20. Part Numbers Addressed by MPC7410TRXnnnNE Part Number Specification

MPC	7410	T	RX	*nnn*	N	E

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency[1]	Application Modifier	Revision Level
MPC	7410	T: –40° to 105°C	RX = CBGA	400 450	N: 1.5 V ±50 mV	E: 1.4; PVR = 800C 1104

Note: Document order number: MPC7410TRXNEPNS.