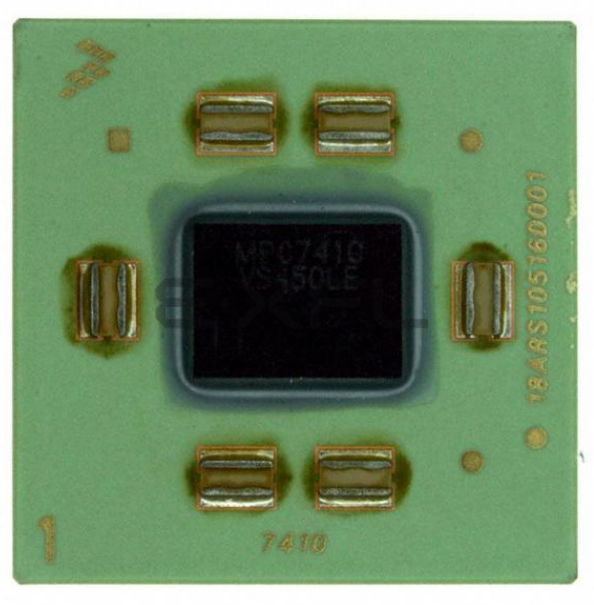

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	450MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410vs450le

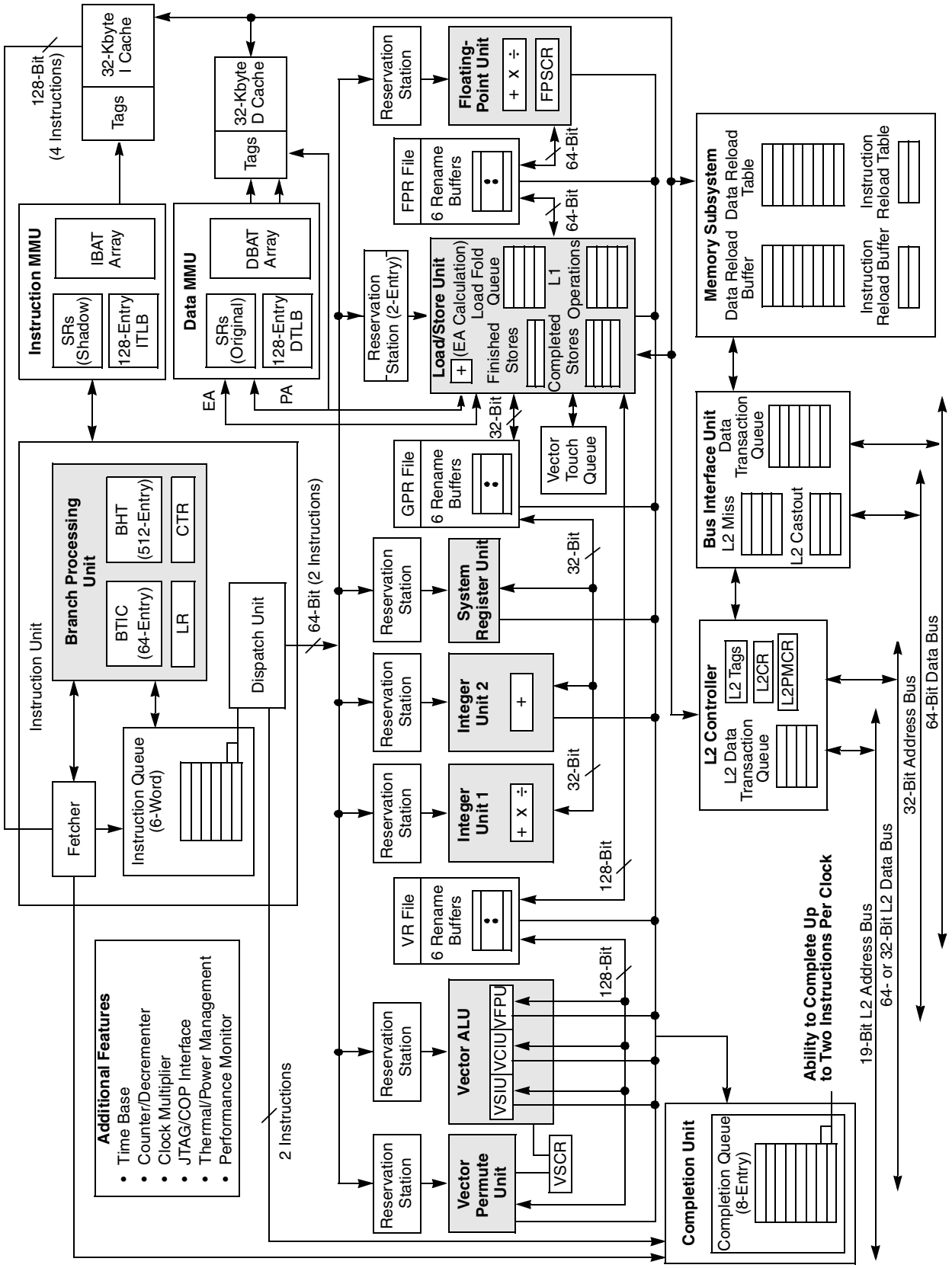


Figure 1. MPC7410 Block Diagram

  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32 Kbyte, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32 Kbyte, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-Kbyte, 1-Mbyte, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-Kbyte), 64-byte (1-Mbyte), or 128-byte (2-Mbyte) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256 Kbytes, 512 Kbytes, 1 Mbyte, or 2 Mbytes of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

  - L2 is fully pipelined to provide 128 bits per L2 clock cycle to the L1s.
  - Up to eight outstanding, out-of-order, cache misses between dL1 and L2/bus
  - Up to seven outstanding, out-of-order transactions on the bus
  - Load folding to fold new dL1 misses into older, outstanding load and store misses to the same line
  - Store miss merging for multiple store misses to the same line. Only coherency action taken (that is, address only) for store misses merged to all 32 bytes of a cache line (no data tenure needed).
  - Two-entry finished store queue and four-entry completed store queue between load/store unit and dL1
  - Separate additional queues for efficient buffering of outbound data (castouts, write throughs, and so on) from dL1 and L2
- Bus interface
  - MPX bus extension to 60x processor interface
  - Mode-compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus
  - Bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 9x supported
  - Selectable interface voltages of 1.8, 2.5, and 3.3 V
- Power management
  - Low-power design with thermal requirements very similar to MPC740 and MPC750
  - Low-voltage processor core
  - Selectable interface voltages can reduce power in output buffers
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE Std 1149.1™ JTAG interface
  - Array built-in self test (ABIST)—factory test only
  - Redundancy on L1 data arrays and L2 tag arrays
- Reliability and serviceability
  - Parity checking on 60x and L2 cache buses

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Maximum Value	Unit	Notes
Rework temperature	T_{rwk}	260	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.8 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

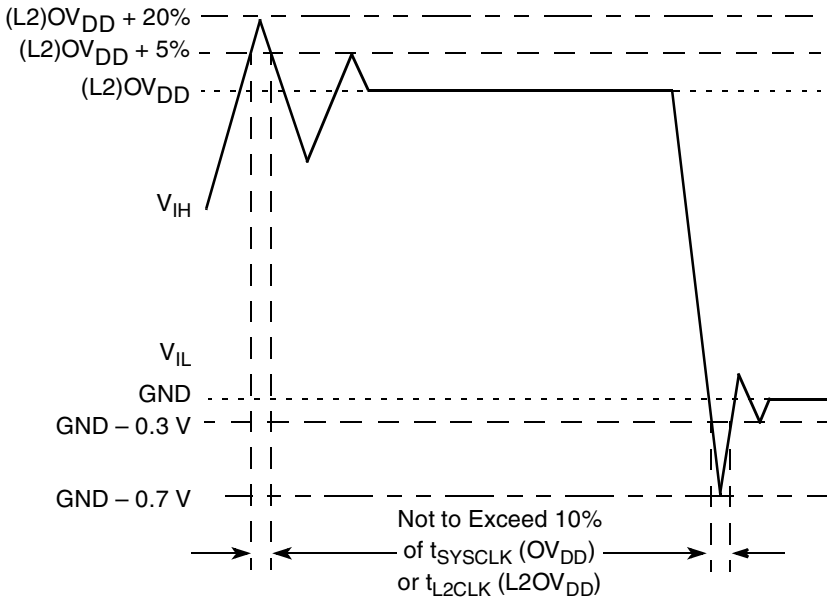


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.8 V ± 100 mV	V	—
PLL supply voltage		AV_{DD}	1.8 V ± 100 mV	V	—
L2 DLL supply voltage		$L2AV_{DD}$	1.8 V ± 100 mV	V	—
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 100 mV	V	—
	BVSEL = $\overline{\text{HRESET}}$	OV_{DD}	2.5 V ± 100 mV	V	—
	BVSEL = ¬$\overline{\text{HRESET}}$ or BVSEL = 1	OV_{DD}	3.3 V ± 165 mV	V	2, 3
L2 bus supply voltage	L2VSEL = 0	$L2OV_{DD}$	1.8 V ± 100 mV	V	—
	L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1	$L2OV_{DD}$	2.5 V ± 100 mV	V	—
Input voltage	Processor bus and JTAG signals	V_{in}	GND to OV_{DD}	V	—
	L2 bus	V_{in}	GND to $L2OV_{DD}$	V	—
Die-junction temperature		T_j	0 to 105	°C	—

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a recommended OV_{DD} value of 2.5 V ± 100 mV for BVSEL = 1.
3. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support BVSEL = ¬$\overline{\text{HRESET}}$.

Table 4 provides the package thermal characteristics for the MPC7410.

Table 4. Package Thermal Characteristics

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	18	20	°C/W	1, 2
Junction-to-ambient thermal resistance, 1m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	16	°C/W	1, 2
Junction-to-ambient thermal resistance, 2m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	13	15	°C/W	1, 2
Junction-to-board thermal resistance	$R_{\theta JB}$	9	11	°C/W	3

Table 6 provides the power consumption for the MPC7410.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency			Unit	Notes
	400 MHz	450 MHz	500 MHz		
Full-On Mode					
Typical	4.2	4.7	5.3	W	1, 3
Maximum	9.5	10.7	11.9	W	1, 2
Doze Mode					
Maximum	4.3	4.8	5.3	W	1
Nap Mode					
Maximum	1.35	1.5	1.65	W	1
Sleep Mode					
Maximum	1.3	1.45	1.6	W	1
Sleep Mode—PLL and DLL Disabled					
Typical	600	600	600	mW	1
Maximum	1.1	1.1	1.1	W	1

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at 105°C and V_{DD} = 1.8 V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65°C and V_{DD} = 1.8 V in a system while running typical benchmarks.

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7410. After fabrication, functional parts are sorted by maximum processor core frequency, see Section 4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, “Ordering Information.”

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 8. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
Input setup	t_{IVKH}	1.0	—	ns	4
Input hold	t_{IXKH}	0	—	ns	4
Output valid times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSV} t_{KHARV} t_{KHOV}	 — — —	 3.0 2.3 3.0	ns	5, 6
Output hold times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	5
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	9
SYSCLK to output high impedance (all except $\overline{ABB}$/$\overline{AMON}$(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/$\overline{DMON}$(0), $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{ABB}$/$\overline{AMON}$(0), $\overline{DBB}$/$\overline{DMON}$(0) high impedance after precharge	t_{KHABPZ}	—	1	t_{SYSCLK}	3, 7, 9
Maximum delay to $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 8, 9

Figure 5 provides the mode select input timing diagram for the MPC7410. The mode select inputs are sampled twice, once before and once after $\overline{\text{HRESET}}$ negation.

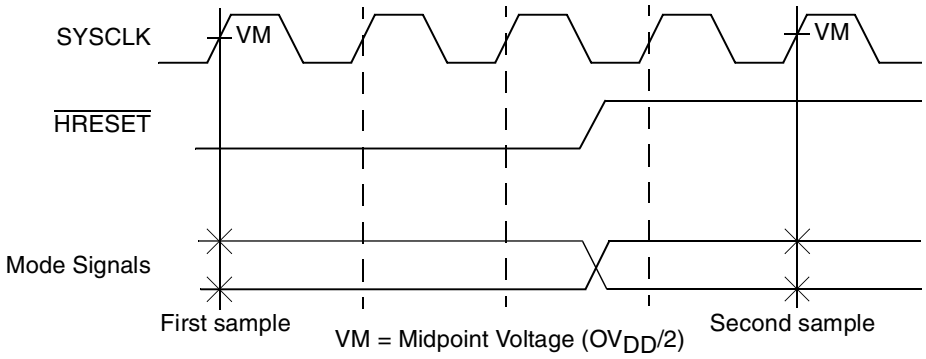


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7410.

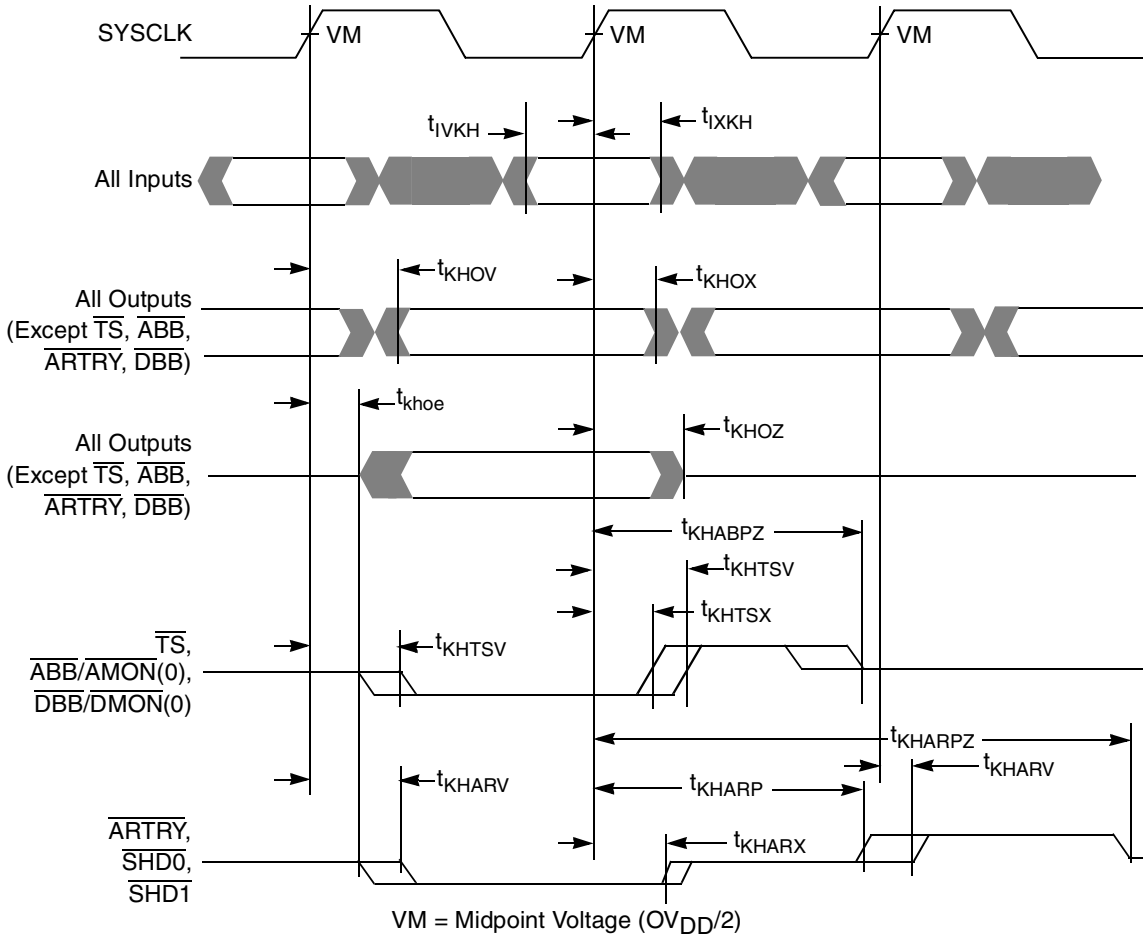


Figure 6. Input/Output Timing Diagram

4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 14 for example core and L2 frequencies at various divisors. Table 9 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC7410 to synchronize L2CLK_OUT at the SRAM with the processor's internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Freescale Application Note AN1794, *Backside L2 Timing Analysis for the PCB Design Engineer.*

The minimum L2CLK frequency in Table 9 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor that results in an L2 frequency below this minimum, or the L2CLK_OUT signals provided for SRAM clocking will not be phase-aligned with the MPC7410 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 9 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC7410 will be a function of the AC timings of the MPC7410, the AC timings for the SRAM, bus loading, and printed-circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies in Table 9. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of two or greater.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings in Table 10 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase-alignment with the internal L2CLK, the signals in Table 10 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	133	400	133	400	133	400	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	7.5	2.5	7.5	2.5	7.5	ns	—
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		50		%	2
Internal DLL-relock time	—	640	—	640	—	640	—	L2CLK	3
DLL capture window	—	0	10	0	10	0	10	ns	5
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	—	50	—	50	ps	6

4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 bus interface AC timing specifications for the MPC7410 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 10. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400, 450, 500 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} and t_{L2CF}	—	1.0	ns	1
Setup times: Data and parity	t_{DVL2CH}	1.5	—	ns	2
Input hold times: Data and parity	t_{DXL2CH}	—	0.0	ns	2
Valid times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOV}	 — — — —	 2.5 2.5 2.9 3.5	ns	3, 4
Output hold times All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOX}	 0.4 0.8 1.2 1.6	 — — — —	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOZ}	 — — — —	 2.0 2.5 3.0 3.5	ns	—

Notes:

1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 00 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 10 is recommended.

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7410, 360 CBGA and 360 HCTE packages.

7.1 Package Parameters for the MPC7410, 360 CBGA and 360 HCTE_CBGA

The package parameters are as provided in the following list. The package types are the 25 × 25 mm, 360-lead ceramic ball grid array package (CBGA) or the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package (HCTE_CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	6.8 ppm/°C (CBGA) 12.3ppm/°C (HCTE_CBGA)

7.2 Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres)

The package parameters are as listed here. The package types are the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package with lead-free C5 spheres (HCTE_CBGA lead-free spheres).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.76 mm (30 mil)
Coefficient of thermal expansion	12.3ppm/°C

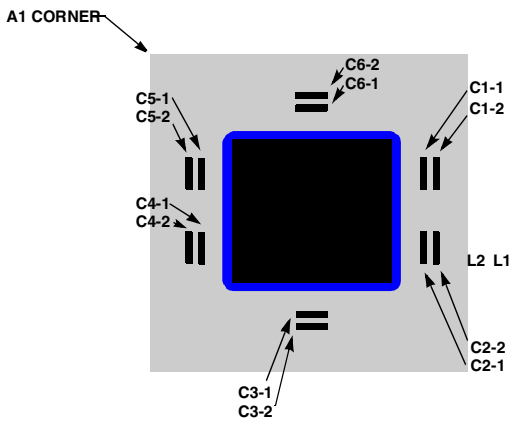
7.5 Package Parameters for the MPC7410, 360 HCTE_LGA

The package parameters are as listed here. The package type is the 25 × 25 mm, 360 high coefficient of thermal expansion LGA package (HCTE_LGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 land array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3ppm/°C

7.6 Substrate Capacitors for the MPC7410

Figure 20 shows the connectivity of the substrate capacitor pads for the MPC7410, 360 CBGA and 360 HCTE packages.



Package Caps	Value µF	Voltage Reference
C1-1	0.01	$L2OV_{DD}$
C1-2		GND
C2-1	0.01	$L2OV_{DD}$
C2-2		GND
C3-1	0.01	V_{DD}
C3-2		GND
C4-1	0.01	OV_{DD}
C4-2		GND
C5-1	0.01	OV_{DD}
C5-2		GND
C6-1	0.01	V_{DD}
C6-2		GND

Figure 20. Substrate Bypass Capacitors for the MPC7410

8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC7410.

8.1 PLL Configuration

The MPC7410 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7410 is shown in Table 13 for example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the minimum and maximum core frequencies listed in Table 8.

Table 13. MPC7410 Microprocessor PLL Configuration

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0100	2x	2x	—	—	—	—	—	—	—
0110	2.5x	2x	—	—	—	—	—	—	—
1000	3x	2x	—	—	—	—	—	—	400 (800)
1110	3.5x	2x	—	—	—	—	—	350 (700)	465 (930)
1010	4x	2x	—	—	—	—	—	400 (800)	—

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used; the remainder of the L2 interface may be left unterminated.

8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 23).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the driver impedance measurement circuit described above.

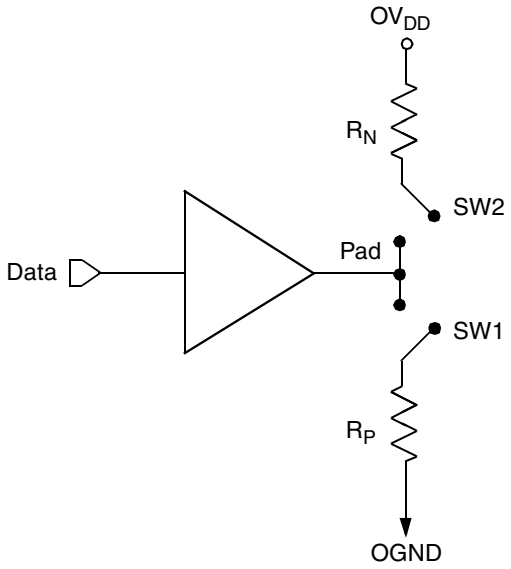


Figure 23. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 24. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 25; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 25 is usually connected to the PCI bridge chip in a system and is an input to the MPC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

8.8 Thermal Management Information

This section provides thermal management information for the MPC7410 for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods such as spring clip to holes in the printed circuit board or with screws and springs to the printed circuit board; see Figure 26 for the BGA package and Figure 27 for the LGA package. This spring force should not exceed 5.5 pounds of force. Note that care should be taken to avoid focused forces being applied to die corners and/or edges when mounting heat sinks.

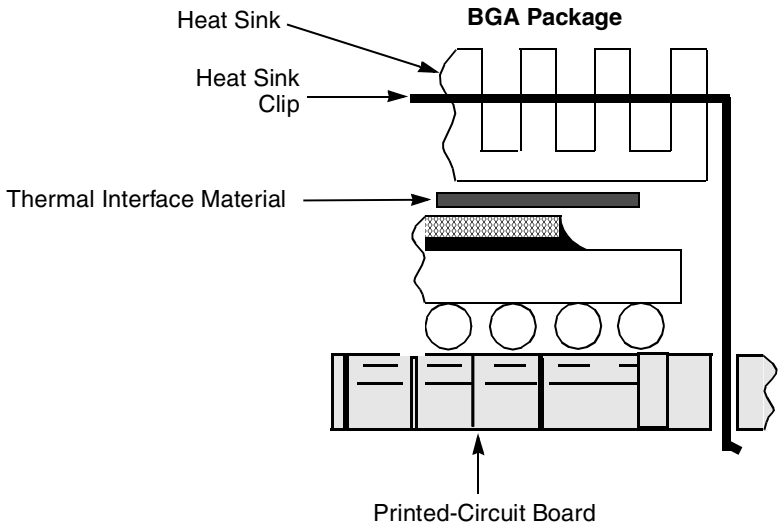


Figure 26. BGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

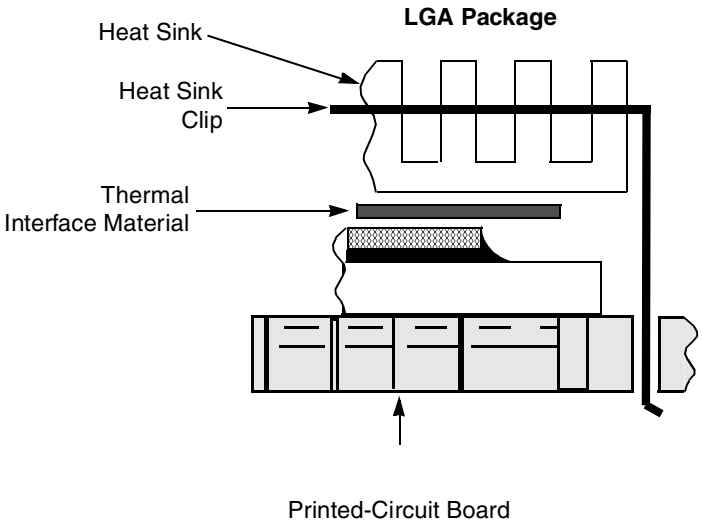


Figure 27. LGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

The board designer can choose between several types of heat sinks to place on the MPC7410. There are several commercially-available heat sinks for the MPC7410 from the following vendors:

Aavid Thermalloy 70 Commercial Street, Suite 200 Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

8.8.1 Internal Package Conduction Resistance

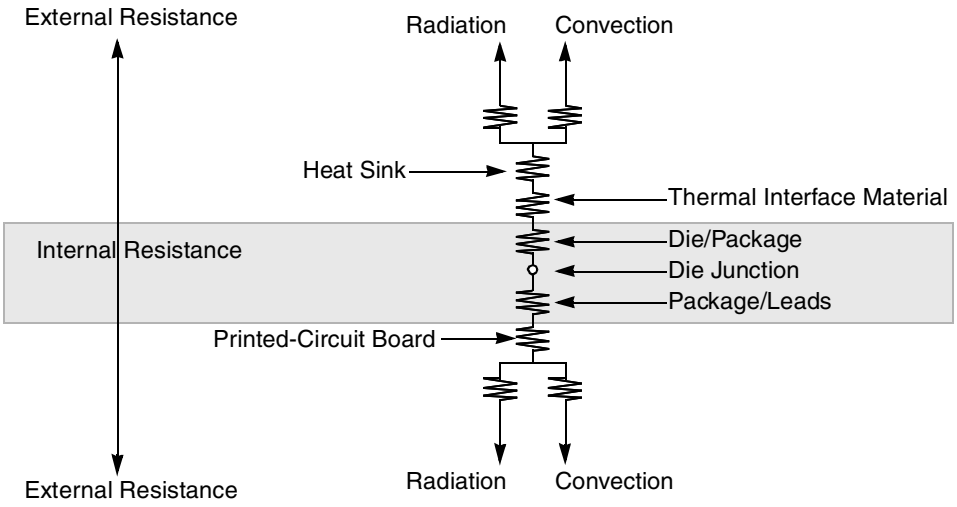
For the exposed-die packaging technology, shown in Table 3, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 28 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.



Note the internal versus external package resistance.

Figure 28. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

8.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 26). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

9 Document Revision History

Table 16 provides a revision history for this hardware specification.

Table 16. Document Revision History

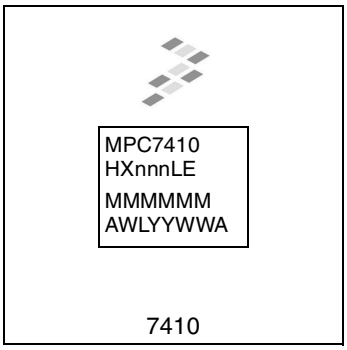
Revision	Date	Substantive Change(s)
6.1	11/16/2007	Updated Table 17 and Table 19 to show the VU package is available as an MC prefix device compared to an MPC prefix for the other package types; this was done to match the specification documents with the device ordering and part marking information. Updated title of Table 19 to reflect correct name of referenced document and updated respective document order information below table. Updated notes in Table 1–Table 3 replacing references to MPC7410RX*nnn*LE with M*xx*7410*xxnnn*LE since notes to apply to all the available packages types.
6	8/14/2007	Updated Table 4 thermal information: • Deleted rows on single-layer (1s) boards. • CBGA package $R_{\theta JMA}$ for natural convection for four layer boards changed from 17 to 18 °C/W. • HCTE package $R_{\theta JMA}$ for natural convection for four layer boards changed from 22 to 20 °C/W. • HCTE package $R_{\theta JMA}$ for 200 ft./min airflow for four layer boards changed from 19 to 16 °C/W with airflow rate specification changed from 200 ft./min to 1 m/sec. • HCTE package $R_{\theta JMA}$ for 400 ft./min airflow for four layer boards changed from 18 to 15 °C/W with airflow rate specification changed from 400 ft./min to 2 m/sec. • CBGA package $R_{\theta JB}$ changed from 8 to 9°C/W. • HCTE package $R_{\theta JB}$ changed from 14 to 11°C/W. • Table 4 Notes 2 - 4 have been revised and updated; Note 5 is no longer used. Notes on table rows have been renumbered. Updated Figure 26 removing optional heat sink clip to package. Removed references in document to adhesive attached thermal solutions. Updated thermal solution vendor information in Section 8.8. Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information to document: • Added Section 7.2, “Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres). • Added Figure 18 for HCTE_CBGA Lead Free C5 Spheres package, similar to Figure 17 but with differences in dimensions A, A1, and b in the figure’s dimension table. • Added HCTE_CBGA Lead Free C5 Spheres (VU) packaging information in Table 17 and Table 19. • Changed part marking example in Figure 31 to an HCTE_CBGA device.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
0.3	—	Added 3.3 V support on the processor bus (BVSEL).
		Table 7—update typical and maximum power numbers for full-on mode in. Removed note 4. Reworded notes 2 and 3.
		Table 9, Note 2—removed reference to application note.
		Figure 17—corrected side view datum A to be datum C.
		Section 1.8.7—added $\overline{CI}$ and $\overline{WT}$ to transfer attribute signals requiring pull-ups.
		Section 1.8.7—added 1-kΩ pull-up recommendation to $\overline{GBL}$ when $\overline{GBL}$ is not connected.
		Table 2— added pull-down resistance necessary for internally pulled-up voltage select pins. Added 3.3-V support for BVSEL.
		Table 13—added note 14 for BVSEL, L2VSEL, and $\overline{TRST}$ pins to address pull-down resistance necessary for these internally pulled-up pins to recognize a low signal.
		Table 6—lowered 2.5 V CV_{IH} from 2.2 to 2.0 V to be compatible with V_{OH} of the MPC107. Added support for 3.3-V processor bus.
		Table 15—modified note 1, use L2CR[L2SL] for L2CLK frequency less than 150 MHz.
		Table 8—revised note 2 discussing for 3.3-V bus voltage support.
		Table 14—added note 5, do not use PL off during power-up sequence.
		Table 1—update output hold times (t_{L2CHOX}).
0.2	—	Corrected Section 1.3—technology from 0.13 µm to 0.18 µm.
		Updated Table 7—adds power consumption numbers; adds note on estimated decrease w/o AltiVec.
		Updated Table 8—adds minimum values for processor frequency and VCO frequency.
		Updated Table 9—input setup, output valid times, output hold times, SYSCLK to output high impedance.
		Updated Table 11—L2SYNC_IN to high impedance.
		Updated Figure 17—mechanical dimensions, adds capacitor pad dimensions.
0.1	—	Minor updates.
0	—	Initial release.

10.3 Part Marking

Parts are marked as the example shown in Figure 31.



HCTE_CBGA

Notes:

MMMMMM is the 6-digit mask number.
AWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 31. Part Marking for HCTE_CBGA Device