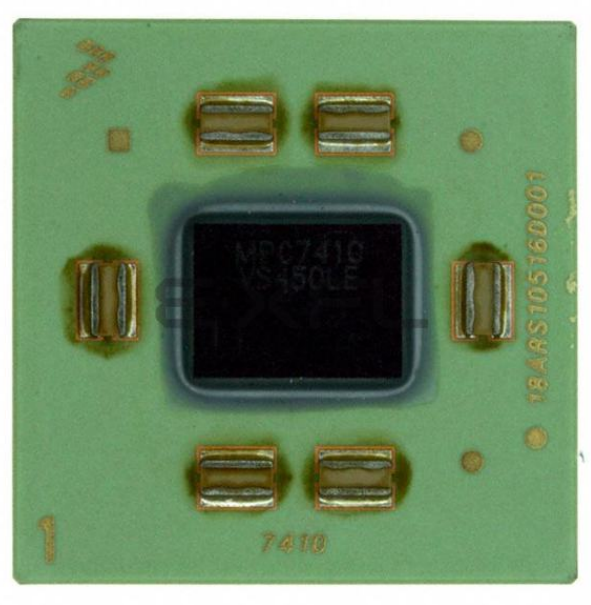


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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC G4 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 450MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 360-CLGA, FCCLGA |
| Supplier Device Package | 360-FCCLGA (25x25) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc7410vs450ne |

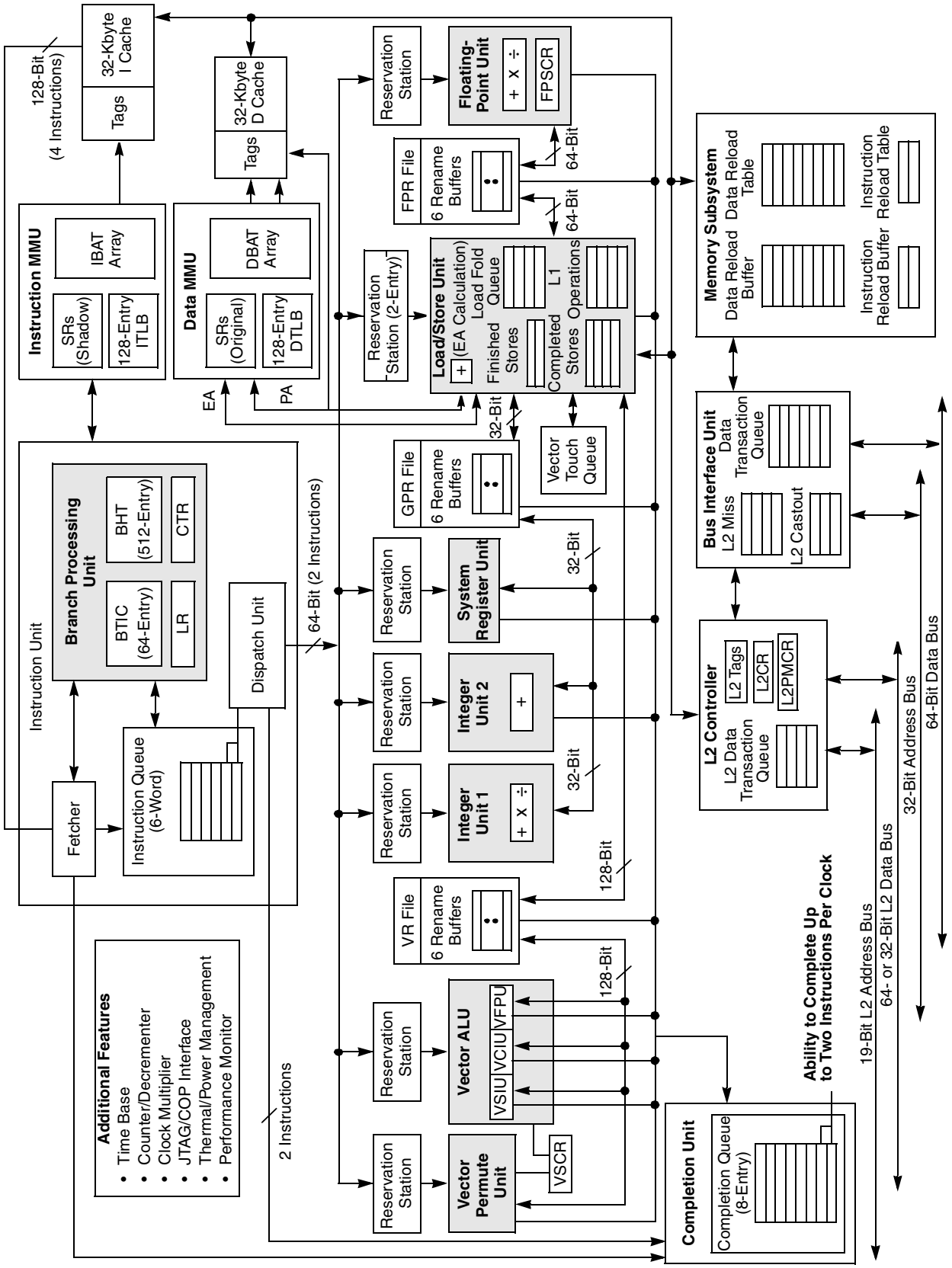



**Figure 1. MPC7410 Block Diagram**

# 3 General Parameters

The following list provides a summary of the general parameters of the MPC7410:

| | |
|---|---|
| Technology | 0.18 µm CMOS, six-layer metal |
| Die size | 6.32 mm × 8.26 mm (52 $mm^2$) |
| Transistor count | 10.5 million |
| Logic design | Fully static |
| Packages | Surface mount 360 ceramic ball grid array (CBGA)<br>Surface mount 360 high coefficient of thermal expansion ceramic ball grid array (HCTE_CBGA)<br>Surface mount 360 high coefficient of thermal expansion ceramic ball grid array with lead free C5 spheres (HCTE_CBGA Lead Free C5 Spheres)<br>Surface mount 360 high coefficient of thermal expansion ceramic land grid array (HCTE_LGA) |
| Core power supply | 1.8 V ± 100 mV DC (nominal; see Table 3 for recommended operating conditions) |
| I/O power supply | 1.8 V ± 100 mV DC or<br>2.5 V ± 100 mV<br>3.3 V ± 165 mV (system bus only)<br>(input thresholds are configuration pin selectable) |

# 4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7410.

## 4.1 DC Electrical Characteristics

The tables in this section describe the MPC7410 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings** [1]

| Characteristic | | Symbol | Maximum Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 2.1 | V | 4 |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 2.1 | V | 4 |
| L2 DLL supply voltage | | $L2AV_{DD}$ | –0.3 to 2.1 | V | 4 |
| Processor bus supply voltage | | $OV_{DD}$ | –0.3 to 3.6 | V | 3, 6 |
| L2 bus supply voltage | | $L2OV_{DD}$ | –0.3 to 2.8 | V | 3 |
| Input voltage | Processor bus | $V_{in}$ | –0.3 to $OV_{DD}$ + 0.2 V | V | 2, 5 |
| | L2 bus | $V_{in}$ | –0.3 to $L2OV_{DD}$ + 0.2 V | V | 2, 5 |
| | JTAG signals | $V_{in}$ | –0.3 to $OV_{DD}$ + 0.2 V | V | — |
| Storage temperature range | | $T_{stg}$ | –55 to 150 | °C | — |

**Table 3. Recommended Operating Conditions [1]**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | 1.8 V ± 100 mV | V | — |
| PLL supply voltage | | $AV_{DD}$ | 1.8 V ± 100 mV | V | — |
| L2 DLL supply voltage | | $L2AV_{DD}$ | 1.8 V ± 100 mV | V | — |
| Processor bus supply voltage | BVSEL = 0 | $OV_{DD}$ | 1.8 V ± 100 mV | V | — |
| | BVSEL = $\overline{\text{HRESET}}$ | $OV_{DD}$ | 2.5 V ± 100 mV | V | — |
| | BVSEL = ¬$\overline{\text{HRESET}}$ or BVSEL = 1 | $OV_{DD}$ | 3.3 V ± 165 mV | V | 2, 3 |
| L2 bus supply voltage | L2VSEL = 0 | $L2OV_{DD}$ | 1.8 V ± 100 mV | V | — |
| | L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1 | $L2OV_{DD}$ | 2.5 V ± 100 mV | V | — |
| Input voltage | Processor bus and JTAG signals | $V_{in}$ | GND to $OV_{DD}$ | V | — |
| | L2 bus | $V_{in}$ | GND to $L2OV_{DD}$ | V | — |
| Die-junction temperature | | $T_j$ | 0 to 105 | °C | — |

**Notes:**
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V $OV_{DD}$ and have a recommended $OV_{DD}$ value of 2.5 V ± 100 mV for BVSEL = 1.
3. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support BVSEL = ¬$\overline{\text{HRESET}}$.

Table 4 provides the package thermal characteristics for the MPC7410.

**Table 4. Package Thermal Characteristics**

| Characteristic | Symbol | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | MPC7410 CBGA | MPC7410 HCTE | | |
| Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board | $R_{\theta JMA}$ | 18 | 20 | °C/W | 1, 2 |
| Junction-to-ambient thermal resistance, 1m/sec airflow, four-layer (2s2p) board | $R_{\theta JMA}$ | 14 | 16 | °C/W | 1, 2 |
| Junction-to-ambient thermal resistance, 2m/sec airflow, four-layer (2s2p) board | $R_{\theta JMA}$ | 13 | 15 | °C/W | 1, 2 |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 9 | 11 | °C/W | 3 |

Figure 5 provides the mode select input timing diagram for the MPC7410. The mode select inputs are sampled twice, once before and once after $\overline{\text{HRESET}}$ negation.

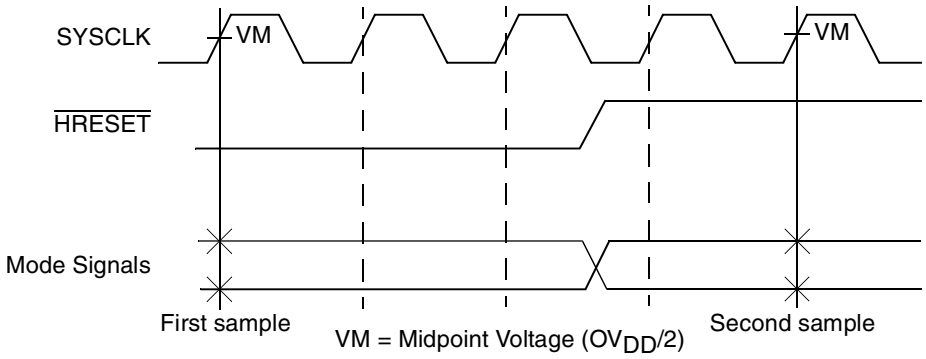



**Figure 5. Mode Input Timing Diagram**

Figure 6 provides the input/output timing diagram for the MPC7410.

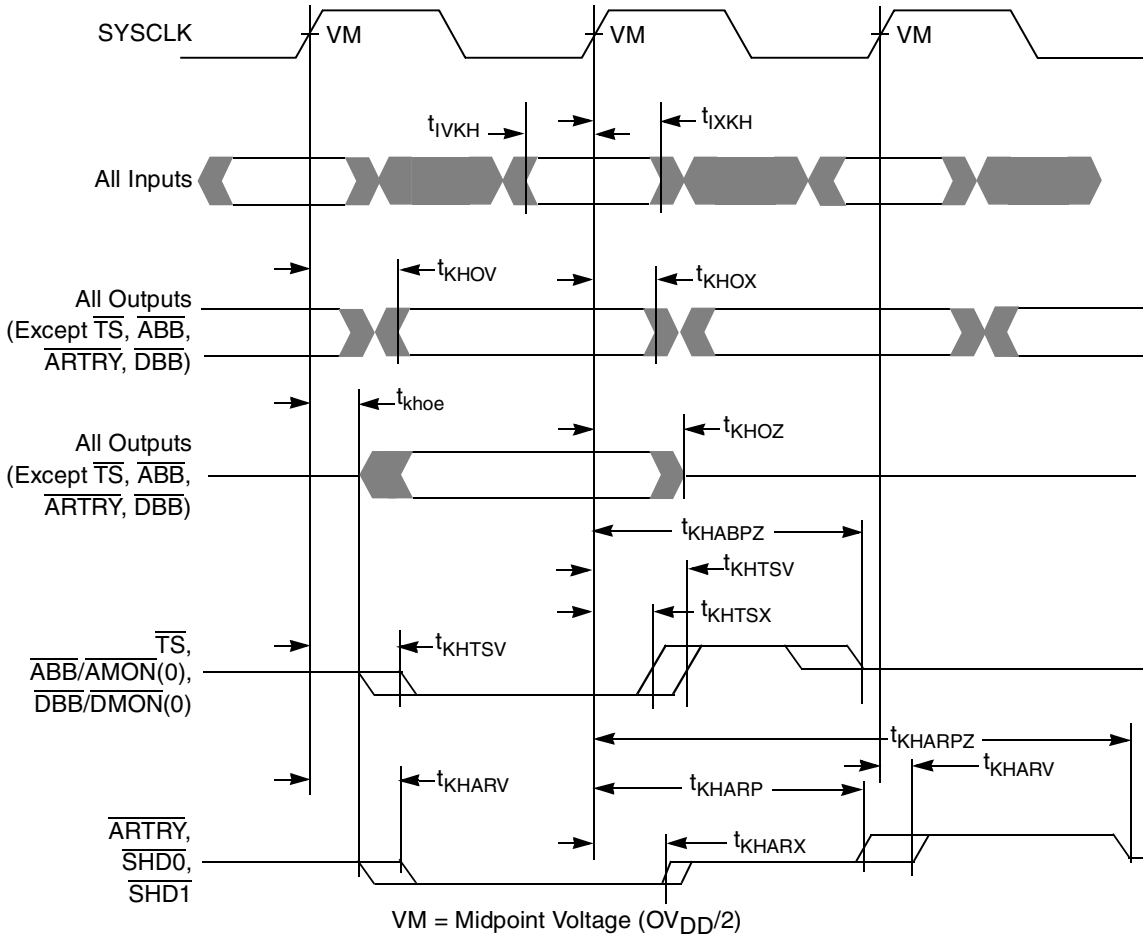



**Figure 6. Input/Output Timing Diagram**

**Table 9. L2CLK Output AC Timing Specifications (continued)**

At recommended operating conditions (see Table 3)

| Parameter | Symbol | 400 MHz | | 450 MHz | | 500 MHz | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| L2CLK_OUT output jitter | — | — | ±150 | — | ±150 | — | ±150 | ps | 6 |

**Notes**:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2CLK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 7.

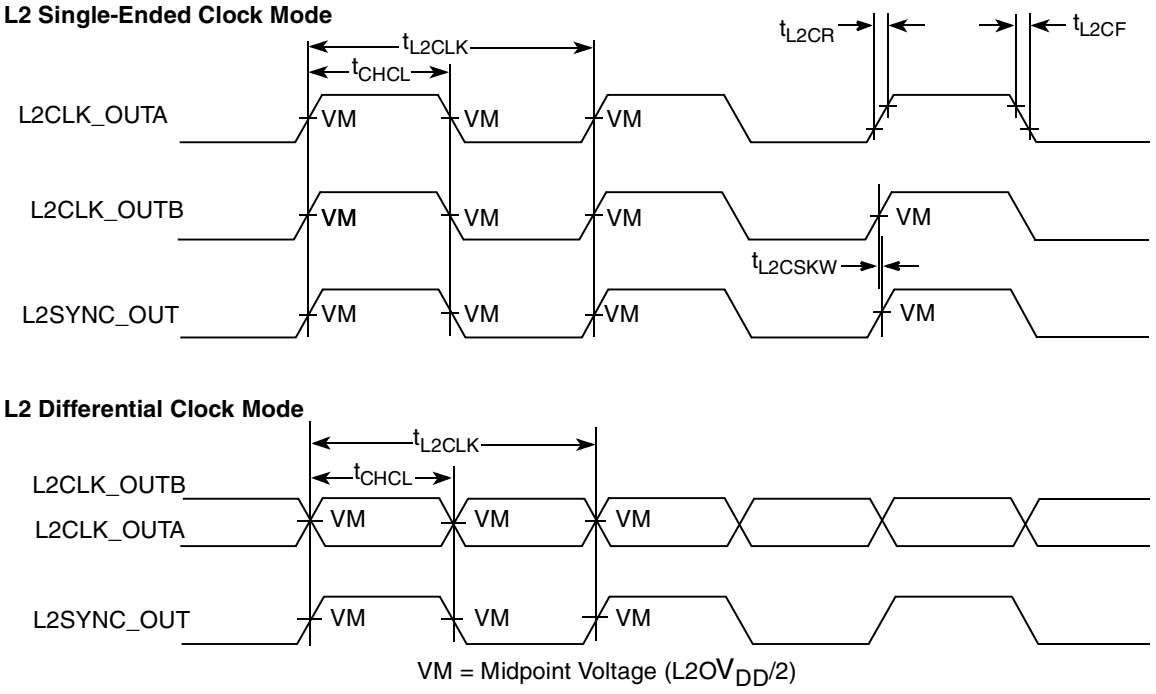



**Figure 7. L2CLK_OUT Output Timing Diagram**

## 4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 bus interface AC timing specifications for the MPC7410 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

**Table 10. L2 Bus Interface AC Timing Specifications**

At recommended operating conditions (see Table 3)

| Parameter | Symbol | 400, 450, 500 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| L2SYNC_IN rise and fall time | $t_{L2CR}$ and $t_{L2CF}$ | — | 1.0 | ns | 1 |
| Setup times: Data and parity | $t_{DVL2CH}$ | 1.5 | — | ns | 2 |
| Input hold times: Data and parity | $t_{DXL2CH}$ | — | 0.0 | ns | 2 |
| Valid times:<br>All outputs when L2CR[14–15] = 00<br>All outputs when L2CR[14–15] = 01<br>All outputs when L2CR[14–15] = 10<br>All outputs when L2CR[14–15] = 11 | $t_{L2CHOV}$ | <br>—<br>—<br>—<br>— | <br>2.5<br>2.5<br>2.9<br>3.5 | ns | 3, 4 |
| Output hold times<br>All outputs when L2CR[14–15] = 00<br>All outputs when L2CR[14–15] = 01<br>All outputs when L2CR[14–15] = 10<br>All outputs when L2CR[14–15] = 11 | $t_{L2CHOX}$ | <br>0.4<br>0.8<br>1.2<br>1.6 | <br>—<br>—<br>—<br>— | ns | 3 |
| L2SYNC_IN to high impedance:<br>All outputs when L2CR[14–15] = 00<br>All outputs when L2CR[14–15] = 01<br>All outputs when L2CR[14–15] = 10<br>All outputs when L2CR[14–15] = 11 | $t_{L2CHOZ}$ | <br>—<br>—<br>—<br>— | <br>2.0<br>2.5<br>3.0<br>3.5 | ns | — |

**Notes**:

1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 00 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 10 is recommended.

Figure 8 shows the L2 bus input timing diagrams for the MPC7410.

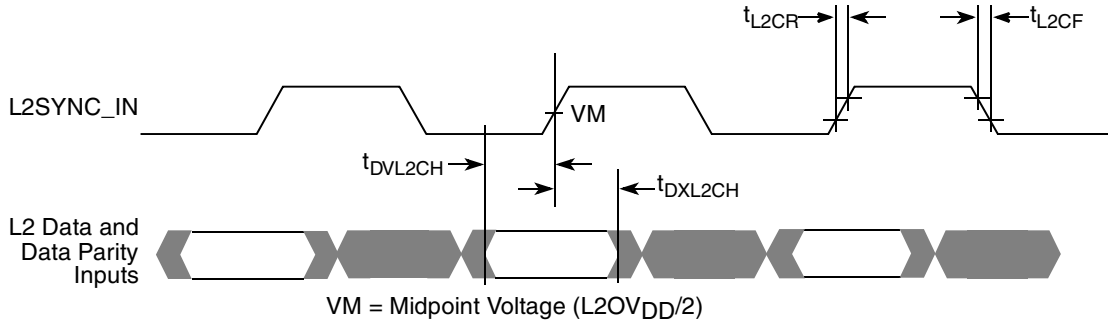



**Figure 8. L2 Bus Input Timing Diagrams**

Figure 9 shows the L2 bus output timing diagrams for the MPC7410.

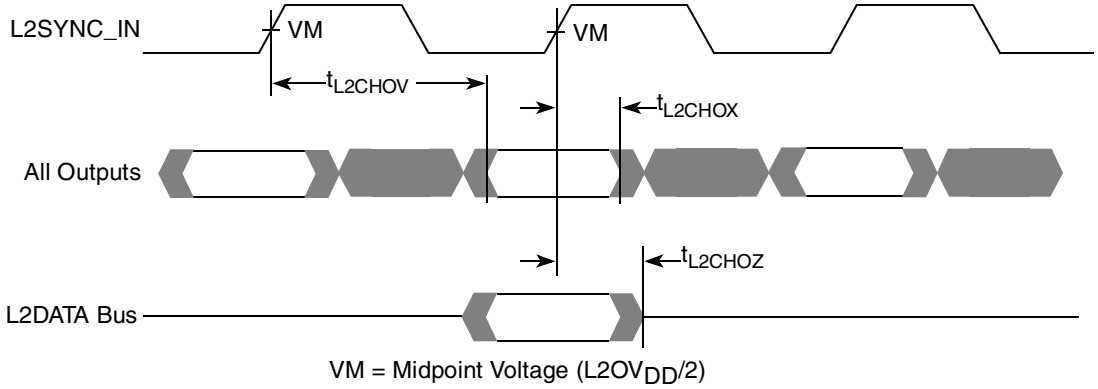



**Figure 9. L2 Bus Output Timing Diagrams**

Figure 10 provides the AC test load for L2 interface of the MPC7410.

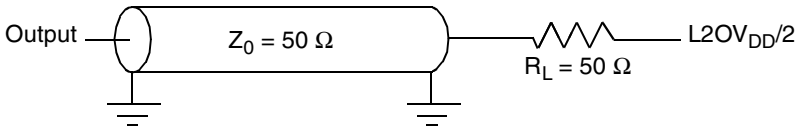



**Figure 10. AC Test Load for the L2 Interface**

## 4.2.5 IEEE 1149.1 AC Timing Specifications

Table 11 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

**Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

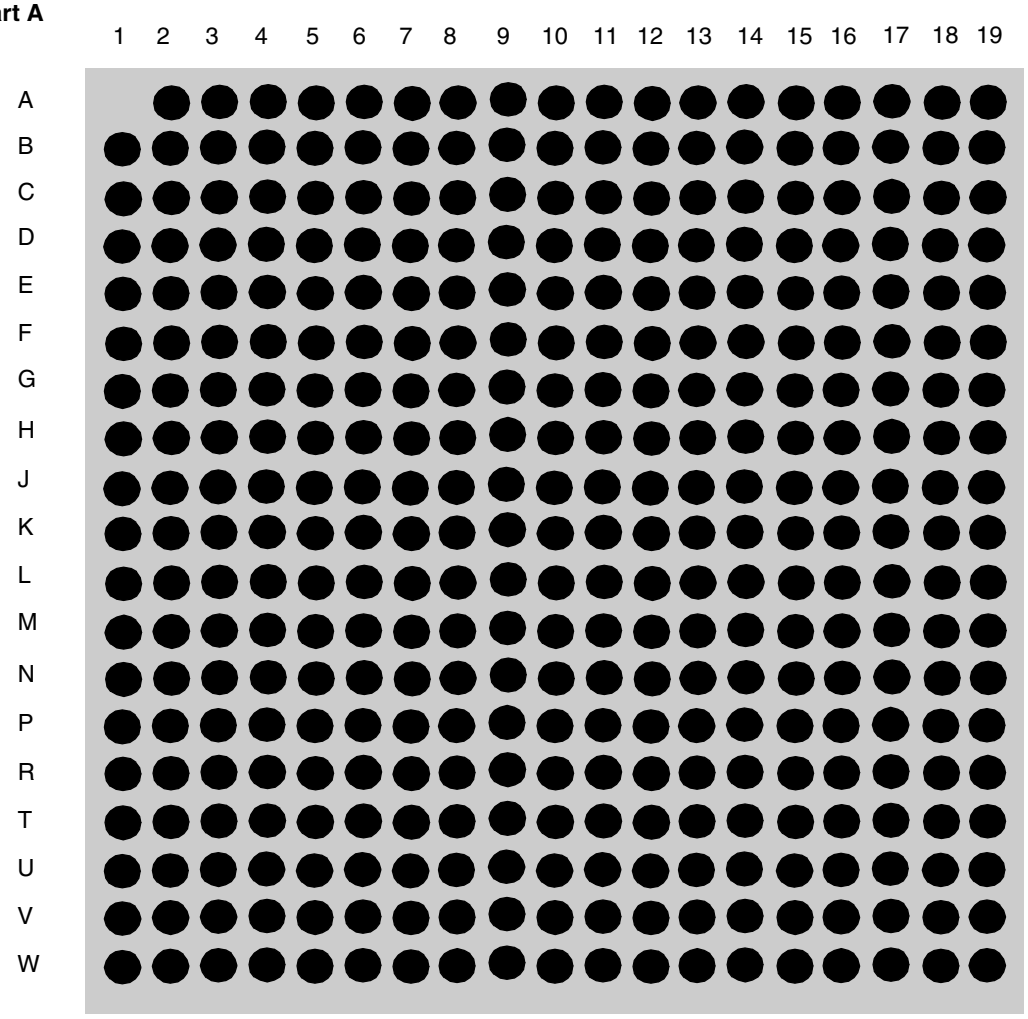
At recommended operating conditions (see Table 3)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| TCK frequency of operation | $f_{TCLK}$ | 0 | 33.3 | MHz | — |
| TCK cycle time | $t_{TCLK}$ | 30 | — | ns | — |
| TCK clock pulse width measured at $OV_{DD}/2$ | $t_{JHJL}$ | 15 | — | ns | — |
| TCK rise and fall times | $t_{JR}$ and $t_{JF}$ | 0 | 2 | ns | — |

# 5 Pin Assignments

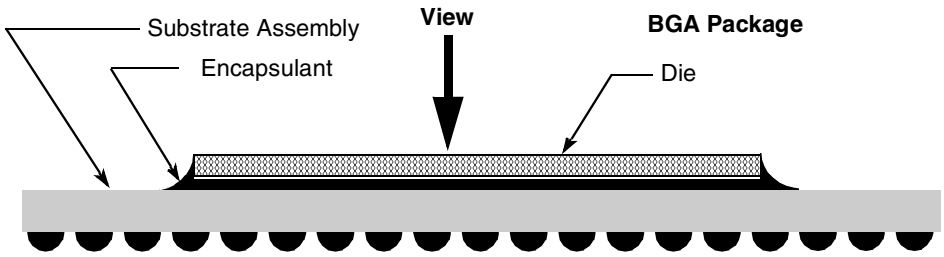
Figure 16, part A shows the pinout for the MPC7410, 360 CBGA, 360 HCTE, and 360 HCTE Lead Free C5 Spheres packages as viewed from the top surface. Figure 16, part B shows the side profile of the CBGA and HCTE_CBGA packages to indicate the direction of the top surface view. Figure 16, part C shows the side profile of the HCTE_LGA package to indicate the direction of the top surface view.

**Part A**




Not to Scale

**Part B**



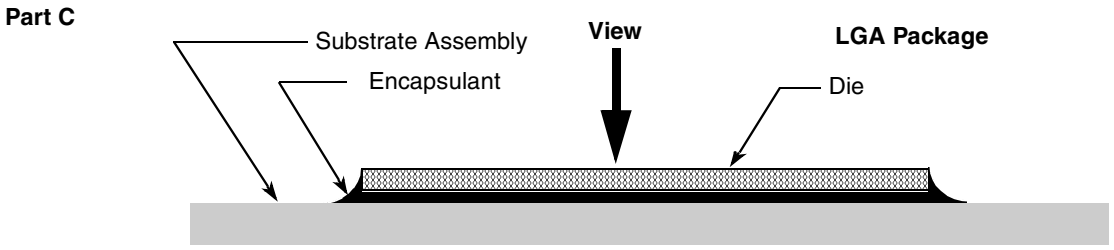



**Figure 16. Pinout of the MPC7410, 360 CBGA and 360 HCTE Packages as Viewed from the Top Surface**

# 6 Pinout Listings

Table 12 provides the pinout listing for the MPC7410 360 CBGA, 360 HCTE packages.

**Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages**

| Signal Name | Pin Number | Active | I/O | I/F Select [1] | Notes |
|---|---|---|---|---|---|
| A[0:31] | A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2 | High | I/O | BVSEL | |
| $\overline{\text{AACK}}$ | N3 | Low | Input | BVSEL | — |
| $\overline{\text{ABB}}$ | L7 | Low | Output | BVSEL | 12, 16 |
| AP[0:3] | C4, C5, C6, C7 | High | I/O | BVSEL | — |
| $\overline{\text{ARTRY}}$ | L6 | Low | I/O | BVSEL | — |
| $AV_{DD}$ | A8 | — | Input | $V_{DD}$ | — |
| $\overline{\text{BG}}$ | H1 | Low | Input | BVSEL | — |
| $\overline{\text{BR}}$ | E7 | Low | Output | BVSEL | — |
| BVSEL | W1 | High | Input | N/A | 1, 3, 8, 9, 14 |
| $\overline{\text{CHK}}$ | K11 | Low | Input | BVSEL | 2, 8, 9 |
| $\overline{\text{CI}}$ | C2 | Low | I/O | BVSEL | — |
| $\overline{\text{CKSTP\_IN}}$ | B8 | Low | Input | BVSEL | — |
| $\overline{\text{CKSTP\_OUT}}$ | D7 | Low | Output | BVSEL | — |
| CLK_OUT | E3 | High | Output | BVSEL | — |
| $\overline{\text{DBB}}$ | K5 | Low | Output | BVSEL | 12, 16 |
| $\overline{\text{DBG}}$ | K1 | Low | Input | BVSEL | — |
| DH[0:31] | W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5 | High | I/O | BVSEL | — |

**Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Select [1] | Notes |
|---|---|---|---|---|---|
| DL[0:31] | M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2 | High | I/O | BVSEL | — |
| DP[0:7] | L1, P2, M2, V2, M1, N2, T3, R1 | High | I/O | BVSEL | — |
| $\overline{\text{DRDY}}$ | K9 | Low | Output | BVSEL | 6, 8, 13 |
| $\overline{\text{DBWO}}$<br>DTI[0] | D1 | Low | Input | BVSEL | — |
| DTI[1:2] | H6, G1 | High | Input | BVSEL | 5, 10, 13 |
| $\overline{\text{EMODE}}$ | A3 | Low | Input | BVSEL | 7, 10 |
| $\overline{\text{GBL}}$ | B1 | Low | I/O | BVSEL | — |
| GND | D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16 | — | — | N/A | — |
| $\overline{\text{HIT}}$ | B5 | Low | Output | BVSEL | 6, 8 |
| $\overline{\text{HRESET}}$ | B6 | Low | Input | BVSEL | — |
| $\overline{\text{INT}}$ | C11 | Low | Input | BVSEL | — |
| L1_TSTCLK | F8 | High | Input | BVSEL | 2 |
| L2ADDR[0:16] | L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18 | High | Output | L2VSEL | — |
| L2ADDR[17:18] | K19,W19 | High | Output | L2VSEL | 8 |
| $L2AV_{DD}$ | L13 | — | Input | $V_{DD}$ | — |
| $\overline{\text{L2CE}}$ | P17 | Low | Output | L2VSEL | — |
| L2CLK_OUTA | N15 | High | Output | L2VSEL | — |
| L2CLK_OUTB | L16 | High | Output | L2VSEL | — |
| L2DATA[0:63] | U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13 | High | I/O | L2VSEL | — |
| L2DP[0:7] | V14, U16, T19, N18, H14, F17, C19, B15 | High | I/O | L2VSEL | — |
| $L2OV_{DD}$ | D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15 | — | — | N/A | 11 |
| L2SYNC_IN | L14 | High | Input | L2VSEL | — |
| L2SYNC_OUT | M14 | High | Output | L2VSEL | — |
| L2_TSTCLK | F7 | High | Input | BVSEL | 2 |

# 7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7410, 360 CBGA and 360 HCTE packages.

## 7.1 Package Parameters for the MPC7410, 360 CBGA and 360 HCTE_CBGA

The package parameters are as provided in the following list. The package types are the 25 × 25 mm, 360-lead ceramic ball grid array package (CBGA) or the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package (HCTE_CBGA).

| | |
|---|---|
| Package outline | 25 × 25 mm |
| Interconnects | 360 (19 × 19 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.72 mm |
| Maximum module height | 3.20 mm |
| Ball diameter | 0.89 mm (35 mil) |
| Coefficient of thermal expansion | 6.8 ppm/°C (CBGA)<br>12.3ppm/°C (HCTE_CBGA) |

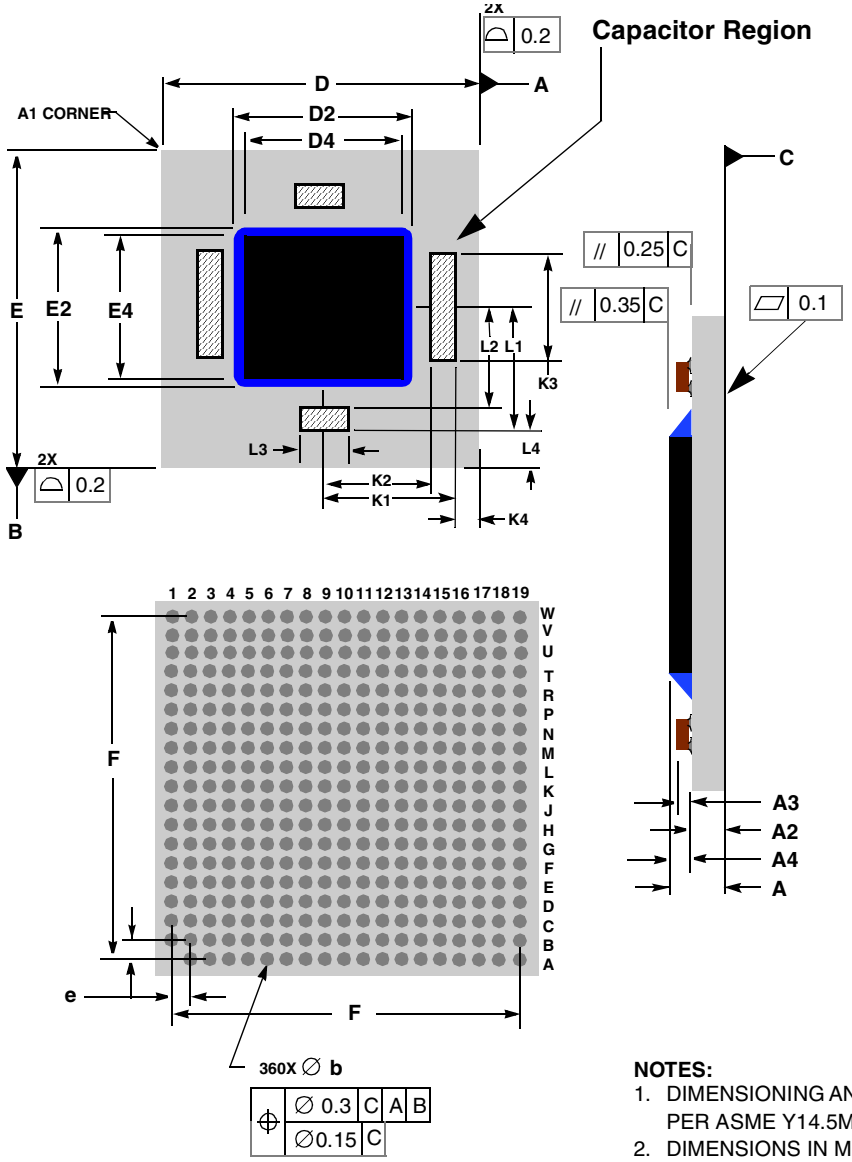
## 7.2 Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres)

The package parameters are as listed here. The package types are the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package with lead-free C5 spheres (HCTE_CBGA lead-free spheres).

| | |
|---|---|
| Package outline | 25 × 25 mm |
| Interconnects | 360 (19 × 19 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.32 mm |
| Maximum module height | 2.80 mm |
| Ball diameter | 0.76 mm (30 mil) |
| Coefficient of thermal expansion | 12.3ppm/°C |

## 7.5.1 Mechanical Dimensions for the MPC7410, 360 HCTE_LGA

Figure 19 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 HCTE_LGA package.




| | Millimeters | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.92 | 2.20 |
| A2 | 1.10 | 1.30 |
| A3 | — | 0.60 |
| A4 | 0.82 | 0.90 |
| b | 0.79 | 0.99 |
| D | 25.00 BSC | |
| D2 | — | 12.50 |
| D4 | 6.00 | 9.00 |
| e | 1.27 BSC | |
| E | 25.00 BSC | |
| E2 | — | 14.30 |
| E4 | 8.00 | 11.00 |
| F | 22.86 BSC | |
| K1 | — | 9.75 |
| K2 | 6.46 | — |
| K3 | 8.20 | 8.60 |
| K4 | 2.75 | — |
| L1 | — | 9.50 |
| L2 | 6.94 | — |
| L3 | 3.10 | 3.30 |
| L4 | 3.00 | — |

**NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A PAD MISSING FROM THE ARRAY.

**Figure 19. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410, 360 HCTE_LGA Package**

**Table 13. MPC7410 Microprocessor PLL Configuration (continued)**

| PLL_CFG [0:3] | Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier | Core-to VCO Multiplier | Bus 33.3 MHz | Bus 50 MHz | Bus 66.6 MHz | Bus 75 MHz | Bus 83.3 MHz | Bus 100 MHz | Bus 133 MHz |
| 0111 | 4.5x | 2x | — | — | — | — | 375 (750) | 450 (900) | — |
| 1011 | 5x | 2x | — | — | — | 375 (750) | 416 (833) | 500 (1000) | — |
| 1001 | 5.5x | 2x | — | — | 366 (733) | 412 (825) | 458 (916) | — | — |
| 1101 | 6x | 2x | — | — | 400 (800) | 450 (900) | 500 (1000) | — | — |
| 0101 | 6.5x | 2x | — | — | 433 (866) | 488 (967) | — | — | — |
| 0010 | 7x | 2x | — | 350 (700) | 466 (933) | — | — | — | — |
| 0001 | 7.5x | 2x | — | 375 (750) | 500 (1000) | — | — | — | — |
| 1100 | 8x | 2x | — | 400 (800) | — | — | — | — | — |
| 0000 | 9x | 2x | — | 450 (900) | — | — | — | — | — |
| 0011 | PLL off/bypass | | PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied | | | | | | |
| 1111 | PLL off | | PLL off, no core clocking occurs | | | | | | |

**Notes:**

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and third-party emulator tool development only.
   **Note**: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7410 regardless of the SYSCLK input.
5. PLL-off mode should not be used during chip power-up sequencing.

The MPC7410 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC7410. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC7410 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the

MPC7410 core, and the phase adjustment range that the L2 DLL supports. Table 14 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 133 MHz. Sample core-to-L2 frequencies for the MPC7410 is shown in Table 14. In this example, shaded cells represent settings that, for a given core frequency, result in L2 frequencies that do not comply with the minimum and maximum L2 frequencies listed in Table 10.

**Table 14. Sample Core-to-L2 Frequencies**

| Core Frequency (MHz) | ÷1 | ÷1.5 | ÷2 | ÷2.5 | ÷3 | ÷3.5 | ÷4 |
|---|---|---|---|---|---|---|---|
| 350 | 350 | 233 | 175 | 140 | — | — | — |
| 366 | 366 | 244 | 183 | 147 | — | — | — |
| 400 | 400 | 266 | 200 | 160 | 133 | — | — |
| 433 | — | 288 | 216 | 173 | 144 | — | — |
| 450 | — | 300 | 225 | 180 | 150 | — | — |
| 466 | — | 311 | 233 | 186 | 155 | 133 | — |
| 500 | — | 333 | 250 | 200 | 166 | 143 | — |

**Note:** The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz.

## 8.2 PLL and DLL Power Supply Filtering

The $AV_{DD}$ and $L2AV_{DD}$ power signals are provided on the MPC7410 to supply power to the PLL and DLL, respectively. Both $AV_{DD}$ and $L2AV_{DD}$ can be supplied power from the $V_{DD}$ power plane. High frequency noise in the 500 kHz to 10 MHz resonant frequency range of the PLL on the $V_{DD}$ power plane could affect the stability of the internal clocks.

On systems that use the MPC7410 HCTE device, the $AV_{DD}$ and $L2AV_{DD}$ input signals should both implement the circuit shown in Figure 21.

On systems that use the MPC7410 CBGA device, the $L2AV_{DD}$ input should implement the circuit shown in Figure 21.

When selecting which filter to use on the $AV_{DD}$ input of the MPC7410 CBGA device specifically, system designers should refer to Erratum No. 18 in the *MPC7410 RISC Microprocessor Chip Errata* (MPC7410CE). The $AV_{DD}$ input of the MPC7410 CBGA device is sensitive to system noise on both the $V_{DD}$ power plane, as described above, and the $OV_{DD}$ power plane as described in the Erratum No. 18. With these $AV_{DD}$ sensitivities to $OV_{DD}$ and $V_{DD}$ noise, care must be taken when selecting the filter circuit for the $AV_{DD}$ input of the MPC7410 CBGA device. Erratum No. 18 does not apply to the $AV_{DD}$ input of the MPC7401 HCTE device, nor does it affect the $L2AV_{DD}$ input of either the HCTE or the CBGA device.

As described in Erratum No. 18, when there is a high amount of noise on the $OV_{DD}$ power plane due to I/O switching rates, it is possible for the $OV_{DD}$ noise to couple into the PLL supply voltage ($AV_{DD}$) internal to the MPC7410 CBGA package. It is the recommendation of Freescale, that new designs using the MPC7410 CBGA package provide the ability to implement either filter shown in Figure 21 and Figure 22 at the $AV_{DD}$ input. Existing designs that implemented Figure 21 on $AV_{DD}$ may never experience the error described in Erratum No. 18. Both new and

existing designs should qualify both $AV_{DD}$ filter solutions, and the filter providing the most robust margin should be implemented.

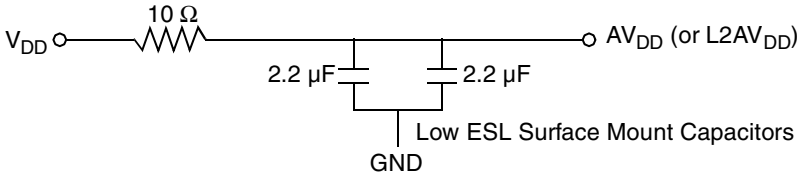



**Figure 21. PLL Power Supply Filter Circuit No.1**

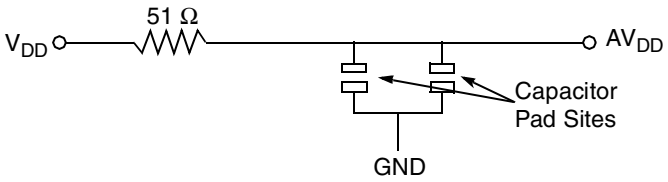



**Figure 22. PLL Power Supply Filter Circuit No. 2**

The filter circuit should be placed as close as possible to the $AV_{DD}$ pin to minimize noise coupled from nearby circuits. A separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

It is the recommendation of Freescale, that systems that implement the $AV_{DD}$ filter shown in Figure 22 design in the pads for the removed capacitors (shown in Figure 21), to provide for the possible reintroduction of the filter in Figure 21. This would be necessary in case there is a planned transition from the CBGA package to the HCTE package of the MPC7410.

## 8.3 Decoupling Recommendations

Due to the MPC7410 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7410 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7410 system, and the MPC7410 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $OV_{DD}$, and $L2OV_{DD}$ pin of the MPC7410. It is also recommended that these decoupling capacitors receive their power from separate $V_{DD}$, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations, where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$, $L2OV_{DD}$, and $OV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

$R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 24 describes the alternate driver impedance measurement circuit.

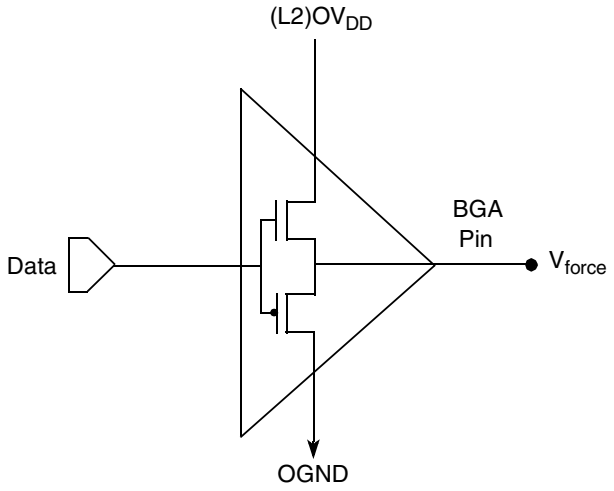



**Figure 24. Alternate Driver Impedance Measurement Circuit**

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

**Table 15. Impedance Characteristics**

$V_{DD}$ = 1.8 V, $OV_{DD}$ = 2.5 V, $T_j$ = 0° – 105°C

| Impedance | Processor Bus | L2 Bus | Symbol | Unit |
|---|---|---|---|---|
| $R_N$ | 41.5–54.3 | 42.7–54.1 | $Z_0$ | Ω |
| $R_P$ | 37.3–55.3 | 39.3–50.0 | $Z_0$ | Ω |

## 8.6 Pull-Up Resistor Requirements

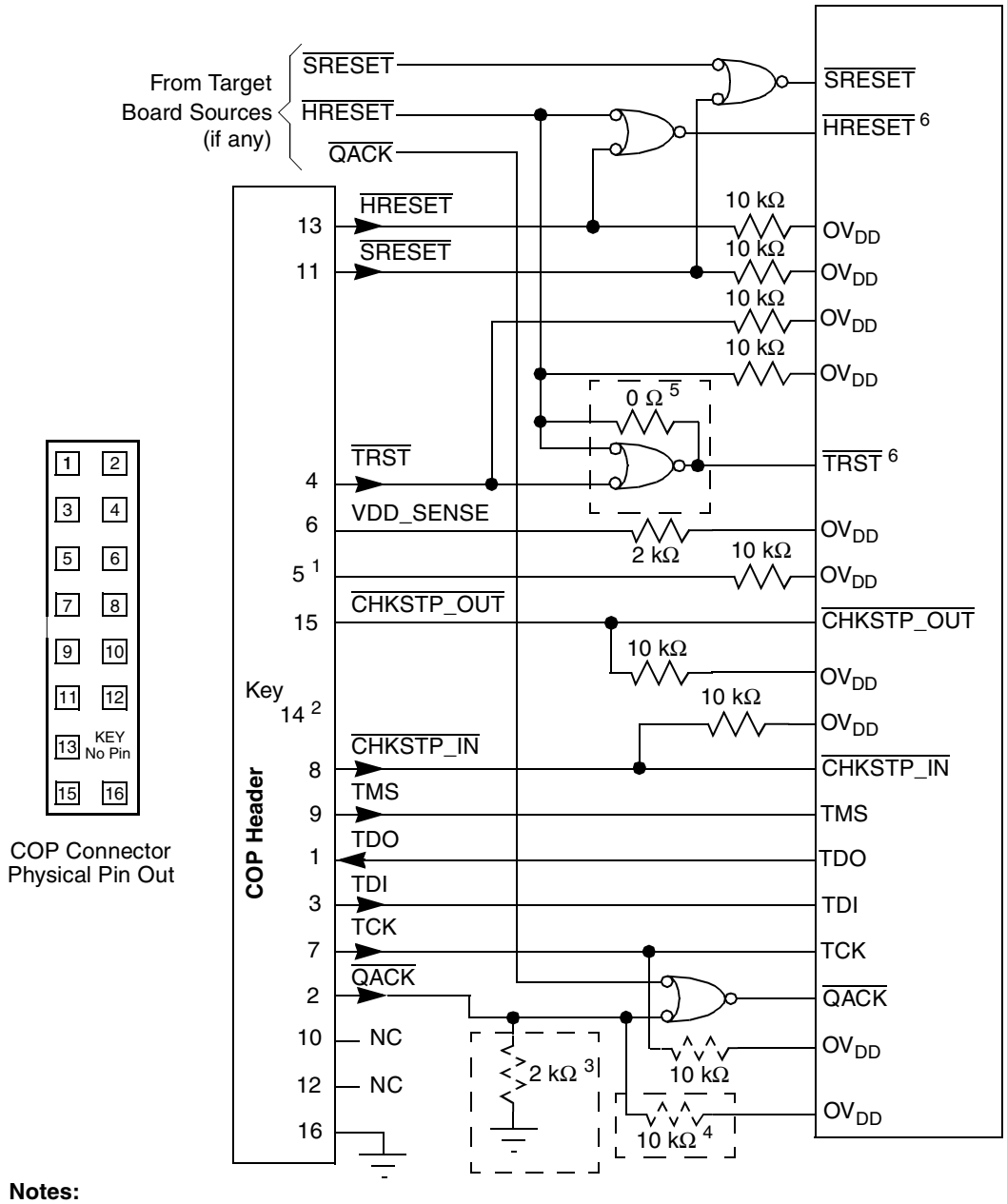
The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on




**Notes:**

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7410. Connect pin 5 of the COP header to $OV_{DD}$ with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

**Figure 25. COP Connector Diagram**

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 25; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 25 is usually connected to the PCI bridge chip in a system and is an input to the MPC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

## 8.8 Thermal Management Information

This section provides thermal management information for the MPC7410 for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods such as spring clip to holes in the printed circuit board or with screws and springs to the printed circuit board; see Figure 26 for the BGA package and Figure 27 for the LGA package. This spring force should not exceed 5.5 pounds of force. Note that care should be taken to avoid focused forces being applied to die corners and/or edges when mounting heat sinks.

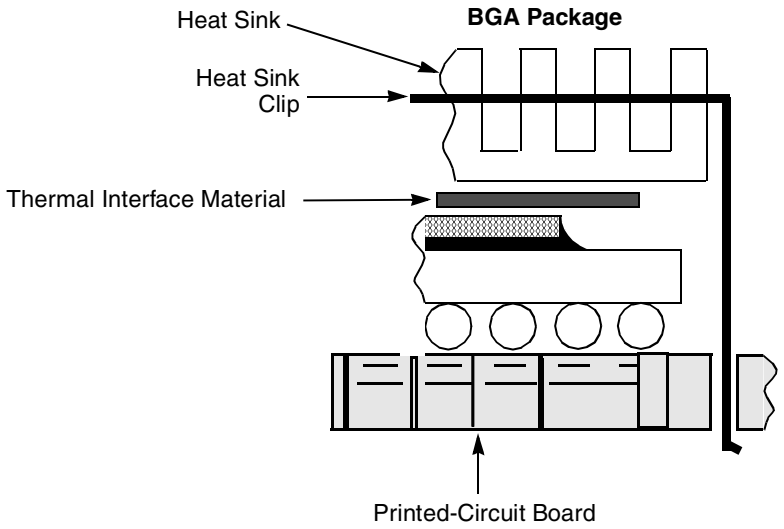



**Figure 26. BGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option**

Figure 29 describes the thermal performance of selected thermal interface materials.

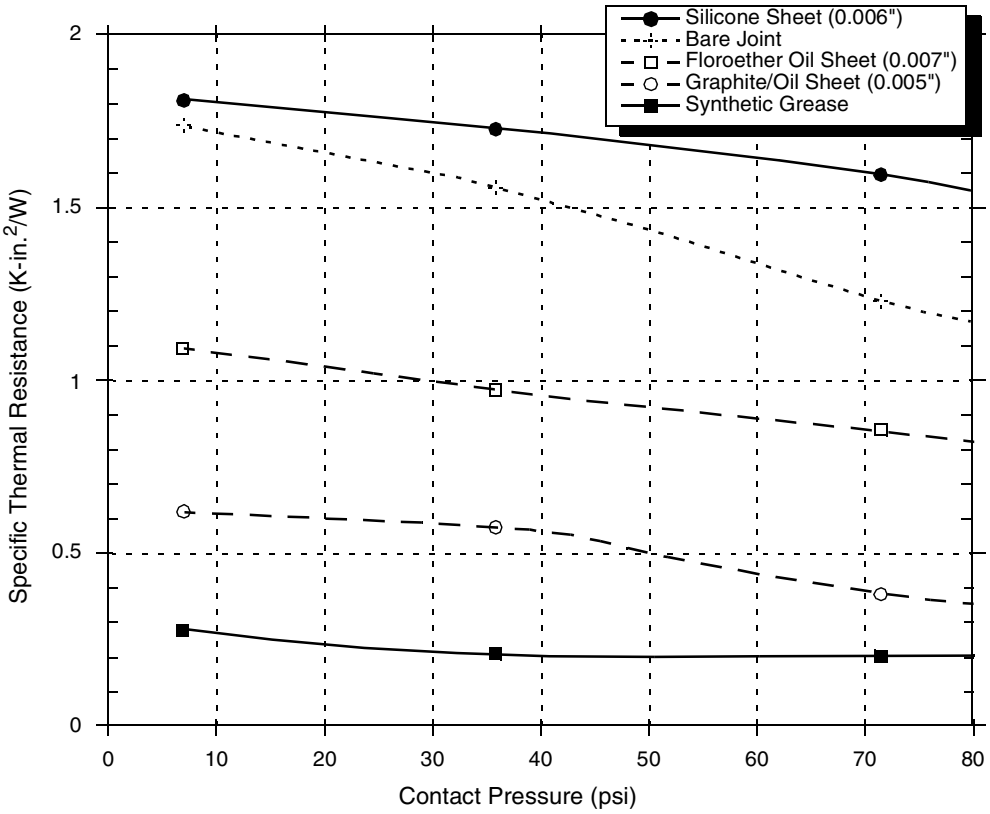



**Figure 29. Thermal Performance of Select Thermal Interface Material**

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Court<br>Woburn, MA 01888-4014<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Dow-Corning Electronic Materials<br>2200 W. Salzburg Rd.<br>Midland, MI 48686-0997<br>Internet: www.dow.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |

**Table 16. Document Revision History (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 1.1 | — | Internal release. |
| | | Table 12—added note 16 for $\overline{\text{ABB}}$/$\overline{\text{AMON}}$ and $\overline{\text{DBB}}$/$\overline{\text{DMON}}$ signal clarification. |
| | | Table 12—changed $\overline{\text{CHK}}$ note 4 reference to note 2, signal is for factory test only. Changed previous note 4 ($\overline{\text{CHK}}$ related) to now provide additional PLL info. |
| | | Table 1—modified maximum value for $OV_{DD}$ from –0.3 to 3.465 to now be –0.3 to 3.6 and $L2OV_{DD}$ from –0.3 to 2.6 to now be –0.3 to 2.8. Modified note 6, $OV_{DD}$ for revisions prior to Rev. 1.4 have maximum value for $OV_{DD}$ of –0.3 to 2.8. |
| | | Table 8—removed note 12. L2_TSTCLK is for factory use only (see Table 12, note 2). |
| | | Section 1.10.2—revised section to include nomenclature tables for part markings not covered by this spec. |
| | | Figure 2—added that under/overshoot for $L2OV_{DD}$ references $t_{L2CLK}$ while $OV_{DD}$ references $t_{SYSCLK}$. |
| | | Table 4—added HCTE package (HX package descriptor) thermal characteristics. |
| | | Section 1.5—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same pin assignments. |
| | | Section 1.6—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same pinout listings. |
| | | Section 1.7—added HCTE package (HX package descriptor). Both the CBGA and HCTE packages have the same package parameters and dimensions. |
| | | Table 17—added HCTE package (HX package descriptor) to part numbering nomenclature. |
| | | Table 21—added MPC7410THXnnnLE extended temperature HCTE package part numbers and part number specification document reference. |