Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc7410vs500le

- The MPC7410 is implemented in a next generation process technology for core frequency improvement.
- The MPC7410 floating-point unit has been improved to make latency equal for double- and single-precision operations involving multiplication.
- The completion queue has been extended to eight slots.
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750 four-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback).

Some comments on the MPC7410 with respect to the MPC7400:

- The MPC7410 adds configurable direct-mapped SRAM capability to the L2 cache interface.
- The MPC7410 adds 32-bit interface support to the L2 cache interface. The MPC7410 implements a 19th L2 address pin (L2ASPARE on the MPC7400) in order to support additional address range.
- The MPC7410 removes support for 3.3-V I/O on the L2 cache interface.

Figure 1 shows a block diagram of the MPC7410.

2 Features

This section summarizes features of the MPC7410 implementation of the PowerPC architecture. Major features of the MPC7410 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)

- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754™ single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations

  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32 Kbyte, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32 Kbyte, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-Kbyte, 1-Mbyte, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-Kbyte), 64-byte (1-Mbyte), or 128-byte (2-Mbyte) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256 Kbytes, 512 Kbytes, 1 Mbyte, or 2 Mbytes of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.8 V ± 100 mV	V	—
PLL supply voltage		AV_{DD}	1.8 V ± 100 mV	V	—
L2 DLL supply voltage		$L2AV_{DD}$	1.8 V ± 100 mV	V	—
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 100 mV	V	—
	BVSEL = $\overline{\text{HRESET}}$	OV_{DD}	2.5 V ± 100 mV	V	—
	BVSEL = ¬$\overline{\text{HRESET}}$ or BVSEL = 1	OV_{DD}	3.3 V ± 165 mV	V	2, 3
L2 bus supply voltage	L2VSEL = 0	$L2OV_{DD}$	1.8 V ± 100 mV	V	—
	L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1	$L2OV_{DD}$	2.5 V ± 100 mV	V	—
Input voltage	Processor bus and JTAG signals	V_{in}	GND to OV_{DD}	V	—
	L2 bus	V_{in}	GND to $L2OV_{DD}$	V	—
Die-junction temperature		T_j	0 to 105	°C	—

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a recommended OV_{DD} value of 2.5 V ± 100 mV for BVSEL = 1.
3. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support BVSEL = ¬$\overline{\text{HRESET}}$.

Table 4 provides the package thermal characteristics for the MPC7410.

Table 4. Package Thermal Characteristics

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	18	20	°C/W	1, 2
Junction-to-ambient thermal resistance, 1m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	16	°C/W	1, 2
Junction-to-ambient thermal resistance, 2m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	13	15	°C/W	1, 2
Junction-to-board thermal resistance	$R_{\theta JB}$	9	11	°C/W	3

Table 5. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
High-Z (off-state) leakage current, V_{in} = $L2OV_{DD}/OV_{DD}$	1.8	I_{TSI}	—	20	µA	2, 3, 5, 7
	2.5	I_{TSI}	—	35		
	3.3	I_{TSI}	—	70		
Output high voltage, I_{OH} = –5 mA	1.8	V_{OH}	$(L2)OV_{DD}$ – 0.45	—	V	8
	2.5	V_{OH}	1.7	—		
	3.3	V_{OH}	2.4	—		
Output low voltage, I_{OL} = 5 mA	1.8	V_{OL}	—	0.45	V	8
	2.5	V_{OL}	—	0.4		
	3.3	V_{OL}	—	0.4		
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	6.0	pF	3, 4, 7

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes factory test signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and $L2OV_{DD}$, or both OV_{DD} and $L2OV_{DD}$ must vary in the same direction (for example, both OV_{DD} and $L2OV_{DD}$ vary by either +5% or –5%).
6. Measured at max $OV_{DD}/L2OV_{DD}$.
7. Excludes IEEE 1149.1 boundary scan (JTAG) signals.
8. For JTAG support: all signals controlled by BVSEL and L2VSEL will see $V_{IL}/V_{IH}/V_{OL}/V_{OH}/CV_{IH}/CV_{IL}$ DC limits of 1.8 V mode while either the EXTEST or CLAMP instruction is loaded into the IEEE 1149.1 instruction register by the UpdateIR TAP state until a different instruction is loaded into the instruction register by either another UpdateIR or a Test-Logic-Reset TAP state. If only $\overline{\text{TSRT}}$ is asserted to the part, and then a SAMPLE instruction is executed, there is no way to control or predict what the DC voltage limits are. If $\overline{\text{HRESET}}$ is asserted before executing a SAMPLE instruction, the DC voltage limits will be controlled by the BVSEL/L2VSEL settings during $\overline{\text{HRESET}}$. Anytime $\overline{\text{HRESET}}$ is not asserted (that is, just asserting $\overline{\text{TRST}}$), the voltage mode is not known until either EXTEST or CLAMP is executed, at which time the voltage level will be at the DC limits of 1.8 V.

Table 6 provides the power consumption for the MPC7410.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency			Unit	Notes
	400 MHz	450 MHz	500 MHz		
Full-On Mode					
Typical	4.2	4.7	5.3	W	1, 3
Maximum	9.5	10.7	11.9	W	1, 2
Doze Mode					
Maximum	4.3	4.8	5.3	W	1
Nap Mode					
Maximum	1.35	1.5	1.65	W	1
Sleep Mode					
Maximum	1.3	1.45	1.6	W	1
Sleep Mode—PLL and DLL Disabled					
Typical	600	600	600	mW	1
Maximum	1.1	1.1	1.1	W	1

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at 105°C and V_{DD} = 1.8 V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65°C and V_{DD} = 1.8 V in a system while running typical benchmarks.

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7410. After fabrication, functional parts are sorted by maximum processor core frequency, see Section 4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, “Ordering Information.”

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 8. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
Input setup	t_{IVKH}	1.0	—	ns	4
Input hold	t_{IXKH}	0	—	ns	4
Output valid times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSV} t_{KHARV} t_{KHOV}	 — — —	 3.0 2.3 3.0	ns	5, 6
Output hold times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	5
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	9
SYSCLK to output high impedance (all except $\overline{ABB}$/$\overline{AMON}$(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/$\overline{DMON}$(0), $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{ABB}$/$\overline{AMON}$(0), $\overline{DBB}$/$\overline{DMON}$(0) high impedance after precharge	t_{KHABPZ}	—	1	t_{SYSCLK}	3, 7, 9
Maximum delay to $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 8, 9

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

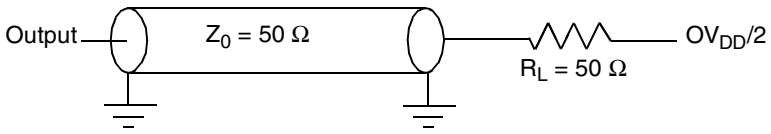


Figure 4. AC Test Load

Table 9. L2CLK Output AC Timing Specifications (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK_OUT output jitter	—	—	±150	—	±150	—	±150	ps	6

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2CLK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 7.

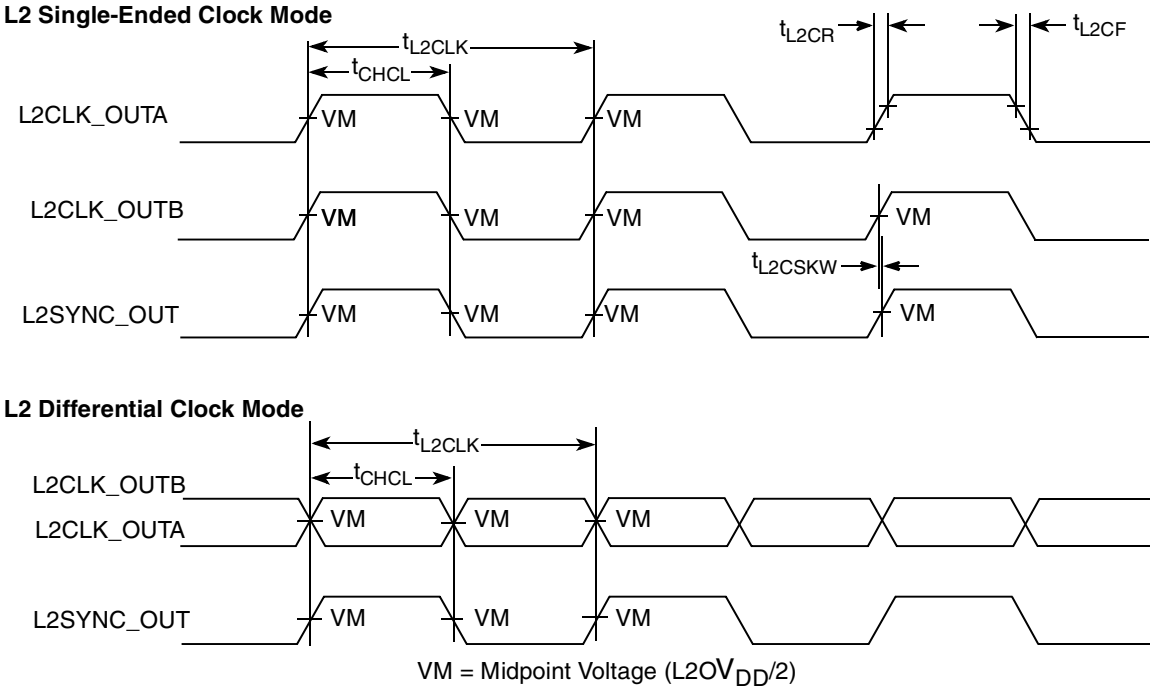


Figure 7. L2CLK_OUT Output Timing Diagram

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

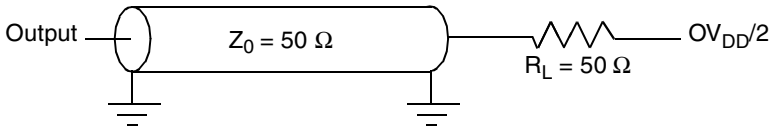


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

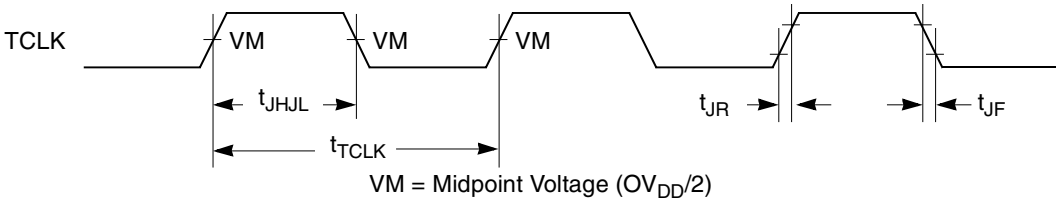


Figure 12. JTAG Clock Input Timing Diagram

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	BVSEL	—
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	BVSEL	—
$\overline{\text{DRDY}}$	K9	Low	Output	BVSEL	6, 8, 13
$\overline{\text{DBWO}}$ DTI[0]	D1	Low	Input	BVSEL	—
DTI[1:2]	H6, G1	High	Input	BVSEL	5, 10, 13
$\overline{\text{EMODE}}$	A3	Low	Input	BVSEL	7, 10
$\overline{\text{GBL}}$	B1	Low	I/O	BVSEL	—
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	N/A	—
$\overline{\text{HIT}}$	B5	Low	Output	BVSEL	6, 8
$\overline{\text{HRESET}}$	B6	Low	Input	BVSEL	—
$\overline{\text{INT}}$	C11	Low	Input	BVSEL	—
L1_TSTCLK	F8	High	Input	BVSEL	2
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	L2VSEL	—
L2ADDR[17:18]	K19,W19	High	Output	L2VSEL	8
$L2AV_{DD}$	L13	—	Input	V_{DD}	—
$\overline{\text{L2CE}}$	P17	Low	Output	L2VSEL	—
L2CLK_OUTA	N15	High	Output	L2VSEL	—
L2CLK_OUTB	L16	High	Output	L2VSEL	—
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	L2VSEL	—
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	L2VSEL	—
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15	—	—	N/A	11
L2SYNC_IN	L14	High	Input	L2VSEL	—
L2SYNC_OUT	M14	High	Output	L2VSEL	—
L2_TSTCLK	F7	High	Input	BVSEL	2

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7410, 360 CBGA and 360 HCTE packages.

7.1 Package Parameters for the MPC7410, 360 CBGA and 360 HCTE_CBGA

The package parameters are as provided in the following list. The package types are the 25 × 25 mm, 360-lead ceramic ball grid array package (CBGA) or the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package (HCTE_CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	6.8 ppm/°C (CBGA) 12.3ppm/°C (HCTE_CBGA)

7.2 Package Parameters for the MPC7410, 360 HCTE_CBGA (Lead Free C5 Spheres)

The package parameters are as listed here. The package types are the 25 × 25 mm, 360-lead high coefficient of thermal expansion CBGA package with lead-free C5 spheres (HCTE_CBGA lead-free spheres).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.76 mm (30 mil)
Coefficient of thermal expansion	12.3ppm/°C

MPC7410 core, and the phase adjustment range that the L2 DLL supports. Table 14 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 133 MHz. Sample core-to-L2 frequencies for the MPC7410 is shown in Table 14. In this example, shaded cells represent settings that, for a given core frequency, result in L2 frequencies that do not comply with the minimum and maximum L2 frequencies listed in Table 10.

Table 14. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3	÷3.5	÷4
350	350	233	175	140	—	—	—
366	366	244	183	147	—	—	—
400	400	266	200	160	133	—	—
433	—	288	216	173	144	—	—
450	—	300	225	180	150	—	—
466	—	311	233	186	155	133	—
500	—	333	250	200	166	143	—

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz.

8.2 PLL and DLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC7410 to supply power to the PLL and DLL, respectively. Both AV_{DD} and $L2AV_{DD}$ can be supplied power from the V_{DD} power plane. High frequency noise in the 500 kHz to 10 MHz resonant frequency range of the PLL on the V_{DD} power plane could affect the stability of the internal clocks.

On systems that use the MPC7410 HCTE device, the AV_{DD} and $L2AV_{DD}$ input signals should both implement the circuit shown in Figure 21.

On systems that use the MPC7410 CBGA device, the $L2AV_{DD}$ input should implement the circuit shown in Figure 21.

When selecting which filter to use on the AV_{DD} input of the MPC7410 CBGA device specifically, system designers should refer to Erratum No. 18 in the *MPC7410 RISC Microprocessor Chip Errata* (MPC7410CE). The AV_{DD} input of the MPC7410 CBGA device is sensitive to system noise on both the V_{DD} power plane, as described above, and the OV_{DD} power plane as described in the Erratum No. 18. With these AV_{DD} sensitivities to OV_{DD} and V_{DD} noise, care must be taken when selecting the filter circuit for the AV_{DD} input of the MPC7410 CBGA device. Erratum No. 18 does not apply to the AV_{DD} input of the MPC7401 HCTE device, nor does it affect the $L2AV_{DD}$ input of either the HCTE or the CBGA device.

As described in Erratum No. 18, when there is a high amount of noise on the OV_{DD} power plane due to I/O switching rates, it is possible for the OV_{DD} noise to couple into the PLL supply voltage (AV_{DD}) internal to the MPC7410 CBGA package. It is the recommendation of Freescale, that new designs using the MPC7410 CBGA package provide the ability to implement either filter shown in Figure 21 and Figure 22 at the AV_{DD} input. Existing designs that implemented Figure 21 on AV_{DD} may never experience the error described in Erratum No. 18. Both new and

R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 24 describes the alternate driver impedance measurement circuit.

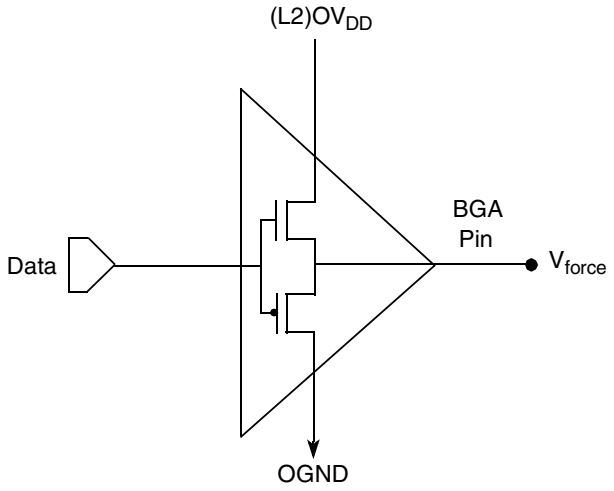


Figure 24. Alternate Driver Impedance Measurement Circuit

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.8 V, OV_{DD} = 2.5 V, T_j = 0° – 105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5–54.3	42.7–54.1	Z_0	Ω
R_P	37.3–55.3	39.3–50.0	Z_0	Ω

8.6 Pull-Up Resistor Requirements

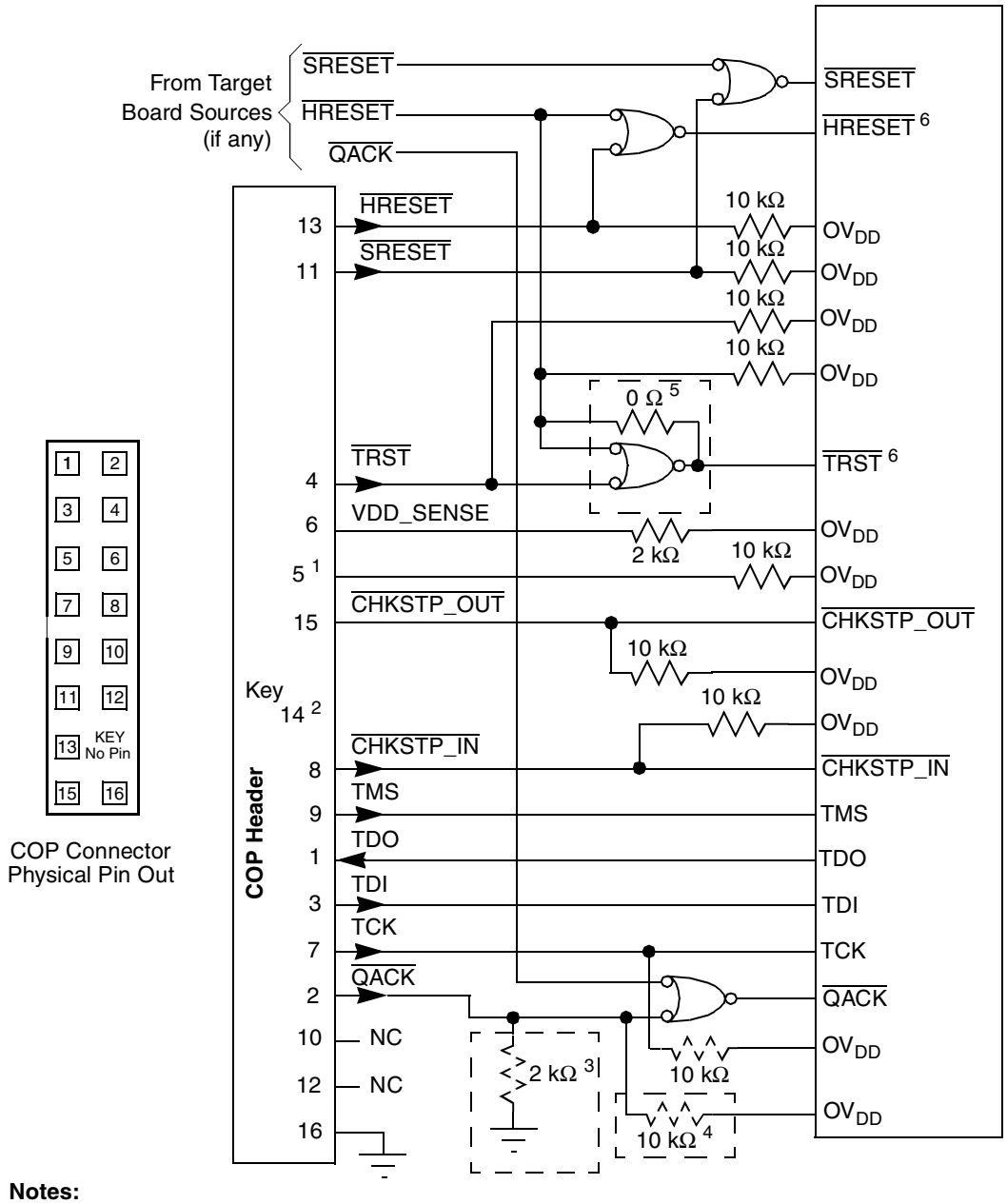
The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7410. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 25. COP Connector Diagram

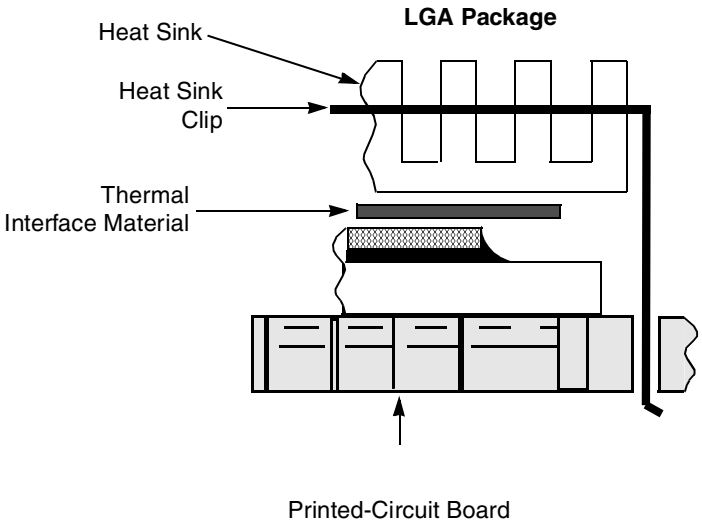


Figure 27. LGA Package Exploded Cross-Sectional View with Heat Sink Clip to PCB Option

The board designer can choose between several types of heat sinks to place on the MPC7410. There are several commercially-available heat sinks for the MPC7410 from the following vendors:

Aavid Thermalloy 70 Commercial Street, Suite 200 Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

8.8.1 Internal Package Conduction Resistance

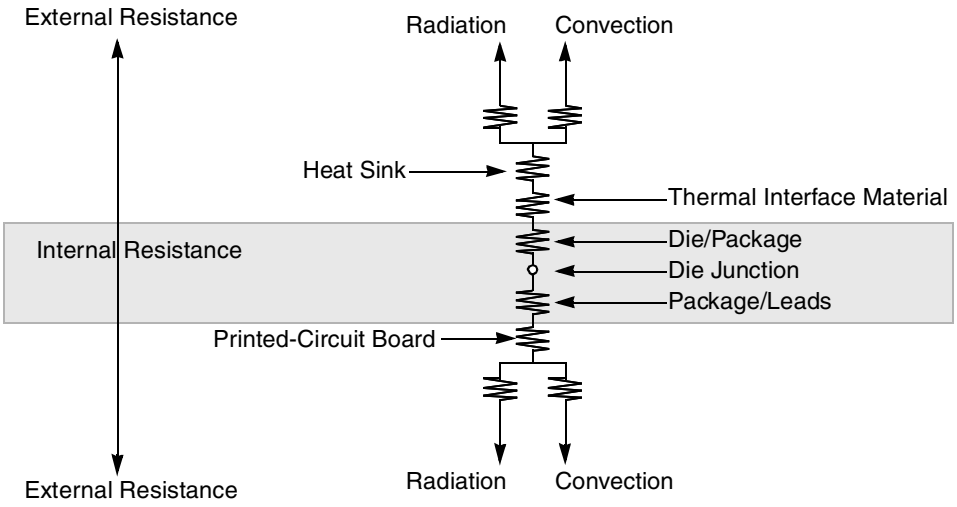
For the exposed-die packaging technology, shown in Table 3, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 28 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.



Note the internal versus external package resistance.

Figure 28. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

8.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 26). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
5	4/13/2005	Section numbering revised. In all previous versions, section numbering began with '1.' These extra '1's' were deleted. For example, previously numbered section 1.8.2 changed to 8.2.
		Section 7.1—added CTE value for HCTE package. Corrected minimum module height from 2.65 mm to 2.72 mm per Figure 17.
		Section 3—added HCTE_LGA (VS package descriptor) package description which is the HCTE_CBGA (HX package descriptor) with the spheres removed.
		Table 4—generalized 'HCTE CBGA' column to 'HCTE' to include both HCTE_CBGA and HCTE_LGA package thermal characteristics.
		Section 5—added HCTE_LGA package. The HCTE_LGA has the same pin assignments as the CBGA and HCTE_CBGA packages. Added side view Part C for HCTE_LGA.
		Section 6—added HCTE_LGA package (VS package descriptor). The HCTE_LGA has the same pinout listing as the CBGA and HCTE packages.
		Section 7.3—added HCTE_LGA package parameters.
		Section 7.4—added HCTE_LGA package mechanical dimensions.
		Table 17—added HCTE_LGA package (VS package descriptor) to part numbering nomenclature.
4	—	Table 5—Changed measurement test condition I_{OH} from -6mA to –5 mA for V_{OH} and I_{OL} from 6 mA to 5 mA for V_{OL} per Product Bulletin.
		Section 1.8.2—revised text regarding AV_{DD} filter selection for the CBGA package.
3	—	Table 6—Changed note 1 to specify that OV_{DD} and $L2OV_{DD}$ power is typically <5% of V_{DD} power.
		Figure 17—revised diagram and dimensions to specify 'cap regions' versus individual cap measurements. Moved individual capacitor placement to separate figure.
		Figure 18—Added this figure to show each individual capacitor placement and value.
		Figure 22—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK.
2	—	Public release, includes Rev 1.1 changes.
		Section 1.7.2—added package capacitor values.
		Section 1.8.6—added recommendation that strong pull-up/down resistors be used on the PLL_CFG[0:3] signals.
		Table 8—removed mode input setup and hold times. These inputs adhere to the general input setup and hold specifications.
		Figure 5—revised mode input diagram to show sample points around $\overline{\text{HRESET}}$ negation.
		Section 1.3—added HCTE package description.
		Figure 22—added note 6 to emphasize that COP emulator and target board need to be able to drive $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ independently to the CPU.
		Section 1.8.2—revised section for HCTE package. Added text and figure for AV_{DD} filter for the CBGA package.
		Section 1.8.6—removed $\overline{\text{AACK}}$, $\overline{\text{TEA}}$, and $\overline{\text{TS}}$ from control signals requiring pull-ups. Removed $\overline{\text{TBST}}$ from snooped transfer attribute list. $\overline{\text{TBST}}$ is an output and is not snooped.

Table 16. Document Revision History (continued)

Revision	Date	Substantive Change(s)
0.3	—	Added 3.3 V support on the processor bus (BVSEL).
		Table 7—update typical and maximum power numbers for full-on mode in. Removed note 4. Reworded notes 2 and 3.
		Table 9, Note 2—removed reference to application note.
		Figure 17—corrected side view datum A to be datum C.
		Section 1.8.7—added $\overline{CI}$ and $\overline{WT}$ to transfer attribute signals requiring pull-ups.
		Section 1.8.7—added 1-kΩ pull-up recommendation to $\overline{GBL}$ when $\overline{GBL}$ is not connected.
		Table 2— added pull-down resistance necessary for internally pulled-up voltage select pins. Added 3.3-V support for BVSEL.
		Table 13—added note 14 for BVSEL, L2VSEL, and $\overline{TRST}$ pins to address pull-down resistance necessary for these internally pulled-up pins to recognize a low signal.
		Table 6—lowered 2.5 V CV_{IH} from 2.2 to 2.0 V to be compatible with V_{OH} of the MPC107. Added support for 3.3-V processor bus.
		Table 15—modified note 1, use L2CR[L2SL] for L2CLK frequency less than 150 MHz.
		Table 8—revised note 2 discussing for 3.3-V bus voltage support.
		Table 14—added note 5, do not use PL off during power-up sequence.
		Table 1—update output hold times (t_{L2CHOX}).
0.2	—	Corrected Section 1.3—technology from 0.13 µm to 0.18 µm.
		Updated Table 7—adds power consumption numbers; adds note on estimated decrease w/o AltiVec.
		Updated Table 8—adds minimum values for processor frequency and VCO frequency.
		Updated Table 9—input setup, output valid times, output hold times, SYSCLK to output high impedance.
		Updated Table 11—L2SYNC_IN to high impedance.
		Updated Figure 17—mechanical dimensions, adds capacitor pad dimensions.
0.1	—	Minor updates.
0	—	Initial release.

10 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 10.1, “Part Numbers Addressed by This Specification.” Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

10.1 Part Numbers Addressed by This Specification

Table 17 provides the Freescale part numbering nomenclature for the MPC7410 Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 17. Part Numbering Nomenclature

Mxx	**7410**	***xx***	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Package [1]**	**Processor Frequency [2]**	**Application Modifier**	**Revision Level**
MPC	7410	RX = CBGA	400 450 500	L: 1.8 V ± 100 mV 0° to 105°C	C: 1.2; PVR = 800C 1102 D: 1.3; PVR = 800C 1103 E: 1.4; PVR = 800C 1104
		HX = HCTE_CBGA			E: 1.4; PVR = 800C 1104
		VS = HCTE_LGA			
MC		VU = HCTE_CBGA (Lead Free C5 Solder Spheres)	400 500		

Notes:

1. See Section 7, “Package Description,” for more information on available package types and Table 4 for more information on thermal characteristics.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.