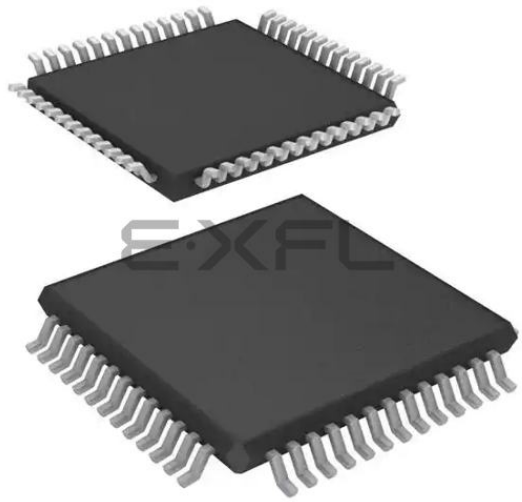

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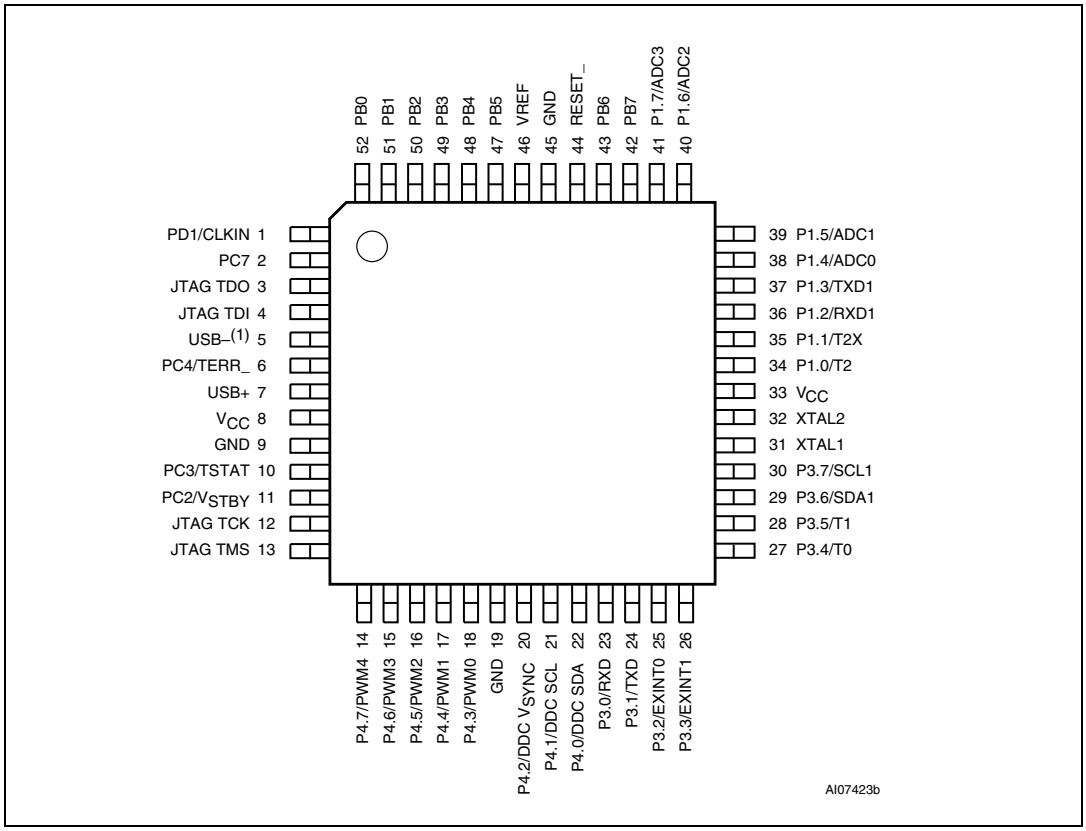
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, UART/USART
Peripherals	LVR, POR, PWM, WDT
Number of I/O	37
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3233b-40t6

Figure 2. TQFP52 connections



1. Pull-up resistor required on pin 5 (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices) for all 52-pin devices, with or without USB function.

Table 4. Arithmetic instructions (continued)

Mnemonic	Operation	Addressing modes			
		Dir.	Ind.	Reg.	Imm.
INC	A = A + 1	Accumulator only			
INC <byte>	<byte> = <byte> + 1	X	X	X	
INC DPTR	DPTR = DPTR + 1	Data Pointer only			
DEC	A = A – 1	Accumulator only			
DEC <byte>	<byte> = <byte> – 1	X	X	X	
MUL AB	B:A = B x A	Accumulator and B only			
DIV AB	A = Int[A / B] B = Mod[A / B]	Accumulator and B only			
DA A	Decimal Adjust	Accumulator only			

2.11 Logical instructions

Table 5 lists logical instructions for UPSD323xx devices. The instructions that perform Boolean operations (AND, OR, Exclusive OR, NOT) on bytes perform the operation on a bit-by-bit basis. That is, if the Accumulator contains 00110101B and byte contains 01010011B, then:

ANL A, <byte>

will leave the Accumulator holding 00010001B.

The addressing modes that can be used to access the <byte> operand are listed in *Table 5*.

The ANL A, <byte> instruction may take any of the forms:

ANL A,7FH(direct addressing)

ANL A, @R1 (indirect addressing)

ANL A,R6 (register addressing)

ANL A,#53H (immediate constant)

Note: Boolean operations can be performed on any byte in the internal Data Memory space without going through the Accumulator. The XRL <byte>, #data instruction, for example, offers a quick and easy way to invert port bits, as in:

XRL P1, #0FFH.

If the operation is in response to an interrupt, not using the Accumulator saves the time and effort to push it onto the stack in the service routine.

The Rotate instructions (RL A, RLC A, etc.) shift the Accumulator 1 bit to the left or right. For a left rotation, the MSB rolls into the LSB position. For a right rotation, the LSB rolls into the MSB position.

The SWAP A instruction interchanges the high and low nibbles within the Accumulator. This is a useful operation in BCD manipulations. For example, if the Accumulator contains a

Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
A1	PWMCON	PWML	PWMP	PWME	CFG4	CFG3	CFG2	CFG1	CFG0	00	PWM Control Polarity
A2	PWM0									00	PWM0 Output Duty Cycle
A3	PWM1									00	PWM1 Output Duty Cycle
A4	PWM2									00	PWM2 Output Duty Cycle
A5	PWM3									00	PWM3 Output Duty Cycle
A6	WDRST									00	Watch Dog Reset
A7	IEA	EDDC			ES2			EI^{2}C	EUSB	00	Interrupt Enable (2nd)
A8	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00	Interrupt Enable
A9											
AA	PWM4P									00	PWM 4 Period
AB	PWM4W									00	PWM 4 Pulse Width
AE	WDKEY									00	Watch Dog Key Register
B0	P3									FF	Port 3
B1	PSCL0L									00	Prescaler 0 Low (8-bit)
B2	PSCL0H									00	Prescaler 0 High (8-bit)
B3	PSCL1L									00	Prescaler 1 Low (8-bit)
B4	PSCL1H									00	Prescaler 1 High (8-bit)
B7	IPA	PDDC			PS2			PI2C	PUSB	00	Interrupt Priority (2nd)
B8	IP			PT2	PS	PT1	PX1	PT0	PX0	00	Interrupt Priority
C0	P4									FF	New Port 4
C8	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00	Timer 2 Control

Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
C9	T2MOD								DCEN	00	Timer 2 mode
CA	RCAP2L									00	Timer 2 Reload low
CB	RCAP2H									00	Timer 2 Reload High
CC	TL2									00	Timer 2 Low byte
CD	TH2									00	Timer 2 High byte
D0	PSW	CY	AC	FO	RS1	RS0	OV		P	00	Program Status Word
D1	S1SETUP									00	DDC I^2C (S1) Setup
D2	S2SETUP									00	I^2C (S2) Setup
D4	RAMBUF									XX	DDC Ram Buffer
D5	DDCDAT									00	DDC Data xmit register
D6	DDCADR									00	Addr pointer register
D7	DDCCON	—	EX_DAT	SWENB	DDC_AX	DDCINT	DDC1EN	SWHINT	M0	00	DDC Control Register
D8	S1CON	CR2	ENI1	STA	STO	ADDR	AA	CR1	CR0	00	DDC I^2C Control Reg
D9	S1STA	GC	Stop	Intr	TX-Md	Bbusy	Blost	ACK_R	SLV	00	DDC I^2C Status
DA	S1DAT									00	Data Hold Register
DB	S1ADR									00	DDC I^2C address
DC	S2CON	CR2	EN1	STA	STO	ADDR	AA	CR1	CR0	00	I^2C Bus Control Reg
DD	S2STA	GC	Stop	Intr	TX-Md	Bbusy	Blost	ACK_R	SLV	00	I^2C Bus Status
DE	S2DAT									00	Data Hold Register
DF	S2ADR									00	I^2C address
E0	ACC									00	Accumulator

Table 17. PSD module register address offset (continued)

CSIOP addr offset	Register name	Bit register name								Reset value	Comments
		7	6	5	4	3	2	1	0		
C0	Primary Flash Protection	Sec7_ Prot	Sec6_ Prot	Sec5_ Prot	Sec4_ Prot	Sec3_ Prot	Sec2_ Prot	Sec1_ Prot	Sec0_ Prot		Bit = 1 sector is protected
C2	Secondary Flash Protection	Security _Bit	*	*	*	Sec3_ Prot	Sec2_ Prot	Sec1_ Prot	Sec0_ Prot		Security Bit = 1 device is secured
B0	PMMR0	*	*	PLD Mcells clk	PLD array-clk	PLD Turbo	*	APD enable	*	00	Control PLD power consumption
B4	PMMR2	*		PLD array Ale	PLD array Cntl2	PLD array Cntl1	PLD array Cntl0	*	*	00	Blocking inputs to PLD array
E0	Page									00	Page Register
E2	VM	Periph-mode	*	*	FL_ data	Boot_ data	FL_ code	Boot_ code	SR_ code		Configure 8032 Program and Data Space

1. (Register address = CSIOP address + address offset; where CSIOP address is defined by user in PSDsoft)
* indicates bit is not used and must be set to '0'.

Table 21. Description of the IEA bits

Bit	Symbol	Function
7	EDDC	Enable DDC Interrupt
6	—	Not used
5	—	Not used
4	ES2	Enable 2nd USART Interrupt
3	—	Not used
2	—	Not used
1	EI2C	Enable I²C Interrupt
0	EUSB	Enable USB Interrupt

Table 22. Description of the IP bits

Bit	Symbol	Function
7	—	Reserved
6	—	Reserved
5	PT2	Timer 2 Interrupt priority level
4	PS	USART Interrupt priority level
3	PT1	Timer 1 Interrupt priority level
2	PX1	External Interrupt (Int1) priority level
1	PT0	Timer 0 Interrupt priority level
0	PX0	External Interrupt (Int0) priority level

Table 23. Description of the IPA bits

Bit	Symbol	Function
7	PDDC	DDC Interrupt priority level
6	—	Not used
5	—	Not used
4	PS2	2nd USART Interrupt priority level
3	—	Not used
2	—	Not used
1	PI2C	I²C Interrupt priority level
0	PUSB	USB Interrupt priority level

Table 54. Description of the SxSTA bits

Bit	Symbol	Function
7	GC	General Call Flag
6	STOP	Stop Flag. This bit is set when a STOP condition is received
5	INTR(1,2)	Interrupt Flag. This bit is set when an I²C Interrupt condition is requested
4	TX_MODE	Transmission mode Flag. This bit is set when the I²C is a transmitter; otherwise this bit is reset
3	BBUSY	Bus Busy Flag. This bit is set when the bus is being used by another master; otherwise, this bit is reset
2	BLOST	Bus Lost Flag. This bit is set when the master loses the bus contention; otherwise this bit is reset
1	/ACK_REP	Acknowledge Response Flag. This bit is set when the receiver transmits the not acknowledge signal This bit is reset when the receiver transmits the acknowledge signal
0	SLV	Slave mode Flag. This bit is set when the I²C plays role in the Slave mode; otherwise this bit is reset

1. Interrupt Flag bit (INTR, SxSTA Bit 5) is cleared by Hardware as reading SxSTA register.
2. I²C interrupt flag (INTR) can occur in below case. (except DDC2B mode at SWENB=0)

Table 55. Data shift register (SxDAT: S1DAT, S2DAT)

7	6	5	4	3	2	1	0
SxDAT7	SxDAT6	SxDAT5	SxDAT4	SxDAT3	SxDAT2	SxDAT1	SxDAT0

15.3 Address register (SxADR: S1ADR, S2ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receive/transmitter.

The Start/Stop Hold Time Detection and System Clock registers (*Table 57* and *Table 58*) are included in the I²C unit to specify the start/stop detection time to work with the large range of MCU frequency values supported. For example, with a system clock of 40MHz.

Table 56. Address register (SxADR)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	—

1. SLA6 to SLA0: Own slave address.

Table 68. Description of the UISTA bits (continued)

Bit	Symbol	R/W	Function
4	TXD0F	R/W	Endpoint0 Data Transmit Flag. This bit is set after the data stored in Endpoint 0 transmit buffers has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag. To enable the next data packet transmission, TX0E must also be set. If TXD0F Bit is not cleared, a NAK handshake will be returned in the next IN transactions. RESET clears this bit.
3	RXD0F	R/W	Endpoint0 Data Receive Flag. This bit is set after the USB module has received a data packet and responded with ACK handshake packet. Software must clear this flag after all of the received data has been read. Software must also set RX0E Bit to one to enable the next data packet reception. If RXD0F Bit is not cleared, a NAK handshake will be returned in the next OUT transaction. RESET clears this bit.
2	TXD1F	R/W	Endpoint1 / Endpoint2 Data Transmit Flag. This bit is shared by Endpoints 1 and Endpoints 2. It is set after the data stored in the shared Endpoint 1/ Endpoint 2 transmit buffer has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag. To enable the next data packet transmission, TX1E must also be set. If TXD1F Bit is not cleared, a NAK handshake will be returned in the next IN transaction. RESET clears this bit.
1	EOPF	R/W	End of Packet Flag. This bit is set when a valid End of Packet sequence is detected on the D+ and D-line. Software must clear this flag. RESET clears this bit.
0	RESUMF	R/W	Resume Flag. This bit is set when USB bus activity is detected while the SUSPND Bit is set. Software must clear this flag. RESET clears this bit.

Table 69. USB Endpoint0 transmit control register (UCON0: 0EAh)

7	6	5	4	3	2	1	0
TSEQ0	STALL0	TX0E	RX0E	TP0SIZ3	TP0SIZ2	TP0SIZ1	TP0SIZ0

Table 83. Methods of programming different functional blocks of the PSD module

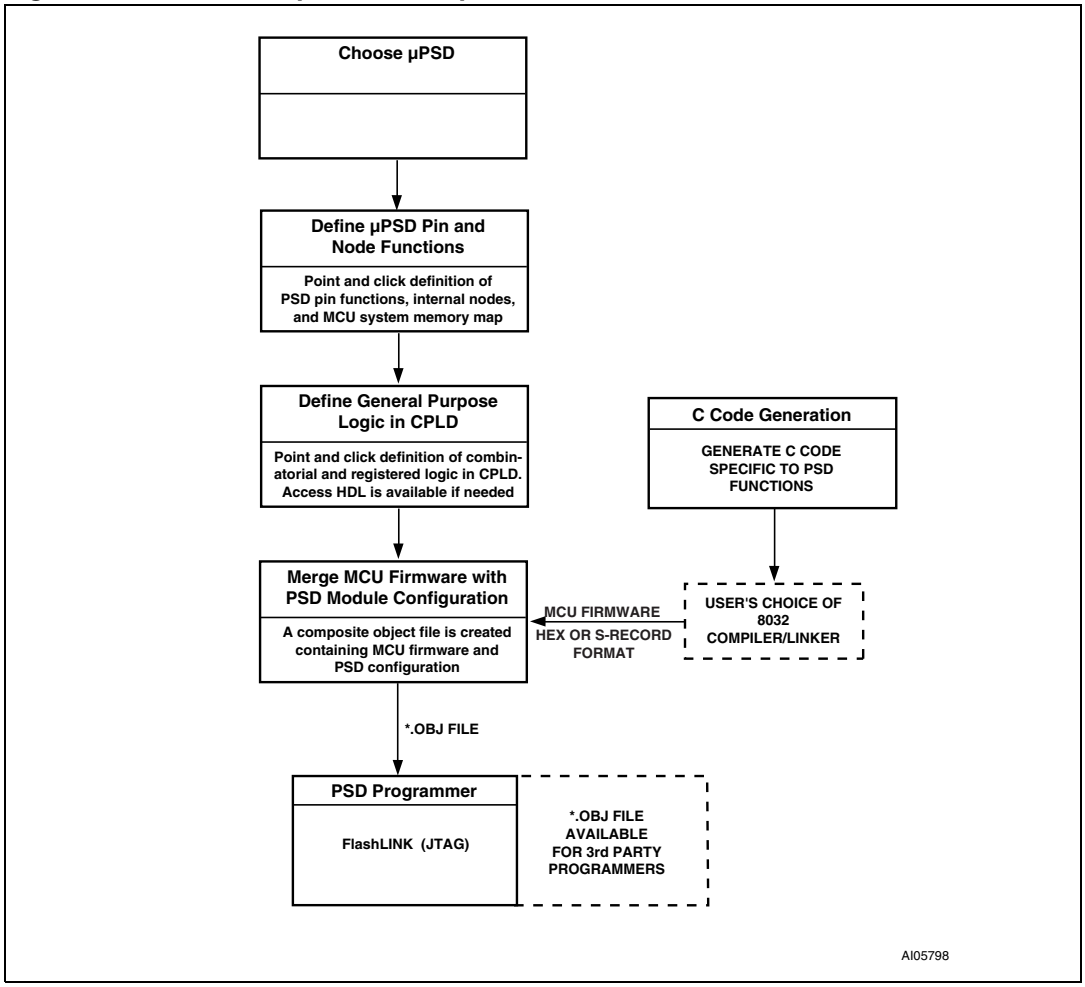
Functional Block	JTAG programming	Device programmer	IAP
Primary Flash memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD array (DPLD and CPLD)	Yes	Yes	No
PSD module configuration	Yes	Yes	No

19 Development system

UPSD323xx devices are supported by PSDsoft, a Windows-based software development tool (Windows-95, Windows-98, Windows-NT). A PSD module design is quickly and easily produced in a point and click environment. The designer does not need to enter Hardware Description Language (HDL) equations, unless desired, to define PSD module pin functions and memory map information. The general design flow is shown in *Figure 50*. PSDsoft is available from our web site (the address is given on the back page of this data sheet) or other distribution channels.

PSDsoft directly supports a low cost device programmer from ST: FlashLINK (JTAG). The programmer may be purchased through your local distributor/representative. UPSD323xx devices are also supported by third party device programmers. See our web site for the current list.

Figure 50. PSDsoft express development tool

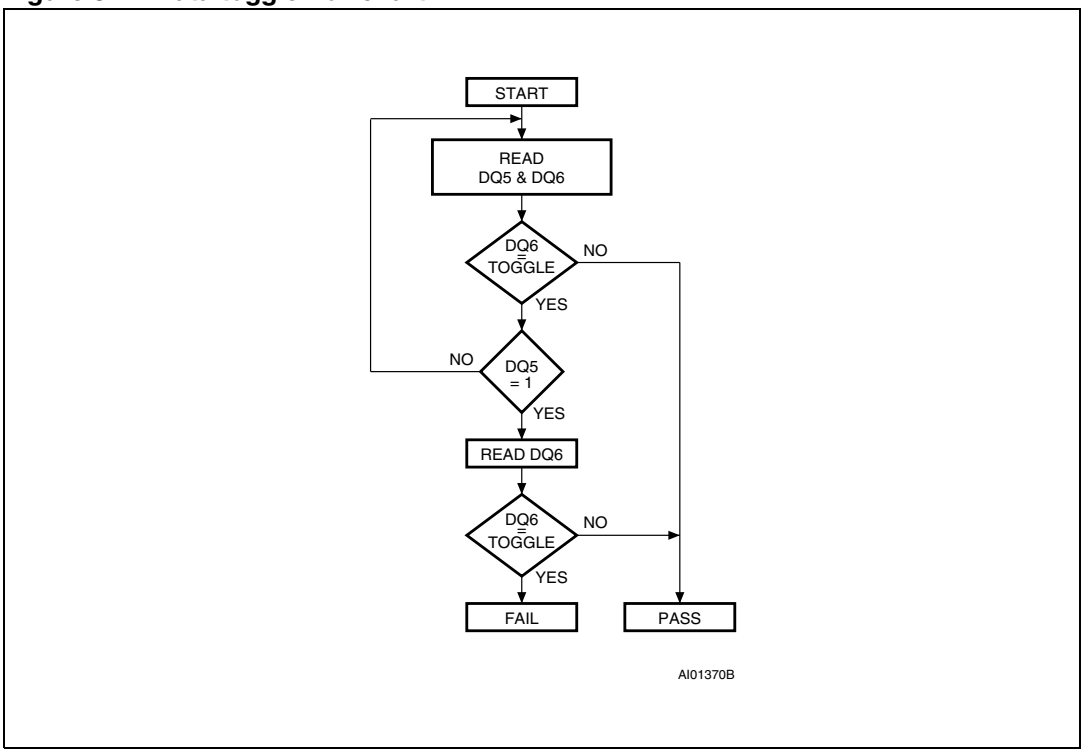


It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed, to compare the byte that was written to Flash memory with the byte that was intended to be written.

When using the Data Toggle method after an Erase cycle, *Figure 52* still applies. the Toggle Flag bit (DQ6) toggles until the Erase cycle is complete. A 1 on the Error Flag bit (DQ5) indicates a time-out condition on the Erase cycle; a '0' indicates no error. The MCU can read any location within the sector being erased to get the Toggle Flag bit (DQ6) and the Error Flag bit (DQ5).

PSDsoft Express generates ANSI C code functions which implement these Data Toggling algorithms.

Figure 52. Data toggle flowchart



22.6.3 Unlock Bypass

The Unlock Bypass instructions allow the system to program bytes to the Flash memories faster than using the standard Program instruction. The Unlock Bypass mode is entered by first initiating two Unlock cycles. This is followed by a third WRITE cycle containing the Unlock Bypass code, 20h (as shown in *Table 85*).

The Flash memory then enters the Unlock Bypass mode. A two-cycle Unlock Bypass Program instruction is all that is required to program in this mode. The first cycle in this instruction contains the Unlock Bypass Program code, A0h. The second cycle contains the program address and data. Additional data is programmed in the same manner. These instructions dispense with the initial two Unlock cycles required in the standard Program instruction, resulting in faster total Flash memory programming.

During the Unlock Bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset Flash instructions are valid.

Figure 53. Priority level of memory and I/O components in the PSD module

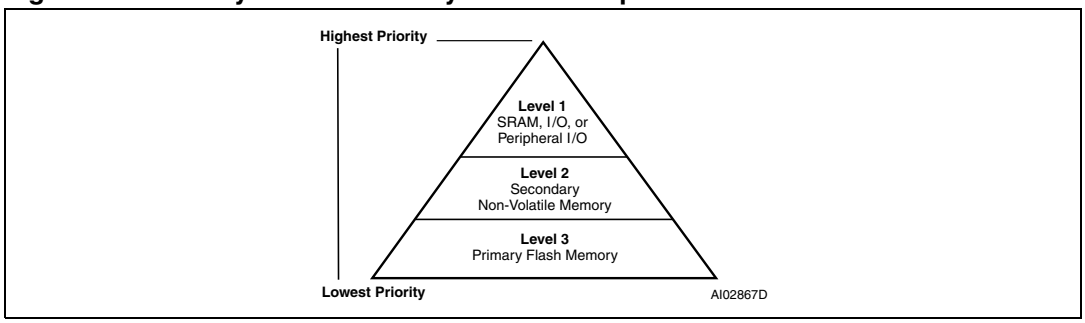


Table 89. VM register

Bit 7 PIO_EN	Bit 6	Bit 5	Bit 4 Primary FL_Data	Bit 3 Secondary Data	Bit 2 Primary FL_Code	Bit 1 Secondary Code	Bit 0 SRAM_Code
0 = disable PIO mode	not used	not used	0 = $\overline{RD}$ can't access Flash memory	0 = $\overline{RD}$ can't access Secondary Flash memory	0 = $\overline{PSEN}$ can't access Flash memory	0 = $\overline{PSEN}$ can't access Secondary Flash memory	0 = $\overline{PSEN}$ can't access SRAM
1= enable PIO mode	not used	not used	1 = $\overline{RD}$ access Flash memory	1 = $\overline{RD}$ access Secondary Flash memory	1 = $\overline{PSEN}$ access Flash memory	1 = $\overline{PSEN}$ access Secondary Flash memory	1 = $\overline{PSEN}$ access SRAM

22.10.3 Separate Space mode

Program space is separated from Data space. For example, Program Select Enable ($\overline{PSEN}$) is used to access the program code from the primary Flash memory, while READ Strobe ($\overline{RD}$) is used to access data from the secondary Flash memory, SRAM and I/O Port blocks. This configuration requires the VM Register to be set to 0Ch (see *Figure 54*).

22.10.4 Combined Space modes

The Program and Data spaces are combined into one memory space that allows the primary Flash memory, secondary Flash memory, and SRAM to be accessed by either Program Select Enable ($\overline{PSEN}$) or READ Strobe ($\overline{RD}$). For example, to configure the primary Flash memory in Combined space, Bits b2 and b4 of the VM Register are set to '1' (see *Figure 55*).

flop. The flip-flop is clocked on the rising edge of CLKIN (PD1). The preset and clear are active High inputs. Each clear input can use up to two product terms.

Table 92. Output macrocell port and data bit assignments

Output Macrocell	Port Assignment (1,2)	Native Product Terms	Max. Borrowed Product Terms	Data Bit for Loading or Reading
McellAB0	Port A0, B0	3	6	D0
McellAB1	Port A1, B1	3	6	D1
McellAB2	Port A2, B2	3	6	D2
McellAB3	Port A3, B3	3	6	D3
McellAB4	Port A4, B4	3	6	D4
McellAB5	Port A5, B5	3	6	D5
McellAB6	Port A6, B6	3	6	D6
McellAB7	Port A7, B7	3	6	D7
McellBC0	Port B0	4	5	D0
McellBC1	Port B1	4	5	D1
McellBC2	Port B2, C2	4	5	D2
McellBC3	Port B3, C3	4	5	D3
McellBC4	Port B4, C4	4	6	D4
McellBC5	Port B5	4	6	D5
McellBC6	Port B6	4	6	D6
McellBC7	Port B7, C7	4	6	D7

1. McellAB0-McellAB7 can only be assigned to Port B in the 52-pin package
2. Port PC0, PC1, PC5, and PC6 are assigned to JTAG pins and are not available as Macrocell outputs.

23.5 Product term allocator

The CPLD has a Product Term Allocator. PSDsoft uses the Product Term Allocator to borrow and place product terms from one macrocell to another. The following list summarizes how product terms are allocated:

- McellAB0-McellAB7 all have three native product terms and may borrow up to six more
- McellBC0-McellBC3 all have four native product terms and may borrow up to five more
- McellBC4-McellBC7 all have four native product terms and may borrow up to six more.

Each macrocell may only borrow product terms from certain other macrocells. Product terms already in use by one macrocell are not available for another macrocell.

If an equation requires more product terms than are available to it, then “external” product terms are required, which consume other Output Macrocells (OMC). If external product terms are used, extra delay is added for the equation that required the extra product terms.

This is called product term expansion. PSDsoft Express performs this expansion as needed.

are not set, writing to the macrocell loads data to the macrocell flip-flops. See *Section 23: PLDs*.

24.9.4 OMC mask register

Each OMC Mask Register Bit corresponds to an Output Macrocell (OMC) flip-flop. When the OMC Mask Register Bit is set to a '1,' loading data into the Output Macrocell (OMC) flip-flop is blocked. The default value is '0' or unblocked.

24.9.5 Input macrocells (IMC)

The Input Macrocells (IMC) can be used to latch or store external inputs. The outputs of the Input Macrocells (IMC) are routed to the PLD input bus, and can be read by the MCU. See *Section 23: PLDs*.

24.9.6 Enable out

The Enable Out register can be read by the MCU. It contains the output enable values for a given port. A '1' indicates the driver is in output mode. A '0' indicates the driver is in tri-state and the pin is in input mode.

Table 100. Drive register pin assignment

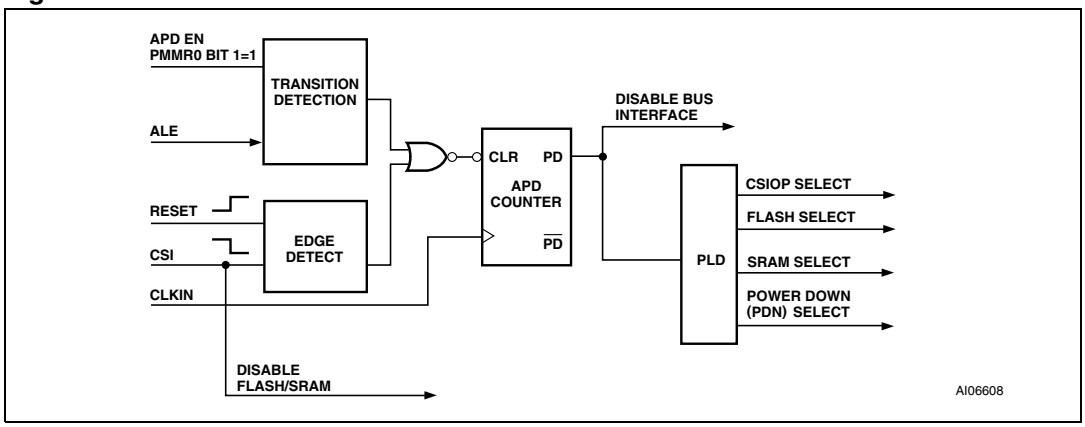
Drive Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port C	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain
Port D	NA(1)	NA(1)	NA(1)	NA(1)	NA(1)	Slew Rate	Slew Rate	NA(1)

1. NA = Not Applicable.

Table 101. Port data registers

Register Name	Port	MCU Access
Data In	A,B,C,D	READ – input on pin
Data Out	A,B,C,D	WRITE/READ
Output Macrocell	A,B,C	READ – outputs of macrocells WRITE – loading macrocells flip-flop
Mask Macrocell	A,B,C	WRITE/READ – prevents loading into a given macrocell
Input Macrocell	A,B,C	READ – outputs of the Input Macrocells
Enable Out	A,B,C	READ – the output enable control of the port driver

Figure 67. APD unit



The PSD module has a Turbo Bit in PMMR0. This bit can be set to turn the Turbo mode off (the default is with Turbo mode turned on). While Turbo mode is off, the PLDs can achieve standby current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo mode is on. When the Turbo mode is on, there is a significant DC current component and the AC component is higher.

Automatic Power-down (APD) Unit and Power-down mode

The APD Unit, shown in *Figure 67*, puts the PSD module into Power-down mode by monitoring the activity of Address Strobe (ALE). If the APD Unit is enabled, as soon as activity on Address Strobe (ALE) stops, a four-bit counter starts counting. If Address Strobe (ALE/AS, PD0) remains inactive for fifteen clock periods of CLKIN (PD1), Power-down (PDN) goes High, and the PSD module enters Power-down mode, as discussed next.

Power-down mode

By default, if you enable the APD Unit, Power-down mode is automatically enabled. The device enters Power-down mode if Address Strobe (ALE) remains inactive for fifteen periods of CLKIN (PD1).

The following should be kept in mind when the PSD module is in Power-down mode:

- If Address Strobe (ALE) starts pulsing again, the PSD module returns to normal Operating mode. The PSD module also returns to normal Operating mode if either PSD Chip Select Input ($\overline{\text{CSI}}$, PD2) is Low or the $\overline{\text{RESET}}$ input is High.
- The MCU address/data bus is blocked from all memory and PLDs.
- Various signals can be blocked (prior to Power-down mode) from entering the PLDs by setting the appropriate bits in the PMMR registers. The blocked signals include MCU control signals and the common CLKIN (PD1).

Note: Blocking CLKIN (PD1) from the PLDs does not block CLKIN (PD1) from the APD Unit.

- All memories enter Standby mode and are drawing standby current. However, the PLD and I/O ports blocks do *not* go into Standby mode because you don't want to have to wait for the logic and I/O to "wake-up" before their outputs can change. See *Table 102* for Power-down mode effects on PSD module ports.
- Typical standby current is of the order of microamperes. These standby current values assume that there are no transitions on any PLD input.

Table 121. External program memory AC characteristics (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{LHLL}	ALE pulse width	43		$2\ t_{CLCL} - 40$		ns
t_{AVLL}	Address set-up to ALE	17		$t_{CLCL} - 25$		ns
t_{LLAX}	Address hold after ALE	17		$t_{CLCL} - 25$		ns
t_{LLIV}	ALE Low to valid instruction in		80		$4\ t_{CLCL} - 87$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	22		$t_{CLCL} - 20$		ns
t_{PLPH}	$\overline{PSEN}$ pulse width	95		$3\ t_{CLCL} - 30$		ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in		60		$3\ t_{CLCL} - 65$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}[2]	Input instruction float after $\overline{PSEN}$		32		$t_{CLCL} - 10$	ns
t_{PXAV}[2]	Address valid after $\overline{PSEN}$	37		$t_{CLCL} - 5$		ns
t_{AVIV}	Address to valid instruction in		148		$5\ t_{CLCL} - 60$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	–10		–10		ns

1. Conditions (in addition to those in *Table 114*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)
2. Interfacing the UPSD323xx devices to devices with float times up to 35 ns is permissible. This limited bus contention does not cause any damage to Port 0 drivers.

Table 122. External clock drive (with the 5 V MCU module)

Symbol	Parameter[1]	40 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 24 to 40 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	Oscillator period			25	41.7	ns
t_{WLWH}	High time			10	$t_{CLCL} - t_{CLCX}$	ns
t_{LLAX2}	Low time			10	$t_{CLCL} - t_{CLCX}$	ns
t_{RHDX}	Rise time				10	ns
t_{RHDX}	Fall time				10	ns

1. Conditions (in addition to those in *Table 113*, V_{CC} = 4.5 to 5.5 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF; C_L for other outputs is 80 pF

Figure 76. Input to output disable / enable

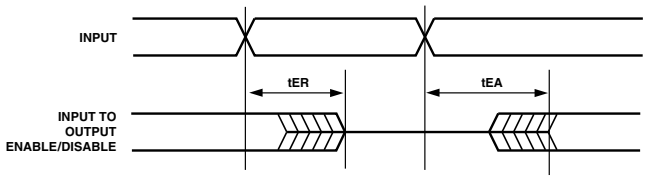


Table 127. CPLD combinatorial timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			20	+ 2	+ 10	– 2	ns
t_{EA}	CPLD input to CPLD output enable			21		+ 10	– 2	ns
t_{ER}	CPLD input to CPLD output disable			21		+ 10	– 2	ns
t_{ARP}	CPLD register clear or preset delay			21		+ 10	– 2	ns
t_{ARPW}	CPLD register clear or preset pulse width		10			+ 10		ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Table 128. CPLD combinatorial timing (3 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			40	+ 4	+ 20	– 6	ns
t_{EA}	CPLD input to CPLD output enable			43		+ 20	– 6	ns
t_{ER}	CPLD input to CPLD output disable			43		+ 20	– 6	ns
t_{ARP}	CPLD register clear or preset delay			40		+ 20	– 6	ns
t_{ARPW}	CPLD register clear or preset pulse width		25			+ 20		ns
t_{ARD}	CPLD array delay	Any macrocell		25	+ 4			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Figure 77. Synchronous clock mode timing – PLD

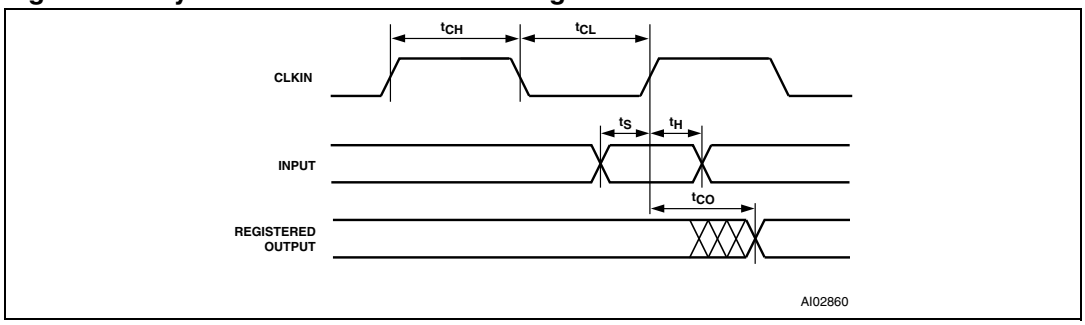


Table 129. CPLD macrocell synchronous clock mode timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT Aloc	Turbo Off	Slew rate(1)	Unit
f_{MAX}	Maximum frequency external feedback	$1/(t_S+t_{CO})$		40.0				MHz
	Maximum frequency internal feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		66.6				MHz
	Maximum frequency pipelined data	$1/(t_{CH}+t_{CL})$		83.3				MHz
t_S	Input setup time		12		+ 2	+ 10		ns
t_H	Input hold time		0					ns
t_{CH}	Clock high time	Clock input	6					ns
t_{CL}	Clock low time	Clock input	6					ns
t_{CO}	Clock to output delay	Clock input		13			– 2	ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns
t_{MIN}	Minimum clock period (2)	$t_{CH}+t_{CL}$	12					ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount.
2. CLKIN (PD1) $t_{CLCL} = t_{CH} + t_{CL}$.

Table 135. Program, Write and Erase times (5 V devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Flash Program		8.5		s
	Flash Bulk Erase(1) (pre-programmed)		3	30	s
	Flash Bulk Erase (not pre-programmed)		5		s
t_{WHQV3}	Sector Erase (pre-programmed)		1	30	s
t_{WHQV2}	Sector Erase (not pre-programmed)		2.2		s
t_{WHQV1}	Byte Program		14	150	µs
	Program / Erase Cycles (per Sector)	100,000			cycles
t_{WHWLO}	Sector Erase Time-Out		100		µs
t_{Q7VQV}	DQ7 Valid to Output (DQ7-DQ0) Valid (Data Polling)(2)			30	ns

1. Programmed to all zero before erase.
2. The polling status, DQ7, is valid t_{Q7VQV} time units before the data byte, DQ0-DQ7, is valid for reading.

Table 136. Program, Write and Erase times (3 V devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Flash Program		8.5		s
	Flash Bulk Erase(1) (pre-programmed)		3	30	s
	Flash Bulk Erase (not pre-programmed)		5		s
t_{WHQV3}	Sector Erase (pre-programmed)		1	30	s
t_{WHQV2}	Sector Erase (not pre-programmed)		2.2		s
t_{WHQV1}	Byte Program		14	150	µs
	Program / Erase Cycles (per Sector)	100,000			cycles
t_{WHWLO}	Sector Erase Time-Out		100		µs
t_{Q7VQV}	DQ7 Valid to Output (DQ7-DQ0) Valid (Data Polling)(2)			30	ns

1. Programmed to all zero before erase.
2. The polling status, DQ7, is valid t_{Q7VQV} time units before the data byte, DQ0-DQ7, is valid for reading.

34 Part numbering

Table 148. Ordering information scheme

Example: UPSD 3 2 3 4 B V – 24 U 6 T

Device type

UPSD = Microcontroller PSD

Family

3 = 8032 core

PLD size

2 = 16 Macrocells

SRAM Size

3 = 8 Kbytes

Main Flash memory size

2 = 64 Kbytes

3 = 128 Kbytes

4 = 256 Kbytes

IP mix

A = USB, I^2C, PWM, DDC, ADC, (2) UARTs, Supervisor (Reset Out, Reset In, LVD, WD)

B = I^2C, PWM, DDC, ADC, (2) UARTs Supervisor (Reset Out, Reset In, LVD, WD)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V

V = V_{CC} = 3.0 to 3.6 V

Speed

–24 = 24 MHz

–40 = 40 MHz

Package

T = 52-pin LQFP

U = 80-pin LQFP

Temperature range

1 = 0 to 70°C

6 = –40 to 85°C

Shipping options

F = ECOPACK® Package, Tape & Reel Packing

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.