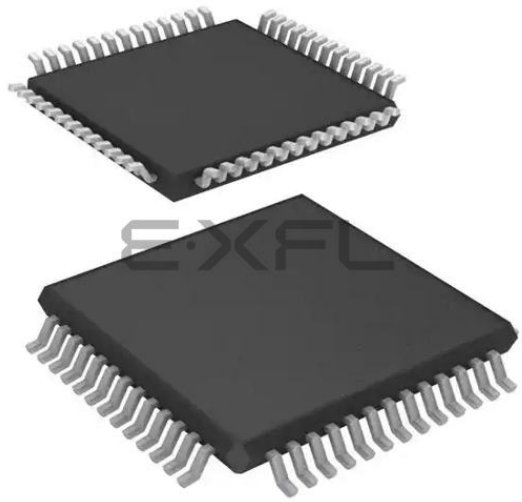


Welcome to E-XFL.COM

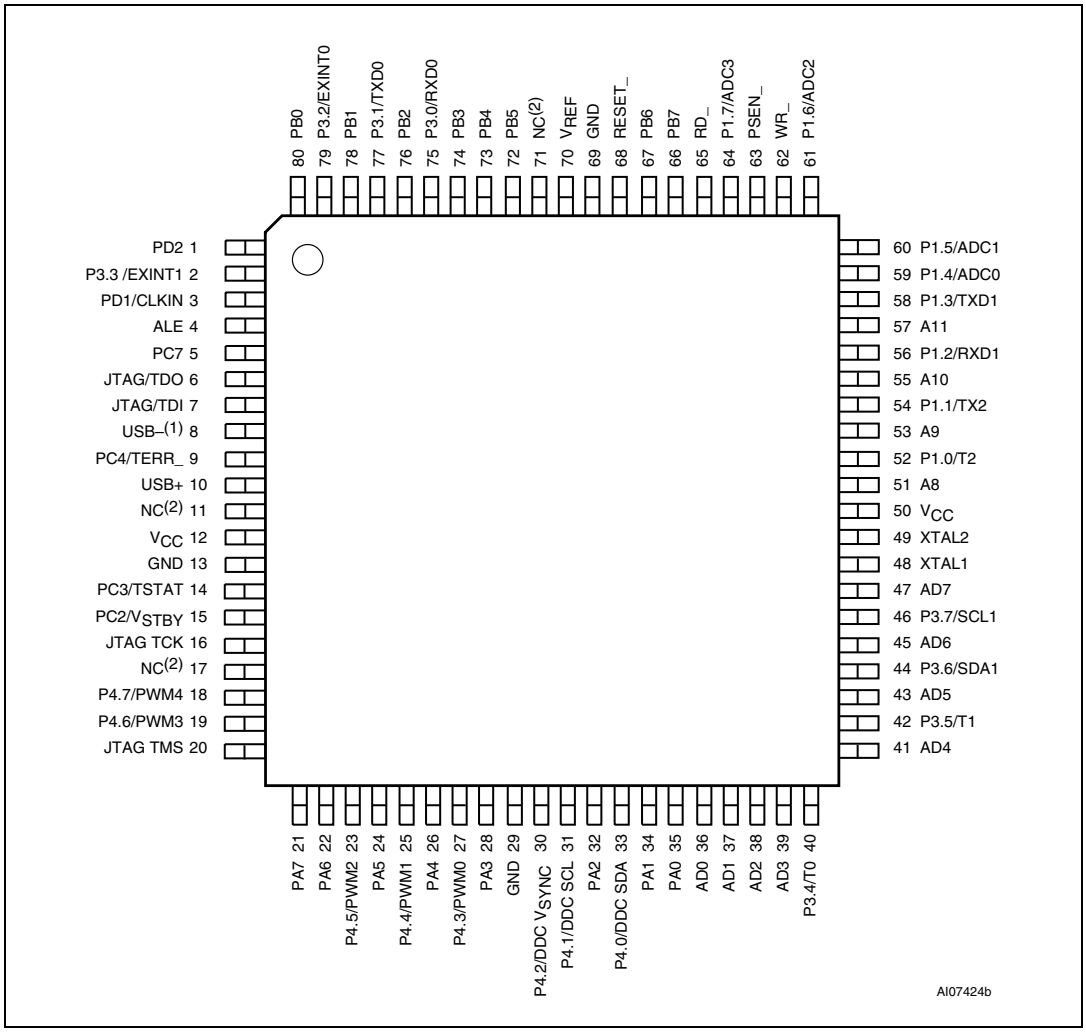
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, UART/USART
Peripherals	LVR, POR, PWM, WDT
Number of I/O	37
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3233bv-24t6

Figure 3. TQFP80 connections



1. Pull-up resistor required on pin 8 (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices) for all 82-pin devices, with or without USB function.
2. NC = Not Connected

Table 2. 80-pin package pin description

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
	AD0	36	I/O	External Bus: Multiplexed Address/Data bus A1/D1	
	AD1	37	I/O	Multiplexed Address/Data bus A0/D0	
	AD2	38	I/O	Multiplexed Address/Data bus A2/D2	
	AD3	39	I/O	Multiplexed Address/Data bus A3/D3	
	AD4	41	I/O	Multiplexed Address/Data bus A4/D4	
	AD5	43	I/O	Multiplexed Address/Data bus A5/D5	
	AD6	45	I/O	Multiplexed Address/Data bus A6/D6	

Table 2. 80-pin package pin description (continued)

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
	JTAG TMS	20	I	JTAG pin	PLD macrocell outputs PLD inputs JTAG pins are dedicated pins
	JTAG TCK	16	I	JTAG pin	
PC3	TSTAT	14	I/O	General I/O port pin	
PC4	TERR_	9	I/O	General I/O port pin	
	JTAG TDI	7	I	JTAG pin	
	JTAG TDO	6	O	JTAG pin	
PC7		5	I/O	General I/O port pin	
PD1	CLKIN	3	I/O	General I/O port pin	PLD I/O Clock input to PLD and APD
PD2		1	I/O	General I/O port pin	PLD I/O Chip select to PSD module
Vcc		12			
Vcc		50			
GND		13			
GND		29			
GND		69			
	USB+	10			
NC		11			
NC		17			
NC		71			

1.1 52-pin package I/O port

The 52-pin package members of the UPSD323xx devices have the same port pins as those of the 80-pin package except:

- Port 0 (P0.0-P0.7, external address/data bus AD0-AD7)
- Port 2 (P2.0-P2.3, external address bus A8-A11)
- Port A (PA0-PA7)
- Port D (PD2)
- Bus control signal (RD,WR,PSEN,ALE)
- Pin 5 requires a pull-up resistor (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices) for all devices, with or without USB function.

2.2.4 Program counter

The Program Counter is a 16-bit wide which consists of two 8-bit registers, PCH and PCL. This counter indicates the address of the next instruction to be executed. In $\overline{\text{RESET}}$ state, the program counter has reset routine address (PCH:00h, PCL:00h).

2.2.5 Program status word

The Program Status Word (PSW) contains several bits that reflect the current state of the CPU and select Internal RAM (00h to 1Fh: Bank0 to Bank3). The PSW is described in *Figure 8*. It contains the Carry flag, the Auxiliary Carry flag, the Half Carry (for BCD operation), the General Purpose flag, the Register Bank Select flags, the Overflow flag, and Parity flag.

[Carry flag, CY]. This flag stores any carry or not borrow from the ALU of CPU after an arithmetic operation and is also changed by the Shift Instruction or Rotate Instruction.

[Auxiliary Carry flag, AC]. After operation, this flag is set when there is a carry from Bit 3 of ALU or there is no borrow from Bit 4 of ALU.

[Register Bank Select flags, RS0, RS1]. These flags select one of four banks (00~07H:bank0, 08~0Fh:bank1, 10~17h:bank2, 17~1Fh:bank3) in Internal RAM.

[Overflow flag, OV]. This flag is set to '1' when an overflow occurs as the result of an arithmetic operation involving signs. An overflow occurs when the result of an addition or subtraction exceeds +127 (7Fh) or -128 (80h). The CLRV instruction clears the overflow flag. There is no set instruction. When the BIT instruction is executed, Bit 6 of memory is copied to this flag.

[Parity flag, P]. This flag reflects the number of Accumulator's 1. If the number of Accumulator's 1 is odd, P=0; otherwise, P=1. The sum when adding Accumulator's 1 to P is always even.

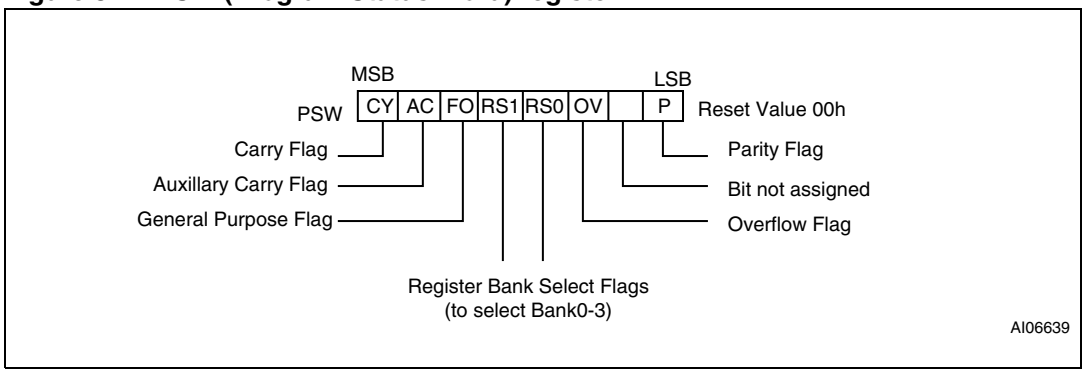
2.2.6 Registers R0~R7

General purpose 8-bit registers that are locked in the lower portion of internal data area.

2.2.7 Data pointer register

Data Pointer Register is 16-bit wide which consists of two-8bit registers, DPH and DPL. This register is used as a data pointer for the data transmission with external data memory in the PSD module.

Figure 8. PSW (Program Status Word) register



2.13 Boolean instructions

The UPSD323xx devices contain a complete Boolean (single-bit) processor. One page of the internal RAM contains 128 address-able bits, and the SFR space can support up to 128 addressable bits as well. All of the port lines are bit-addressable, and each one can be treated as a separate single-bit port. The instructions that access these bits are not just conditional branches, but a complete menu of move, set, clear, complement, OR and AND instructions. These kinds of bit operations are not easily obtained in other architectures with any amount of byte-oriented software.

The instruction set for the Boolean processor is shown in *Table 12*. All bits accesses are by direct addressing.

Bit addresses 00h through 7Fh are in the Lower 128, and bit addresses 80h through FFh are in SFR space.

Note how easily an internal flag can be moved to a port pin:

```
MOV C,FLAG
MOV P1.0,C
```

In this example, FLAG is the name of any addressable bit in the Lower 128 or SFR space. An I/O line (the LSB of Port 1, in this case) is set or cleared depending on whether the Flag bit is '1' or '0.'

The Carry Bit in the PSW is used as the single-bit Accumulator of the Boolean processor. Bit instructions that refer to the Carry Bit as C assemble as Carry-specific instructions (CLR C, etc.). The Carry Bit also has a direct address, since it resides in the PSW register, which is bit-addressable.

Note: The Boolean instruction set includes ANL and ORL operations, but not the XRL (Exclusive OR) operation. An XRL operation is simple to implement in software. Suppose, for example, it is required to form the Exclusive OR of two bits:

```
C = bit 1 .XRL. bit2
```

The software to do that could be as follows:

```
MOV C , bit1
JNB bit2, OVER
CPL C
OVER: (continue)
```

First, Bit 1 is moved to the Carry. If bit2 = 0, then C now contains the correct result. That is, Bit 1 .XRL. bit2 = bit1 if bit2 = 0. On the other hand, if bit2 = 1, C now contains the complement of the correct result. It need only be inverted (CPL C) to complete the operation.

This code uses the JNB instruction, one of a series of bit-test instructions which execute a jump if the addressed bit is set (JC, JB, JBC) or if the addressed bit is not set (JNC, JNB). In the above case, Bit 2 is being tested, and if bit2 = 0, the CPL C instruction is jumped over.

JBC executes the jump if the addressed bit is set, and also clears the bit. Thus a flag can be tested and cleared in one operation. All the PSW bits are directly addressable, so the Parity Bit, or the general-purpose flags, for example, are also available to the bit-test instructions.

5 Interrupt system

There are interrupt requests from 10 sources as follows.

- INT0 external interrupt
- 2nd USART interrupt
- Timer 0 interrupt
- I^2C interrupt
- INT1 external interrupt (or ADC interrupt)
- DDC interrupt
- Timer 1 interrupt
- USB interrupt
- USART interrupt
- Timer 2 interrupt

5.1 External Int0 interrupt

- The INT0 can be either level-active or transition-active depending on Bit IT0 in register TCON. The flag that actually generates this interrupt is Bit IE0 in TCON.
- When an external interrupt is generated, the corresponding request flag is cleared by the hardware when the service routine is vectored to only if the interrupt was transition activated.
- If the interrupt was level activated then the interrupt request flag remains set until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

5.2 Timer 0 and 1 interrupts

- Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1 which are set by an overflow of their respective Timer/Counter registers (except for Timer 0 in Mode 3).
- These flags are cleared by the internal hardware when the interrupt is serviced.

5.3 Timer 2 interrupt

- Timer 2 Interrupt is generated by TF2 which is set by an overflow of Timer 2. This flag has to be cleared by the software - not by hardware.
- It is also generated by the T2EX signal (Timer 2 External Interrupt P1.1) which is controlled by EXEN2 and EXF2 Bits in the T2CON register.

5.4 I^2C interrupt

- The interrupt of the I^2C is generated by Bit INTR in the register S2STA.
- This flag is cleared by hardware.

5.11 How interrupts are handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this H/W generated LCALL is not blocked by any of the following conditions:

- An interrupt of equal priority or higher priority level is already in progress.
- The current machine cycle is not the final cycle in the execution of the instruction in progress.
- The instruction in progress is RETI or any access to the interrupt priority or interrupt enable registers.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle.

Note: If an interrupt flag is active but being responded to for one of the above mentioned conditions, if the flag is still inactive when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate service routine. The hardware generated LCALL pushes the contents of the Program Counter on to the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to as shown in *Table 24*.

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note: A simple RET instruction would also return execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress, making future interrupts impossible.

Table 24. Vector addresses

Source	Vector address
Int0	0003h
2nd USART	004Bh
Timer 0	000Bh
I²C	0043h
Int1	0013h
DDC	003Bh
Timer 1	001Bh
USB	0033h
1st USART	0023h
Timer 2+EXF2	002Bh

9.3 Watchdog timer overflow

The Watchdog timer generates an internal reset when its 22-bit counter overflows. See Watchdog Timer section for details.

9.4 USB reset

The USB reset is generated by a detection on the USB bus $\overline{\text{RESET}}$ signal. A single-end zero on its upstream port for 4 to 8 times will set RSTF Bit in UISTA register. If Bit 6 (RSTE) of the UIEN Register is set, the detection will also generate the $\overline{\text{RESET}}$ signal to reset the CPU and other peripherals in the MCU.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the '1' that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “WRITE to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not '0,' the receive circuits are reset and the unit goes back to looking for an-other 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the reset of the rest of the frame will proceed.

As data bits come in from the right, '1s' shift out to the left. When the start bit arrives at the left-most position in the shift register (which in Mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

1. R1 = 0, and
2. Either SM2 = 0, or the received Stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the Stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

12.2.6 More about Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a Start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a Stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of '0' or '1.' On receive, the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figure 30 and *Figure 32* show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “WRITE to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next roll-over in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “WRITE to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a '1' (the Stop bit) into the 9th bit position of the shift register. There-after, only zeros are clocked in. Thus,

14 Pulse width modulation (PWM)

The PWM block has the following features:

- Four-channel, 8-bit PWM unit with 16-bit prescaler
- One-channel, 8-bit unit with programmable frequency and pulse width
- PWM Output with programmable polarity

14.1 4-channel PWM unit (PWM 0-3)

The 8-bit counter of a PWM counts module 256 (i.e., from 0 to 255, inclusive). The value held in the 8-bit counter is compared to the contents of the Special Function Register (PWM 0-3) of the corresponding PWM. The polarity of the PWM outputs is programmable and selected by the PWML Bit in PWMCON register. Provided the contents of a PWM 0-3 register is greater than the counter value, the corresponding PWM output is set HIGH (with PWML = 0). When the contents of this register is less than or equal to the counter value, the corresponding PWM output is set LOW (with PWML = 0). The pulse-width-ratio is therefore defined by the contents of the corresponding Special Function Register (PWM 0-3) of a PWM. By loading the corresponding Special Function Register (PWM 0-3) with either 00H or FFH, the PWM output can be retained at a constant HIGH or LOW level respectively (with PWML = 0).

For each PWM unit, there is a 16-bit Prescaler that are used to divide the main system clock to form the input clock for the corresponding PWM unit. This prescaler is used to define the desired repetition rate for the PWM unit. SFR registers B1h - B2h are used to hold the 16-bit divisor values.

The repetition frequency of the PWM output is given by:

$fPWM_8 = (f_{OSC} / prescaler0) / (2 \times 256)$

And the input clock frequency to the PWM counters is = $f_{OSC} / 2 /$ (prescaler data value + 1)

See *Section 7: I/O ports (MCU module)* for more information on how to configure the Port 4 pin as PWM output.

Table 54. Description of the SxSTA bits

Bit	Symbol	Function
7	GC	General Call Flag
6	STOP	Stop Flag. This bit is set when a STOP condition is received
5	INTR(1,2)	Interrupt Flag. This bit is set when an I²C Interrupt condition is requested
4	TX_MODE	Transmission mode Flag. This bit is set when the I²C is a transmitter; otherwise this bit is reset
3	BBUSY	Bus Busy Flag. This bit is set when the bus is being used by another master; otherwise, this bit is reset
2	BLOST	Bus Lost Flag. This bit is set when the master loses the bus contention; otherwise this bit is reset
1	/ACK_REP	Acknowledge Response Flag. This bit is set when the receiver transmits the not acknowledge signal This bit is reset when the receiver transmits the acknowledge signal
0	SLV	Slave mode Flag. This bit is set when the I²C plays role in the Slave mode; otherwise this bit is reset

1. Interrupt Flag bit (INTR, SxSTA Bit 5) is cleared by Hardware as reading SxSTA register.
2. I²C interrupt flag (INTR) can occur in below case. (except DDC2B mode at SWENB=0)

Table 55. Data shift register (SxDAT: S1DAT, S2DAT)

7	6	5	4	3	2	1	0
SxDAT7	SxDAT6	SxDAT5	SxDAT4	SxDAT3	SxDAT2	SxDAT1	SxDAT0

15.3 Address register (SxADR: S1ADR, S2ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receive/transmitter.

The Start/Stop Hold Time Detection and System Clock registers (*Table 57* and *Table 58*) are included in the I²C unit to specify the start/stop detection time to work with the large range of MCU frequency values supported. For example, with a system clock of 40MHz.

Table 56. Address register (SxADR)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	—

1. SLA6 to SLA0: Own slave address.

Table 57. Start /Stop Hold Time Detection Register (S1SETUP, S2SETUP)

	Address	Register Name	Reset Value	Note
SFR	D1h	S1SETUP	00h	To control the start/stop hold time detection for the DDC module in Slave mode
	D2h	S2SETUP	00h	To control the start/stop hold time detection for the multi-master I²C module in Slave mode

Table 58. System clock of 40MHz

S1SETUP, S2SETUP Register Value	Number of Sample Clock (f_{OSC}/2 -> 50ns)	Required Start/Stop Hold Time	Note
00h	1EA	50ns	When Bit 7 (enable bit) = 0, the number of sample clock is 1EA (ignore Bit 6 to Bit 0)
80h	1EA	50ns	
81h	2EA	100ns	
82h	3EA	150ns	
...	...	...	
8Bh	12EA	600ns	Fast mode I²C Start/Stop hold time specification
...	...	...	
FFh	128EA	6000ns	

Table 59. System clock setup examples

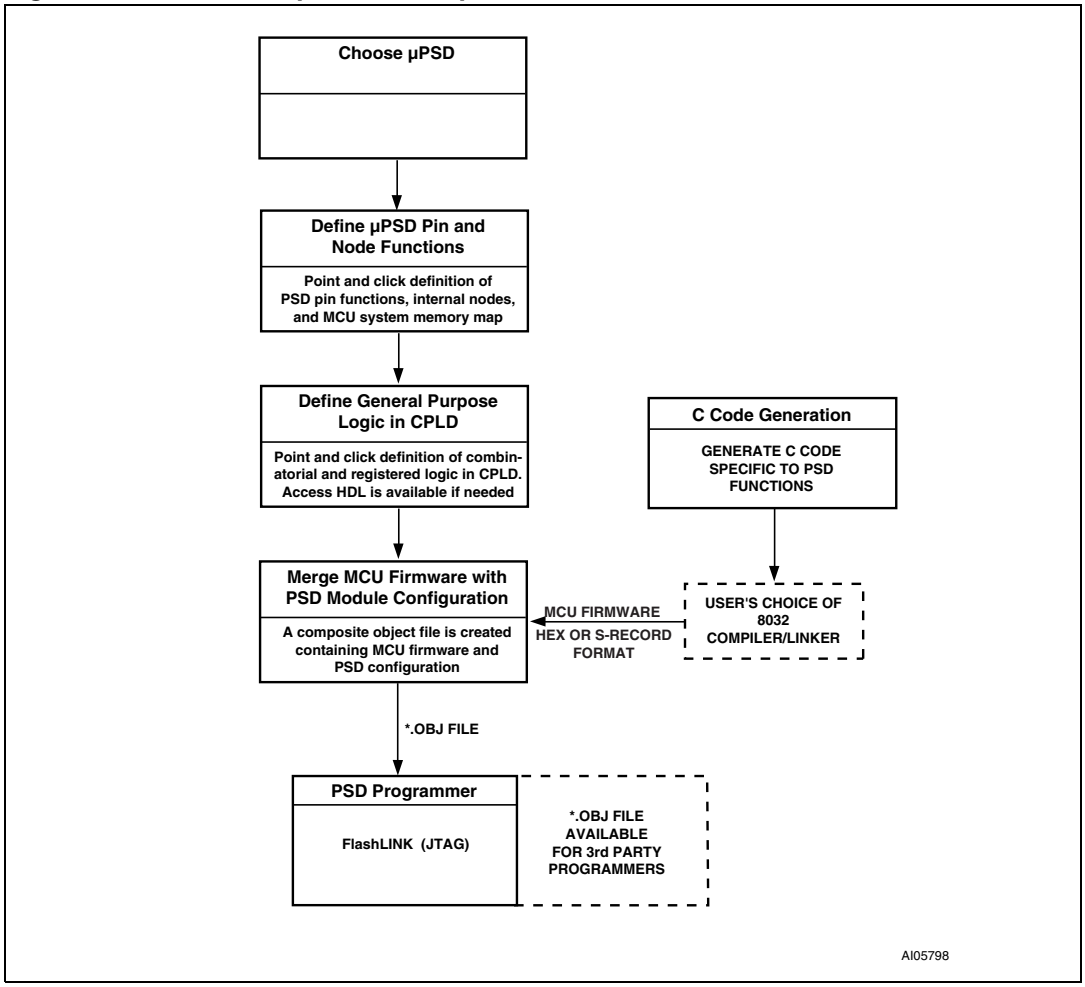
System Clock	S1SETUP, S2SETUP Register Value	Number of Sample Clock	Required Start/Stop Hold Time
40MHz (f_{OSC}/2 -> 50ns)	8Bh	12 EA	600ns
30MHz (f_{OSC}/2 -> 66.6ns)	89h	9 EA	600ns
20MHz (f_{OSC}/2 -> 100ns)	86h	6 EA	600ns
8MHz (f_{OSC}/2 -> 250ns)	83h	3 EA	750ns

19 Development system

UPSD323xx devices are supported by PSDsoft, a Windows-based software development tool (Windows-95, Windows-98, Windows-NT). A PSD module design is quickly and easily produced in a point and click environment. The designer does not need to enter Hardware Description Language (HDL) equations, unless desired, to define PSD module pin functions and memory map information. The general design flow is shown in *Figure 50*. PSDsoft is available from our web site (the address is given on the back page of this data sheet) or other distribution channels.

PSDsoft directly supports a low cost device programmer from ST: FlashLINK (JTAG). The programmer may be purchased through your local distributor/representative. UPSD323xx devices are also supported by third party device programmers. See our web site for the current list.

Figure 50. PSDsoft express development tool



21 PSD module detailed operation

As shown in *Figure 14*, the PSD module consists of five major types of functional blocks:

- Memory blocks
- PLD blocks
- I/O Ports
- Power Management Unit (PMU)
- JTAG Interface

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

22.5.7 Erase time-out flag (DQ3)

The Erase Time-out Flag bit (DQ3) reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase Time-out Flag bit (DQ3) is reset to '0' after a Sector Erase cycle for a time period of 100µs + 20% unless an additional Sector Erase instruction is decoded. After this time period, or when the additional Sector Erase instruction is decoded, the Erase Time-out Flag bit (DQ3) is set to ‘1’.

Table 86. Status bit

Functional Block	FS0-FS7/ CSBOOT0-CSBOOT3	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash Memory	V_{IH}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-out	X	X	X

1. X = Not guaranteed value, can be read either '1' or '0.'
2. DQ7-DQ0 represent the Data Bus bits, D7-D0.
3. FS0-FS7 and CSBOOT0-CSBOOT3 are active High.

22.6 Programming Flash memory

Flash memory must be erased prior to being programmed. A byte of Flash memory is erased to all '1's (FFh), and is programmed by setting selected bits to '0'. The MCU may erase Flash memory all at once or by-sector, but not byte-by-byte. However, the MCU may program Flash memory byte-by-byte.

The primary and secondary Flash memories require the MCU to send an instruction to program a byte or to erase sectors (see *Table 85*).

Once the MCU issues a Flash memory Program or Erase instruction, it must check for the status bits for completion. The embedded algorithms that are invoked support several means to provide status to the MCU. Status may be checked using any of three methods: Data Polling, Data Toggle, or Ready/$\overline{\text{Busy}}$ (PC3).

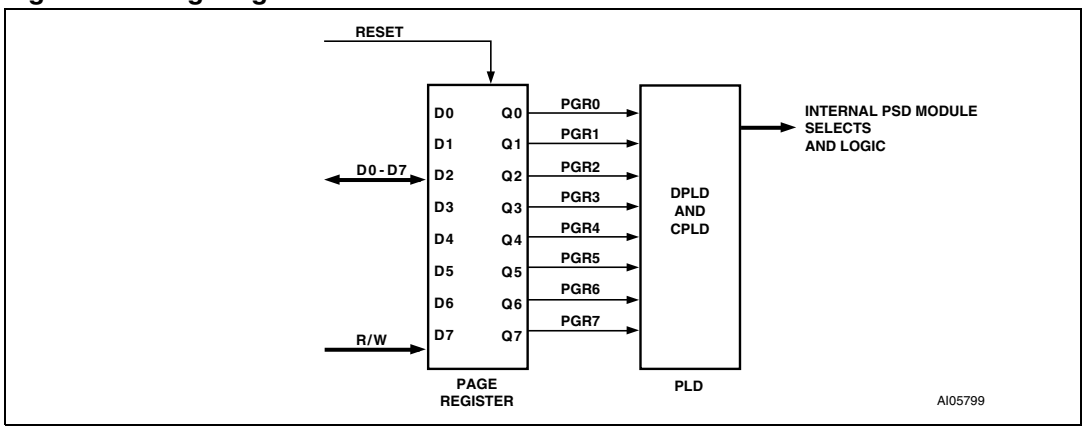
22.6.1 Data Polling

Polling on the Data Polling Flag bit (DQ7) is a method of checking whether a Program or Erase cycle is in progress or has completed. *Figure 51* shows the Data Polling algorithm.

When the MCU issues a Program instruction, the embedded algorithm begins. The MCU then reads the location of the byte to be programmed in Flash memory to check status. The Data Polling Flag bit (DQ7) of this location becomes the complement of b7 of the original data byte to be programmed. The MCU continues to poll this location, comparing the Data Polling Flag bit (DQ7) and monitoring the Error Flag bit (DQ5). When the Data Polling Flag bit (DQ7) matches b7 of the original data, and the Error Flag bit (DQ5) remains '0,' the embedded algorithm is complete. If the Error Flag bit (DQ5) is '1,' the MCU should test the Data Polling Flag bit (DQ7) again since the Data Polling Flag bit (DQ7) may have changed simultaneously with the Error Flag bit (DQ5) (see *Figure 51*).

The Error Flag bit (DQ5) is set if either an internal time-out occurred while the embedded algorithm attempted to program the byte or if the MCU attempted to program a '1' to a bit that was not erased (not erased is logic '0').

Figure 56. Page register



25.2 PSD chip select input ($\overline{CSI}$, PD2)

PD2 of Port D can be configured in PSDsoft Express as PSD Chip Select Input ($\overline{CSI}$). When Low, the signal selects and enables the PSD module Flash memory, SRAM, and I/O blocks for READ or WRITE operations. A High on PSD Chip Select Input ($\overline{CSI}$, PD2) disables the Flash memory, and SRAM, and reduces power consumption. However, the PLD and I/O signals remain operational when PSD Chip Select Input ($\overline{CSI}$, PD2) is High.

25.3 Input clock

CLKIN (PD1) can be turned off, to the PLD to save AC power consumption. CLKIN (PD1) is an input to the PLD AND Array and the Output Macrocells (OMC).

During Power-down mode, or, if CLKIN (PD1) is not being used as part of the PLD logic equation, the clock should be disabled to save AC power. CLKIN (PD1) is disconnected from the PLD AND Array or the Macrocells block by setting Bits 4 or 5 to a '1' in PMMR0.

25.4 Input control signals

The PSD module provides the option to turn off the MCU signals ($\overline{WR}$, $\overline{RD}$, $\overline{PSEN}$, and Address Strobe (ALE)) to the PLD to save AC power consumption. These control signals are inputs to the PLD AND Array. During Power-down mode, or, if any of them are not being used as part of the PLD logic equation, these control signals should be disabled to save AC power. They are disconnected from the PLD AND Array by setting Bits 2, 3, 4, 5, and 6 to a '1' in PMMR2.

Table 103. Power management mode registers (PMMR0)

Bit 0	X	0	Not used, and should be set to zero.
Bit 1	APD Enable	0 = off	Automatic Power-down (APD) is disabled.
		1 = on	Automatic Power-down (APD) is enabled.
Bit 2	X	0	Not used, and should be set to zero.
Bit 3	PLD Turbo	0 = on	PLD Turbo mode is on
		1 = off	PLD Turbo mode is off, saving power. UPSD323xx devices operate at 5MHz below the maximum rated clock frequency
Bit 4	PLD Array clk	0 = on	CLKIN (PD1) input to the PLD AND Array is connected. Every change of CLKIN (PD1) Powers-up the PLD when Turbo Bit is '0.'
		1 = off	CLKIN (PD1) input to PLD AND Array is disconnected, saving power.
Bit 5	PLD MCell clk	0 = on	CLKIN (PD1) input to the PLD macrocells is connected.
		1 = off	CLKIN (PD1) input to PLD macrocells is disconnected, saving power.
Bit 6	X	0	Not used, and should be set to zero.
Bit 7	X	0	Not used, and should be set to zero.

Table 118. DC characteristics (5 V devices)

Symbol	Parameter	Test conditions (in addition to those in *Table 113*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], XTAL1, $\overline{RESET}$)	4.5 V < V_{CC} < 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IH1}	Input high voltage (Ports A, B, C, D, 4[Bit 2], USB+, USB–)	4.5 V < V_{CC} < 5.5 V	2.0		V_{CC} + 0.5	V
V_{IL}	Input low voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], XTAL1, $\overline{RESET}$)	4.5 V < V_{CC} < 5.5 V	V_{SS}– 0.5		0.3 V_{CC}	V
V_{IL1}	Input low voltage (Ports A, B, C, D, 4[Bit 2])	4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
	Input low voltage (USB+, USB–)	4.5 V < V_{CC} < 5.5 V	V_{SS}– 0.5		0.8	V
V_{OL}	Output low voltage (Ports A,B,C,D)	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.25	0.45	V
V_{OL1}	Output low voltage (Ports 1,2,3,4, $\overline{WR}$, $\overline{RD}$)	I_{OL} = 1.6 mA			0.45	V
V_{OL2}	Output low voltage (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA			0.45	V
V_{OH}	Output high voltage (Ports A,B,C,D)	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		V
V_{OH2}	Output high voltage (Port 0 in ext. Bus mode, ALE, PSEN)	I_{OH} = –800 µA	2.4			V
		I_{OH} = –80 µA	4.05			V
V_{LVR}	Low Voltage $\overline{RESET}$	0.1 V hysteresis	3.75	4.0	4.25	V
V_{OP}	XTAL open bias voltage (XTAL1, XTAL2)	I_{OL} = 3.2 mA	2.0		3.0	V
V_{LKO}	V_{CC}(min) for Flash Erase and Program		2.5		4.2	V
I_{IL}	Logic '0' input current (Ports 1,2,3,4)	V_{IN} = 0.45 V (0 V for Port 4[pin 2])	–10		–50	µA
I_{TL}	Logic 1-to-0 transition current (Ports 1,2,3,4)	V_{IN} = 3.5 V (2.5 V for Port 4[pin 2])	–65		–650	µA
I_{RST}	Reset pin pull-up current ($\overline{RESET}$)	V_{IN} = V_{SS}	–10		–55	µA

Table 125. External data memory AC characteristics (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{WLWH}	$\overline{WR}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{LLAX2}	Address hold after ALE	56		2 t_{CLCL} – 27		ns
t_{RHDX}	$\overline{RD}$ to valid data in		118		5 t_{CLCL} – 90	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		63		2 t_{CLCL} – 20	ns
t_{LLDV}	ALE to valid data in		200		8 t_{CLCL} – 133	ns
t_{AVDV}	Address to valid data in		220		9 t_{CLCL} – 155	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	75	175	3 t_{CLCL} – 50	t_{CLCL} + 50	ns
t_{AVWL}	Address valid to $\overline{WR}$ or $\overline{RD}$	67		4 t_{CLCL} – 97		ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	17	67	t_{CLCL} – 25	t_{CLCL} + 25	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5		t_{CLCL} – 37		ns
t_{QVWH}	Data set-up before $\overline{WR}$	170		7 t_{CLCL} – 122		ns
t_{WHQX}	Data hold after $\overline{WR}$	15		t_{CLCL} – 27		ns
t_{RLAZ}	Address float after $\overline{RD}$		0		0	ns

1. Conditions (in addition to those in *Table 114*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)

Table 126. A/D analog specification

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
AV_{REF}	Analog power supply input voltage range		V_{SS}		V_{CC}	V
V_{AN}	Analog input voltage range		V_{SS} – 0.3		AV_{REF} + 0.3	V
I_{AVDD}	Current following between V_{CC} and V_{SS}				200	µA
CA_{IN}	Overall accuracy				±2	l.s.b.
N_{NLE}	Non-linearity error				±2	l.s.b.
N_{DNLE}	Differential non-linearity error				±2	l.s.b.
N_{ZOE}	Zero-offset error				±2	l.s.b.
N_{FSE}	Full scale error				±2	l.s.b.
N_{GE}	Gain error				±2	l.s.b.
t_{CONV}	Conversion time	at 8 MHz clock			20	µs

Figure 77. Synchronous clock mode timing – PLD

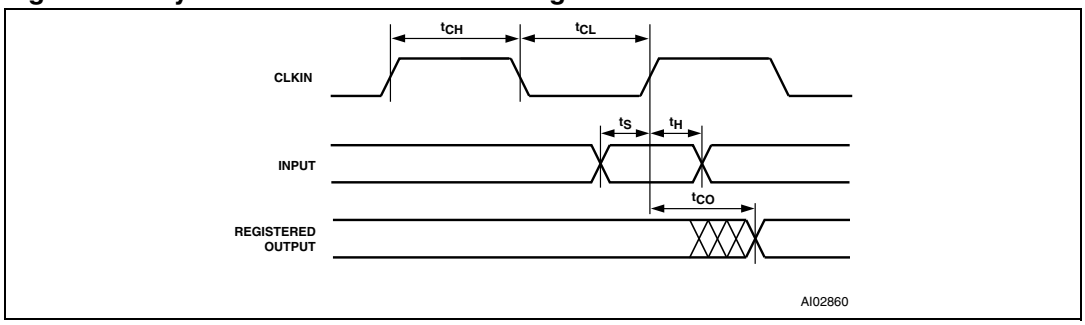
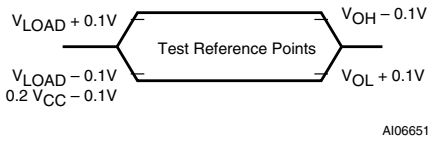


Table 129. CPLD macrocell synchronous clock mode timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT Aloc	Turbo Off	Slew rate(1)	Unit
f_{MAX}	Maximum frequency external feedback	$1/(t_S+t_{CO})$		40.0				MHz
	Maximum frequency internal feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		66.6				MHz
	Maximum frequency pipelined data	$1/(t_{CH}+t_{CL})$		83.3				MHz
t_S	Input setup time		12		+ 2	+ 10		ns
t_H	Input hold time		0					ns
t_{CH}	Clock high time	Clock input	6					ns
t_{CL}	Clock low time	Clock input	6					ns
t_{CO}	Clock to output delay	Clock input		13			– 2	ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns
t_{MIN}	Minimum clock period (2)	$t_{CH}+t_{CL}$	12					ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount.
2. CLKIN (PD1) $t_{CLCL} = t_{CH} + t_{CL}$.

Figure 86. PSD module AC float I/O waveform



1. For timing purposes, a Port pin is considered to be no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH} or V_{OL} level occurs
2. I_{OL} and $I_{OH} \geq 20mA$

Figure 87. External clock cycle

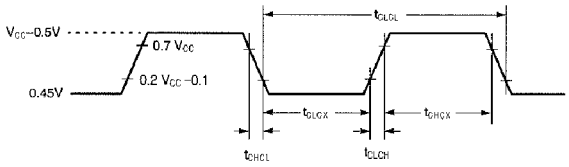
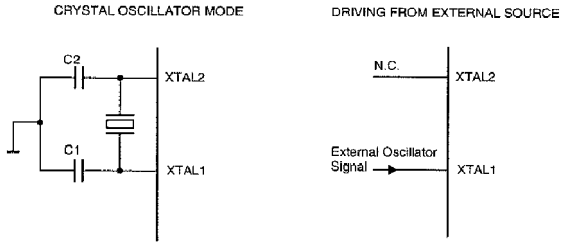


Figure 88. Recommended oscillator circuits



1. C1, C2 = 30 pF ± 10 pF for crystals
2. For ceramic resonators, contact resonator manufacturer
3. Oscillation circuit is designed to be used either with a ceramic resonator or crystal oscillator. Since each crystal and ceramic resonator
4. have their own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Figure 89. PSD module AC measurement I/O waveform