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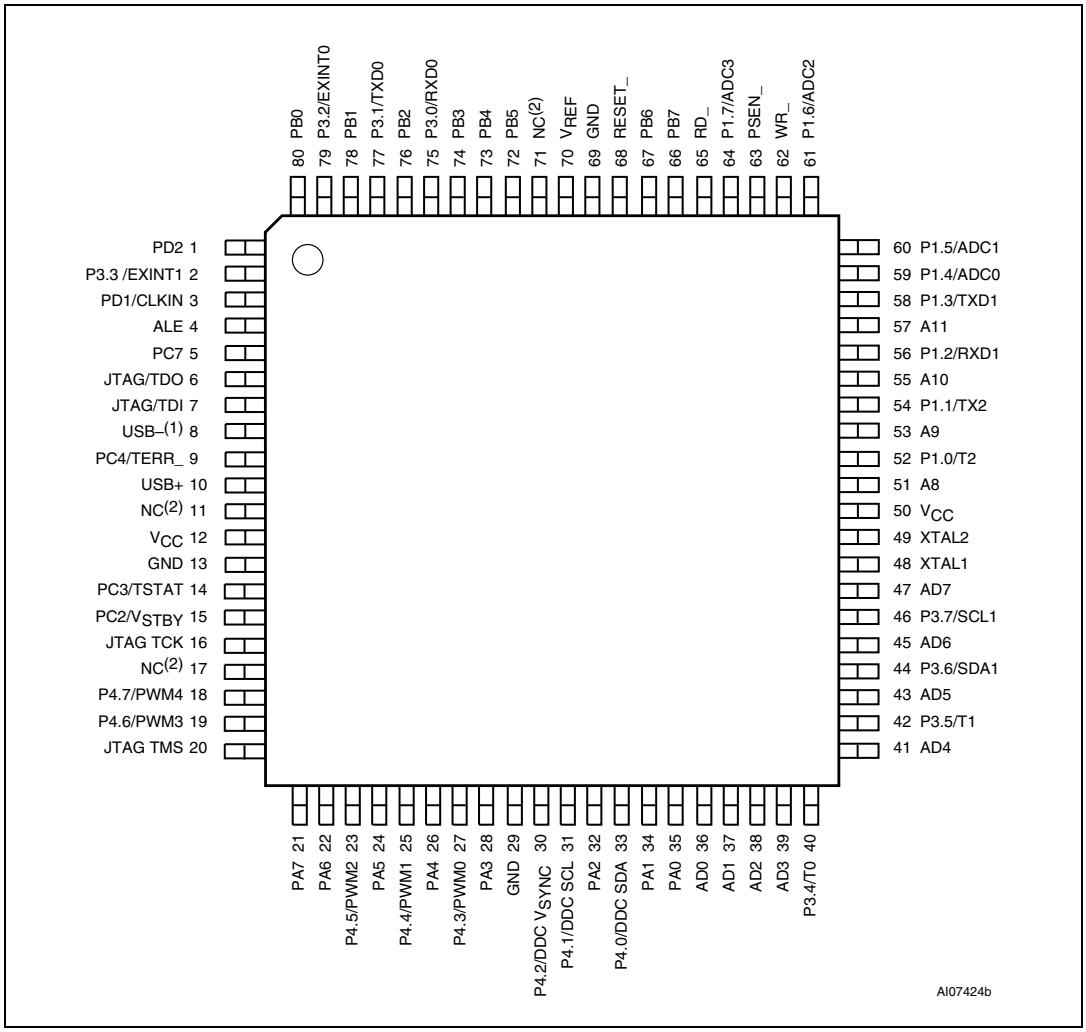
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, UART/USART
Peripherals	LVR, POR, PWM, WDT
Number of I/O	46
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3233bv-24u6

Figure 3. TQFP80 connections



1. Pull-up resistor required on pin 8 (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices) for all 82-pin devices, with or without USB function.
2. NC = Not Connected

Table 2. 80-pin package pin description

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
	AD0	36	I/O	External Bus: Multiplexed Address/Data bus A1/D1	
	AD1	37	I/O	Multiplexed Address/Data bus A0/D0	
	AD2	38	I/O	Multiplexed Address/Data bus A2/D2	
	AD3	39	I/O	Multiplexed Address/Data bus A3/D3	
	AD4	41	I/O	Multiplexed Address/Data bus A4/D4	
	AD5	43	I/O	Multiplexed Address/Data bus A5/D5	
	AD6	45	I/O	Multiplexed Address/Data bus A6/D6	

Table 2. 80-pin package pin description (continued)

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
	JTAG TMS	20	I	JTAG pin	PLD macrocell outputs PLD inputs JTAG pins are dedicated pins
	JTAG TCK	16	I	JTAG pin	
PC3	TSTAT	14	I/O	General I/O port pin	
PC4	TERR_	9	I/O	General I/O port pin	
	JTAG TDI	7	I	JTAG pin	
	JTAG TDO	6	O	JTAG pin	
PC7		5	I/O	General I/O port pin	
PD1	CLKIN	3	I/O	General I/O port pin	PLD I/O Clock input to PLD and APD
PD2		1	I/O	General I/O port pin	PLD I/O Chip select to PSD module
Vcc		12			
Vcc		50			
GND		13			
GND		29			
GND		69			
	USB+	10			
NC		11			
NC		17			
NC		71			

1.1 52-pin package I/O port

The 52-pin package members of the UPSD323xx devices have the same port pins as those of the 80-pin package except:

- Port 0 (P0.0-P0.7, external address/data bus AD0-AD7)
- Port 2 (P2.0-P2.3, external address bus A8-A11)
- Port A (PA0-PA7)
- Port D (PD2)
- Bus control signal (RD,WR,PSEN,ALE)
- Pin 5 requires a pull-up resistor (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices) for all devices, with or without USB function.

2 Architecture overview

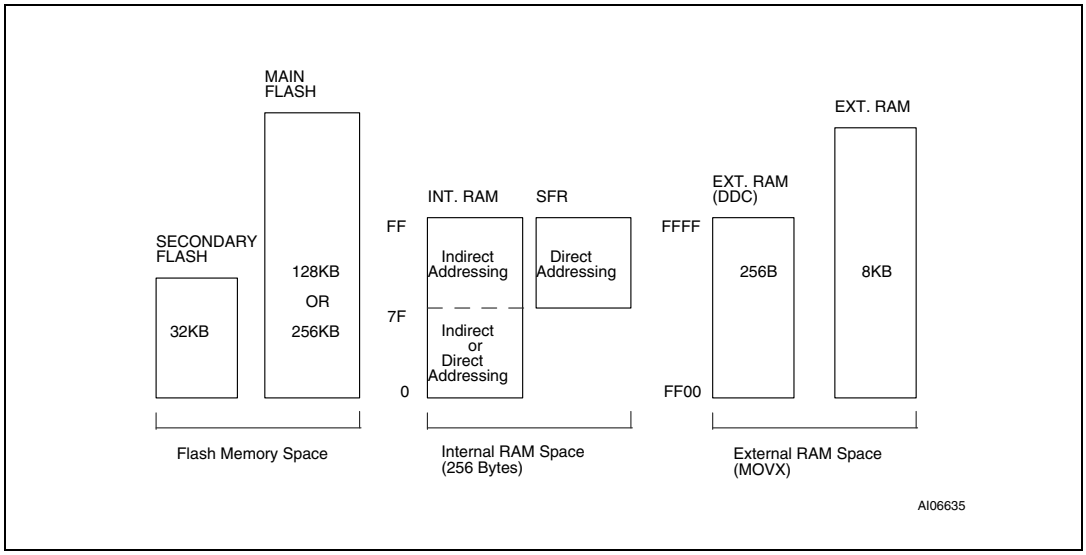
2.1 Memory organization

The UPSD323xx devices' standard 8032 Core has separate 64-Kbyte address spaces for Program memory and Data Memory. Program memory is where the 8032 executes instructions from. Data memory is used to hold data variables. Flash memory can be mapped in either program or data space. The Flash memory consists of two Flash memory blocks: the main Flash memory (1 or 2 Mbit) and the Secondary Flash memory (256 Kbit). Except during flash memory programming or update, Flash memory can only be read, not written to. A Page Register is used to access memory beyond the 64-Kbyte address space. Refer to the PSD module for details on mapping of the Flash memory.

The 8032 core has two types of data memory (internal and external) that can be read and written. The internal SRAM consists of 256 bytes, and includes the stack area.

The SFR (Special Function Registers) occupies the upper 128 bytes of the internal SRAM, the registers can be accessed by Direct addressing only. There are two separate blocks of external SRAM inside the UPSD325X devices: one 256-byte block is assigned for DDC data storage. Another 8 Kbytes resides in the PSD module that can be mapped to any address space defined by the user.

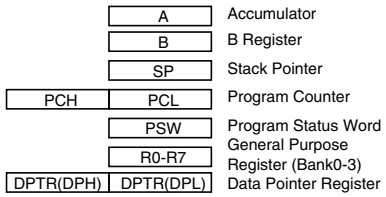
Figure 4. Memory map and address space



2.2 Registers

The 8032 has several registers; these are the Program Counter (PC), Accumulator (A), B Register (B), the Stack Pointer (SP), the Program Status Word (PSW), General purpose registers (R0 to R7), and DPTR (Data Pointer register).

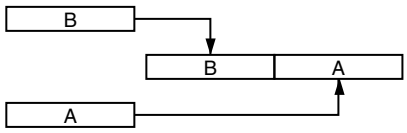
Figure 5. 8032 MCU registers



2.2.1 Accumulator

The Accumulator is the 8-bit general purpose register, used for data operation such as transfer, temporary saving, and conditional tests. The Accumulator can be used as a 16-bit register with B Register as shown below.

Figure 6. Configuration of BA 16-bit registers



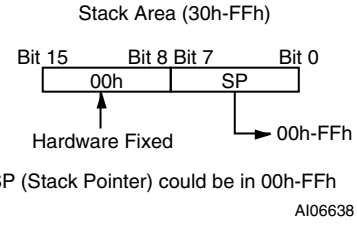
2.2.2 B register

The B Register is the 8-bit general purpose register, used for an arithmetic operation such as multiply, division with Accumulator.

2.2.3 Stack pointer

The Stack Pointer Register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07h after reset. This causes the stack to begin at location 08h.

Figure 7. Stack pointer



4 MCU module description

This section provides a detail description of the MCU module system functions and Peripherals, including:

- Special function registers
- Timers/counter
- Interrupts
- PWM
- Supervisory function (LVD and Watchdog)
- USART
- Power-saving modes
- I^2C Bus
- On-chip oscillator
- ADC
- I/O Ports
- USB

4.1 Special function registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in *Table 15*.

Note: In the SFRs not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. READ accesses to these addresses will in general return random data, and WRITE accesses will have no effect. User software should write '0s' to these unimplemented locations.

Table 15. SFR memory map

F8									FF
F0	B(1)								F7
E8	UISTA(1)	UIEN	UCON0	UCON1	UCON2	USTA	UADR	UDR0	EF
E0	ACC(1)	USCL					UDT1	UDT0	E7
D8	S1CON(1)	S1STA	S1DAT	S1ADR	S2CON	S2STA	S2DAT	S2ADR	DF
D0	PSW(1)	S1SETUP	S2SETUP		RAMBUF	DDCDAT	DDCADR	DDCCON	D7
C8	T2CON(1)	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CF
C0	P4(1)								C7
B8	IP(1)								BF
B0	P3(1)	PSCL0L	PSCL0H	PSCL1L	PSCL1H			IPA	B7
A8	IE(1)		PWM4P	PWM4W			WDKEY		AF
A0	P2(1)	PWMCON	PWM0	PWM1	PWM2	PWM3	WDRST	IEA	A7
98	SCON	SBUF	SCON2	SBUF2					9F
90	P1(1)	P1SFS		P3SFS	P4SFS	ASCL	ADAT	ACON	97

Table 17. PSD module register address offset (continued)

CSIOP addr offset	Register name	Bit register name								Reset value	Comments
		7	6	5	4	3	2	1	0		
01	Data In (Port B)										
03	Control (Port B)									00	
05	Data Out (Port B)									00	
07	Direction (Port B)									00	
09	Drive (Port B)									00	
0B	Input Macrocell (Port B)										
0D	Enable Out (Port B)										
10	Data In (Port C)										
12	Data Out (Port C)									00	
14	Direction (Port C)									00	
16	Drive (Port C)									00	
18	Input Macrocell (Port C)										
1A	Enable Out (Port C)										
11	Data In (Port D)	*	*	*	*	*		*			Only Bit 1 and 2 are used
13	Data Out (Port D)	*	*	*	*	*		*		00	Only Bit 1 and 2 are used
15	Direction (Port D)	*	*	*	*	*		*		00	Only Bit 1 and 2 are used
17	Drive (Port D)	*	*	*	*	*		*		00	Only Bit 1 and 2 are used
1B	Enable Out (Port D)	*	*	*	*	*		*			Only Bit 1 and 2 are used
20	Output Macrocells AB										
21	Output Macrocells BC										
22	Mask Macrocells AB										
23	Mask Macrocells BC										

Table 21. Description of the IEA bits

Bit	Symbol	Function
7	EDDC	Enable DDC Interrupt
6	—	Not used
5	—	Not used
4	ES2	Enable 2nd USART Interrupt
3	—	Not used
2	—	Not used
1	EI2C	Enable I²C Interrupt
0	EUSB	Enable USB Interrupt

Table 22. Description of the IP bits

Bit	Symbol	Function
7	—	Reserved
6	—	Reserved
5	PT2	Timer 2 Interrupt priority level
4	PS	USART Interrupt priority level
3	PT1	Timer 1 Interrupt priority level
2	PX1	External Interrupt (Int1) priority level
1	PT0	Timer 0 Interrupt priority level
0	PX0	External Interrupt (Int0) priority level

Table 23. Description of the IPA bits

Bit	Symbol	Function
7	PDDC	DDC Interrupt priority level
6	—	Not used
5	—	Not used
4	PS2	2nd USART Interrupt priority level
3	—	Not used
2	—	Not used
1	PI2C	I²C Interrupt priority level
0	PUSB	USB Interrupt priority level

9 Supervisory

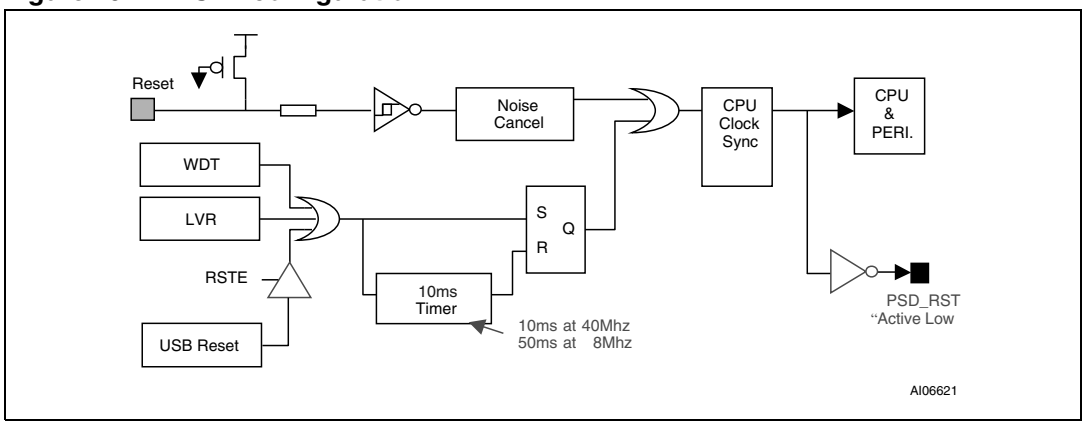
There are four ways to invoke a reset and initialize the UPSD323xx devices.

1. Via the external $\overline{\text{RESET}}$ pin
2. Via the internal LVR block
3. Via USB bus reset signaling
4. Via Watchdog Timer (WDT)

The $\overline{\text{RESET}}$ mechanism is illustrated in *Figure 19*.

Each $\overline{\text{RESET}}$ source will cause an internal reset signal active. The CPU responds by executing an internal reset and puts the internal registers in a defined state. This internal reset is also routed as an active low reset input to the PSD module.

Figure 19. $\overline{\text{RESET}}$ configuration



9.1 External reset

The $\overline{\text{RESET}}$ pin is connected to a Schmitt trigger for noise reduction. A $\overline{\text{RESET}}$ is accomplished by holding the $\overline{\text{RESET}}$ pin LOW for at least 1ms at power up while the oscillator is running. Refer to AC spec on other $\overline{\text{RESET}}$ timing requirements.

9.2 Low V_{DD} voltage reset

An internal reset is generated by the LVR circuit when the V_{DD} drops below the reset threshold. After V_{DD} reaching back up to the reset threshold, the $\overline{\text{RESET}}$ signal will remain asserted for 10ms before it is released. On initial power-up the LVR is enabled (default). After power-up the LVR can be disabled via the LVREN Bit in the PCON Register.

Note: The LVR logic is still functional in both the Idle and Power-down modes.

The reset threshold:

- 5 V operation: 4 V ± 0.25 V
- 3.3 V operation: 2.5 V ± 0.2 V

This logic supports approximately 0.1 V of hysteresis and 1 µs noise-cancelling delay.

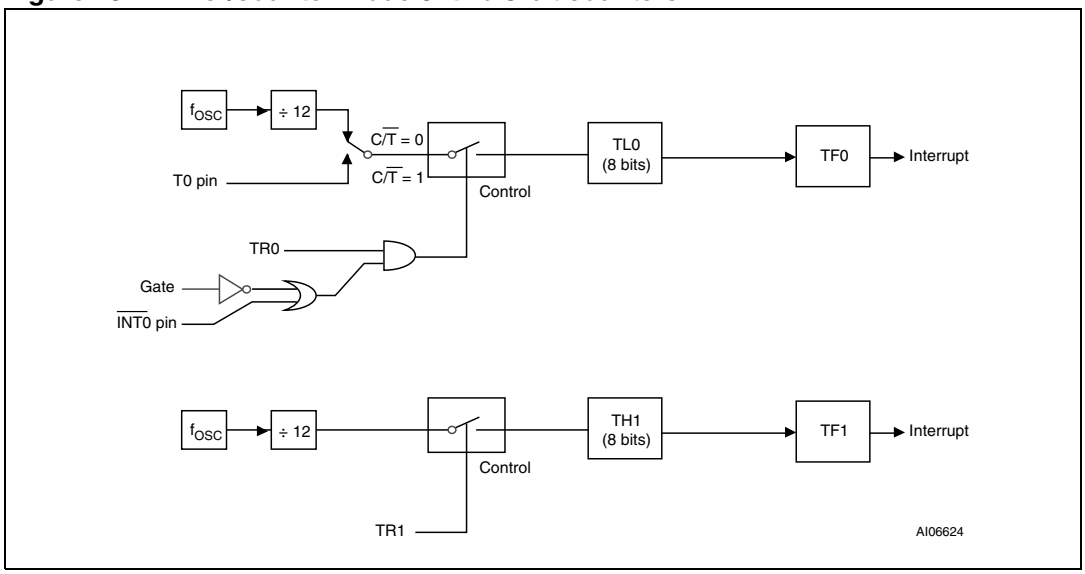
11.1.4 Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in *Figure 23*. TL0 uses the Timer 0 control Bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the “Timer 1“ Interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. With Timer 0 in Mode 3, an UPSD323xx devices can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

Figure 23. Timer/counter mode 3: two 8-bit counters



11.2 Timer 2

Like Timers 0 and 1, Timer 2 can operate as either an event timer or as an event counter. This is selected by Bit C/T2 in the special function register T2CON. It has three operating modes: Capture, Auto-reload, and Baud Rate Generator, which are selected by bits in the T2CON as shown in *Table 41*. In the Capture mode there are two options which are selected by Bit EXEN2 in T2CON. if EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets Bit TF2, the Timer 2 Overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt. The Capture mode is illustrated in *Figure 24*.

In the Auto-reload mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload

Table 74. Description of the UCON2 bits (continued)

Bit	Symbol	R/W	Function
2	EP1E	R/W	Endpoint1 enable. $\overline{\text{RESET}}$ clears this bit
1	STALL2	R/W	Endpoint2 Force Stall Bit. $\overline{\text{RESET}}$ clears this bit
0	STALL1	R/W	Endpoint1 Force Stall Bit. $\overline{\text{RESET}}$ clears this bit

Table 75. USB Endpoint0 status register (USTA: 0EDh)

7	6	5	4	3	2	1	0
RSEQ	SETUP	IN	OUT	RP0SIZ3	RP0SIZ2	RP0SIZ1	RP0SIZ0

Table 76. Description of the USTA bits

Bit	Symbol	R/W	Function
7	RSEQ	R/W	Endpoint0 receive data packet PID. (0=DATA0, 1=DATA1) This bit will be compared with the type of data packet last received for Endpoint0
6	SETUP	R	SETUP Token Detect Bit. This bit is set when the received token packet is a SEPUP token, PID = b1101.
5	IN	R	IN Token Detect Bit. This bit is set when the received token packet is an IN token.
4	OUT	R	OUT Token Detect Bit. This bit is set when the received token packet is an OUT token.
3 to 0	RP0SIZ3 to RP0SIZ0	R	The number of data bytes received in a DATA packet

Table 77. USB Endpoint0 data receive register (UDR0: 0EFh)

7	6	5	4	3	2	1	0
UDR0.7	UDR0.6	UDR0.5	UDR0.4	UDR0.3	UDR0.2	UDR0.1	UDR0.0

Table 78. USB Endpoint0 data transmit register (UDT0: 0E7h)

7	6	5	4	3	2	1	0
UDT0.7	UDT0.6	UDT0.5	UDT0.4	UDT0.3	UDT0.2	UDT0.1	UDT0.0

Table 79. USB Endpoint1 data transmit register (UDT1: 0E6h)

7	6	5	4	3	2	1	0
UDT1.7	UDT1.6	UDT1.5	UDT1.4	UDT1.3	UDT1.2	UDT1.1	UDT1.0

The USCL 8-bit prescaler register for USB is at E1h. The USCL should be loaded with a value that results in a clock rate of 6 MHz for the USB using the following formula:

USB clock input = (f_{OSC} / 2) / (Prescaler register value +1)

Where f_{OSC} is the MCU clock input frequency.

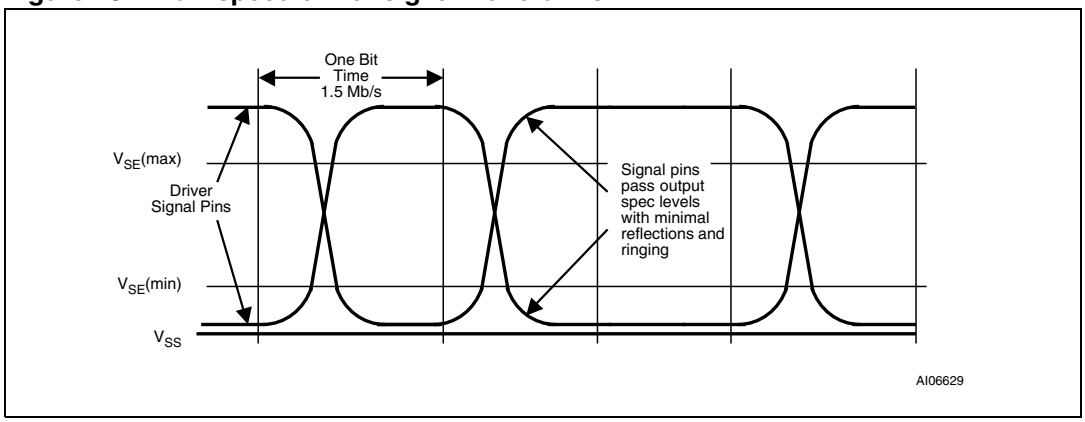
Note: USB works ONLY with the MCU Clock frequencies of 12, 24, or 36 MHz. The Prescaler values for these frequencies are 0, 1, and 2.

17.2.2 Low speed driver characteristics

The UPSD323xx devices use a differential output driver to drive the Low Speed USB data signal onto the USB cable. The output swings between the differential high and low state are well balanced to minimize signal skew. The slew rate control on the driver minimizes the radiated noise and cross talk on the USB cable. The driver's outputs support three-state operation to achieve bi-directional half duplex operation. The UPSD323xx devices driver tolerates a voltage on the signal pins of -0.5 V to 3.6 V with respect to local ground reference without damage. The driver tolerates this voltage for 10.0µs while the driver is active and driving, and tolerates this condition indefinitely when the driver is in its high impedance state.

A low speed USB connection is made through an unshielded, untwisted wire cable a maximum of 3 meters in length. The rise and fall time of the signals on this cable are well controlled to reduce RFI emissions while limiting delays, signaling skews and distortions. The UPSD323xx devices driver reaches the specified static signal levels with smooth rise and fall times, resulting in segments between low speed devices and the ports to which they are connected.

Figure 43. Low speed driver signal waveforms



17.3 Receiver characteristics

UPSD323xx devices have a differential input receiver which is able to accept the USB data signal. The receiver features an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is the common mode range, as shown in *Figure 44*. The receiver tolerates static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there is a single-ended receiver for each of the two data lines. The single-ended receivers have a switching threshold between 0.8 V and 2.0 V (TTL inputs).

Table 82. Transceiver AC characteristics

Symb	Parameter	Test Conditions(1)	Min	Max	Unit
tDRATE	Low Speed Data Rate	Ave. bit rate (1.5Mb/s ± 1.5%)	1.4775	1.5225	Mbit/s
tDJR1	Receiver Data Jitter Tolerance	To next transition, *Figure 46*(5)	–75	75	ns
tDJR2	Differential Input Sensitivity	For paired transition, *Figure 46*(5)	–45	45	ns
tDEOP	Differential to EOP Transition Skew	*Figure 47*(5)	–40	100	ns
tEOPR1	EOP Width at Receiver	Rejects as EOP(5,6)	165	—	ns
tEOPR2	EOP Width at Receiver	Accepts as EOP(5)	675	—	ns
tEOPT	Source EOP Width	—	–1.25	1.50	µs
tUDJ1	Differential Driver Jitter	To next transition, *Figure 48*	–95	95	ns
tUDJ2	Differential Driver Jitter	To paired transition, *Figure 48*	–150	150	ns
tR	USB Data Transition Rise Time	Notes 2, 3, 4	75	300	ns
tF	USB Data Transition Fall Time	Notes 2, 3, 4	75	300	ns
tRFM	Rise/Fall Time Matching	t_R / t_F	80	120	%
V_{CRS}	Output Signal Crossover Voltage	—	1.3	2.0	V

1. V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to 70°C.
2. Level guaranteed for range of V_{CC} = 4.5 V to 5.5 V.
3. With RPU, external idle resistor, 7.5κ±2%, D- to V_{CC}.
4. C_L of 50 pF (75 ns) to 350 pF (300 ns).
5. Measured at crossover point of differential data signals.
6. USB specification indicates 330 ns.

Table 83. Methods of programming different functional blocks of the PSD module

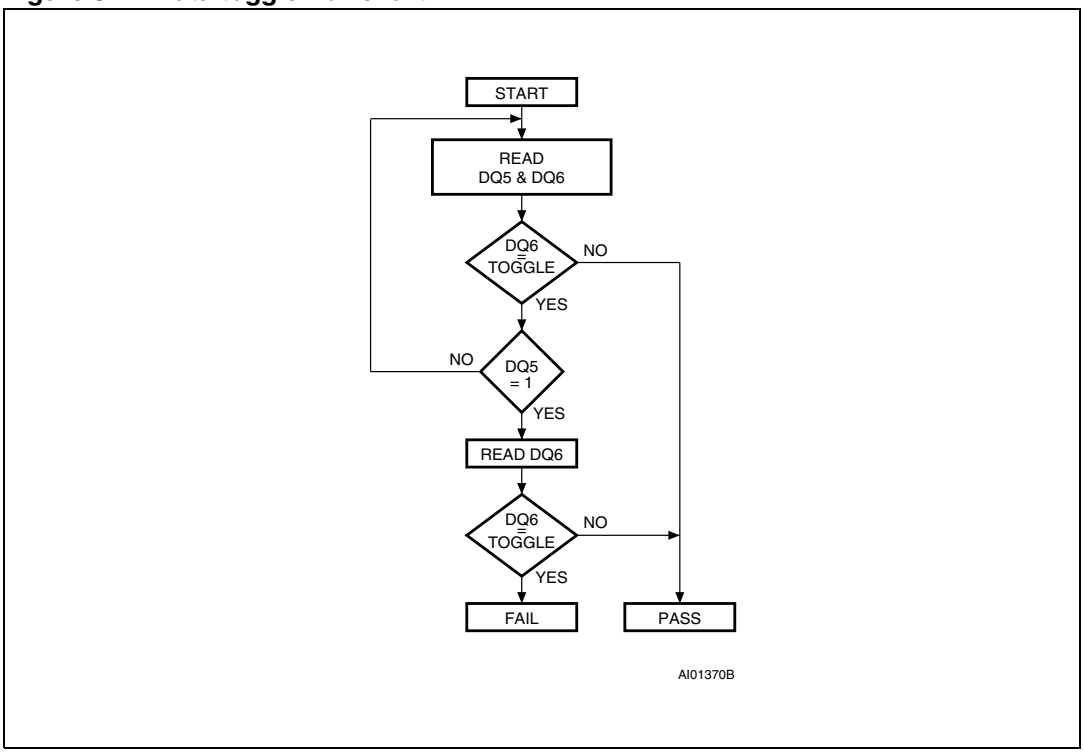
Functional Block	JTAG programming	Device programmer	IAP
Primary Flash memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD array (DPLD and CPLD)	Yes	Yes	No
PSD module configuration	Yes	Yes	No

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed, to compare the byte that was written to Flash memory with the byte that was intended to be written.

When using the Data Toggle method after an Erase cycle, *Figure 52* still applies. the Toggle Flag bit (DQ6) toggles until the Erase cycle is complete. A 1 on the Error Flag bit (DQ5) indicates a time-out condition on the Erase cycle; a '0' indicates no error. The MCU can read any location within the sector being erased to get the Toggle Flag bit (DQ6) and the Error Flag bit (DQ5).

PSDsoft Express generates ANSI C code functions which implement these Data Toggling algorithms.

Figure 52. Data toggle flowchart



22.6.3 Unlock Bypass

The Unlock Bypass instructions allow the system to program bytes to the Flash memories faster than using the standard Program instruction. The Unlock Bypass mode is entered by first initiating two Unlock cycles. This is followed by a third WRITE cycle containing the Unlock Bypass code, 20h (as shown in *Table 85*).

The Flash memory then enters the Unlock Bypass mode. A two-cycle Unlock Bypass Program instruction is all that is required to program in this mode. The first cycle in this instruction contains the Unlock Bypass Program code, A0h. The second cycle contains the program address and data. Additional data is programmed in the same manner. These instructions dispense with the initial two Unlock cycles required in the standard Program instruction, resulting in faster total Flash memory programming.

During the Unlock Bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset Flash instructions are valid.

23 PLDs

PLDs bring programmable logic functionality to the UPSD. After specifying the logic for the PLDs using PSDsoft Express, the logic is programmed into the device and available upon Power-up.

Table 90. DPLD and CPLD Inputs

Input Source	Input Name	Number of Signals
MCU Address Bus	A15-A0	16
MCU Control Signals	$\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$, ALE	4
RESET	$\overline{RST}$	1
Power-down	PDN	1
Port A Input Macrocells(1)	PA7-PA0	8
Port B Input Macrocells	PB7-PB0	8
Port C Input Macrocells	PC2-4, PC7	4
Port D Inputs	PD2-PD1	2
Page Register	PGR7-PGR0	8
Macrocell AB Feedback	MCELLAB.FB7-FB0	8
Macrocell BC Feedback	MCELLBC.FB7-FB0	8
Flash memory Program Status bit	Ready/$\overline{Busy}$	1

Note: 1. These inputs are not available in the 52-pin package.

The PSD module contains two PLDs: the Decode PLD (DPLD), and the Complex PLD (CPLD). The PLDs are briefly discussed in the next few paragraphs, and in more detail in *Section 23.2: Decode PLD (DPLD)*, and *Section 23.3: Complex PLD (CPLD)*. *Figure 57* shows the configuration of the PLDs.

The DPLD performs address decoding for Select signals for PSD module components, such as memory, registers, and I/O ports.

The CPLD can be used for logic functions, such as loadable counters and shift registers, state machines, and encoding and decoding logic. These logic functions can be constructed using the Output Macrocells (OMC), Input Macrocells (IMC), and the AND Array. The CPLD can also be used to generate External Chip Select (ECS1-ECS2) signals.

The AND Array is used to form product terms. These product terms are specified using PSDsoft. The PLD input signals consist of internal MCU signals and external inputs from the I/O ports. The input signals are shown in *Table 90*.

23.1 Turbo bit in PSD module

The PLDs can minimize power consumption by switching off when inputs remain unchanged for an extended time of about 70ns. Resetting the Turbo bit to '0' (Bit 3 of PMMR0) automatically places the PLDs into standby if no inputs are changing. Turning the Turbo mode off increases propagation delays while reducing power consumption.

flop. The flip-flop is clocked on the rising edge of CLKIN (PD1). The preset and clear are active High inputs. Each clear input can use up to two product terms.

Table 92. Output macrocell port and data bit assignments

Output Macrocell	Port Assignment (1,2)	Native Product Terms	Max. Borrowed Product Terms	Data Bit for Loading or Reading
McellAB0	Port A0, B0	3	6	D0
McellAB1	Port A1, B1	3	6	D1
McellAB2	Port A2, B2	3	6	D2
McellAB3	Port A3, B3	3	6	D3
McellAB4	Port A4, B4	3	6	D4
McellAB5	Port A5, B5	3	6	D5
McellAB6	Port A6, B6	3	6	D6
McellAB7	Port A7, B7	3	6	D7
McellBC0	Port B0	4	5	D0
McellBC1	Port B1	4	5	D1
McellBC2	Port B2, C2	4	5	D2
McellBC3	Port B3, C3	4	5	D3
McellBC4	Port B4, C4	4	6	D4
McellBC5	Port B5	4	6	D5
McellBC6	Port B6	4	6	D6
McellBC7	Port B7, C7	4	6	D7

1. McellAB0-McellAB7 can only be assigned to Port B in the 52-pin package
2. Port PC0, PC1, PC5, and PC6 are assigned to JTAG pins and are not available as Macrocell outputs.

23.5 Product term allocator

The CPLD has a Product Term Allocator. PSDsoft uses the Product Term Allocator to borrow and place product terms from one macrocell to another. The following list summarizes how product terms are allocated:

- McellAB0-McellAB7 all have three native product terms and may borrow up to six more
- McellBC0-McellBC3 all have four native product terms and may borrow up to five more
- McellBC4-McellBC7 all have four native product terms and may borrow up to six more.

Each macrocell may only borrow product terms from certain other macrocells. Product terms already in use by one macrocell are not available for another macrocell.

If an equation requires more product terms than are available to it, then “external” product terms are required, which consume other Output Macrocells (OMC). If external product terms are used, extra delay is added for the equation that required the extra product terms.

This is called product term expansion. PSDsoft Express performs this expansion as needed.

29 AC/DC parameters

These tables describe the AD and DC parameters of the UPSD323xx devices:

- DC Electrical Specification
- AC Timing Specification
- PLD Timing
  - Combinatorial Timing
  - Synchronous Clock mode
  - Asynchronous Clock mode
  - Input Macrocell Timing
- MCU module Timing
  - READ Timing
  - WRITE Timing
  - Power-down and $\overline{\text{RESET}}$ Timing

The following are issues concerning the parameters presented:

- In the DC specification the supply current is given for different modes of operation.
- The AC power component gives the PLD, Flash memory, and SRAM mA/MHz specification. *Figure 70* and *Figure 71* show the PLD mA/MHz as a function of the number of Product Terms (PT) used.
- In the PLD timing parameters, add the required delay when Turbo Bit is '0.'

Figure 70. PLD I_{CC}/frequency consumption (5 V range)

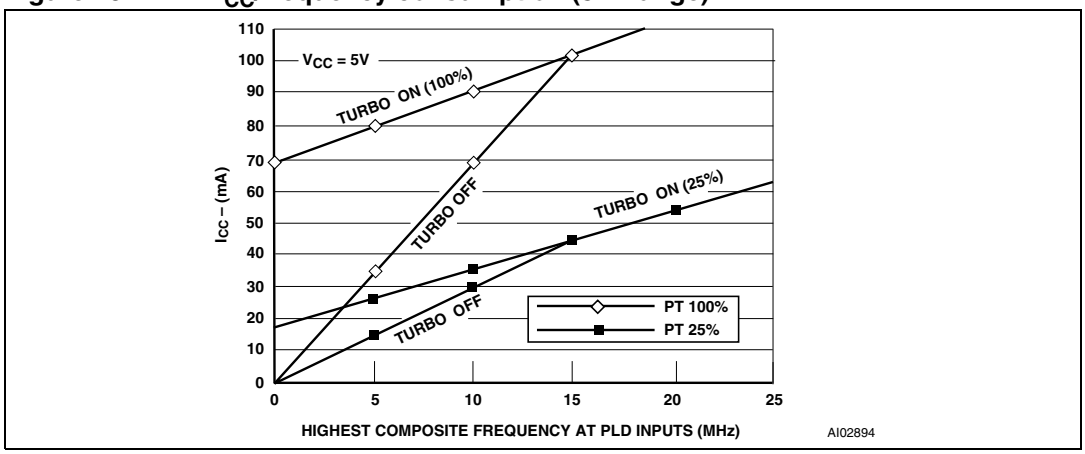


Table 125. External data memory AC characteristics (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{WLWH}	$\overline{WR}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{LLAX2}	Address hold after ALE	56		2 t_{CLCL} – 27		ns
t_{RHDX}	$\overline{RD}$ to valid data in		118		5 t_{CLCL} – 90	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		63		2 t_{CLCL} – 20	ns
t_{LLDV}	ALE to valid data in		200		8 t_{CLCL} – 133	ns
t_{AVDV}	Address to valid data in		220		9 t_{CLCL} – 155	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	75	175	3 t_{CLCL} – 50	t_{CLCL} + 50	ns
t_{AVWL}	Address valid to $\overline{WR}$ or $\overline{RD}$	67		4 t_{CLCL} – 97		ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	17	67	t_{CLCL} – 25	t_{CLCL} + 25	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5		t_{CLCL} – 37		ns
t_{QVWH}	Data set-up before $\overline{WR}$	170		7 t_{CLCL} – 122		ns
t_{WHQX}	Data hold after $\overline{WR}$	15		t_{CLCL} – 27		ns
t_{RLAZ}	Address float after $\overline{RD}$		0		0	ns

1. Conditions (in addition to those in *Table 114*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)

Table 126. A/D analog specification

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
AV_{REF}	Analog power supply input voltage range		V_{SS}		V_{CC}	V
V_{AN}	Analog input voltage range		V_{SS} – 0.3		AV_{REF} + 0.3	V
I_{AVDD}	Current following between V_{CC} and V_{SS}				200	µA
CA_{IN}	Overall accuracy				±2	l.s.b.
N_{NLE}	Non-linearity error				±2	l.s.b.
N_{DNLE}	Differential non-linearity error				±2	l.s.b.
N_{ZOE}	Zero-offset error				±2	l.s.b.
N_{FSE}	Full scale error				±2	l.s.b.
N_{GE}	Gain error				±2	l.s.b.
t_{CONV}	Conversion time	at 8 MHz clock			20	µs

Figure 90. PSD module AC measurement load circuit

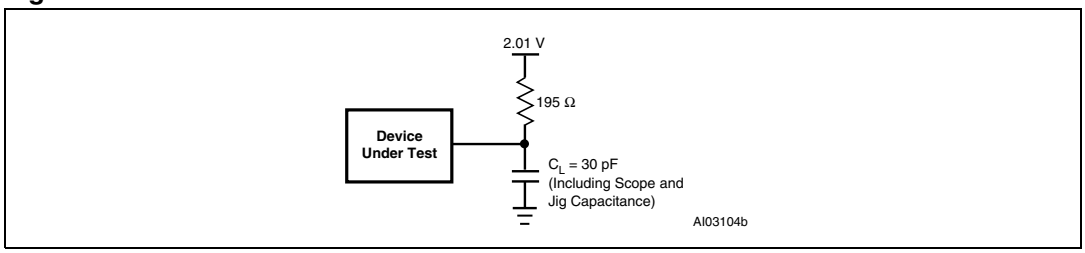


Table 145. Capacitance

Symbol	Parameter	Test conditions (1)	Typ.(2)	Max.	Unit
C_{IN}	Input capacitance (for input pins)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Output capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF

1. Sampled only, not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.