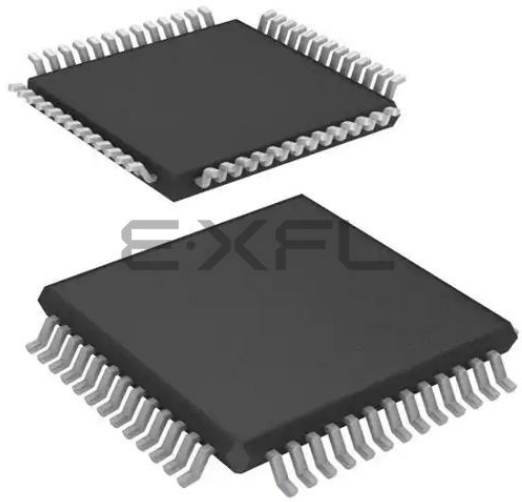

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, UART/USART, USB
Peripherals	LVR, POR, PWM, WDT
Number of I/O	37
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3234a-40t6t

Figure 1. UPSD323xx block diagram

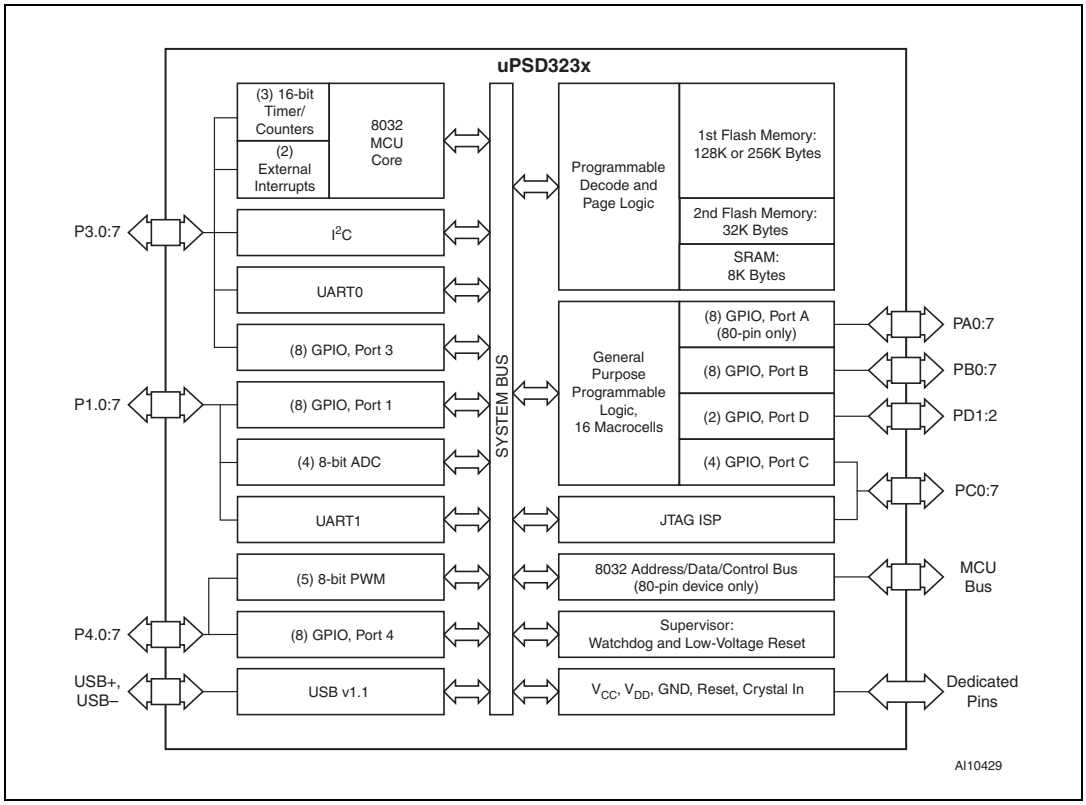


Table 2. 80-pin package pin description (continued)

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
	AD7	47	I/O	Multiplexed Address/Data bus A7/D7	
P1.0	T2	52	I/O	General I/O port pin	Timer 2 Count input
P1.1	TX2	54	I/O	General I/O port pin	Timer 2 Trigger input
P1.2	RxD1	56	I/O	General I/O port pin	2nd UART Receive
P1.3	TxD1	58	I/O	General I/O port pin	2nd UART Transmit
P1.4	ADC0	59	I/O	General I/O port pin	ADC Channel 0 input
P1.5	ADC1	60	I/O	General I/O port pin	ADC Channel 1 input
P1.6	ADC2	61	I/O	General I/O port pin	ADC Channel 2 input
P1.7	ADC3	64	I/O	General I/O port pin	ADC Channel 3 input
	A8	51	O	External Bus, Address A8	
	A9	53	O	External Bus, Address A9	
	A10	55	O	External Bus, Address A10	
	A11	57	O	External Bus, Address A11	
P3.0	RxD0	75	I/O	General I/O port pin	UART Receive
P3.1	TxD0	77	I/O	General I/O port pin	UART Transmit
P3.2	EXINT0	79	I/O	General I/O port pin	Interrupt 0 input / Timer 0 gate control
P3.3	EXINT1	2	I/O	General I/O port pin	Interrupt 1 input / Timer 1 gate control
P3.4	T0	40	I/O	General I/O port pin	Counter 0 input
P3.5	T1	42	I/O	General I/O port pin	Counter 1 input
P3.6	SDA1	44	I/O	General I/O port pin	I^2C Bus serial data I/O
P3.7	SCL1	46	I/O	General I/O port pin	I^2C Bus clock I/O
P4.0	DDC SDA	33	I/O	General I/O port pin	
P4.1	DDC SCL	31	I/O	General I/O port pin	
P4.2	DDC V_{SYNC}	30	I/O	General I/O port pin	
P4.3	PWM0	27	I/O	General I/O port pin	8-bit Pulse Width Modulation output 0
P4.4	PWM1	25	I/O	General I/O port pin	8-bit Pulse Width Modulation output 1
P4.5	PWM2	23	I/O	General I/O port pin	8-bit Pulse Width Modulation output 2
P4.6	PWM3	19	I/O	General I/O port pin	8-bit Pulse Width Modulation output 3

Table 2. 80-pin package pin description (continued)

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
	JTAG TMS	20	I	JTAG pin	PLD macrocell outputs PLD inputs JTAG pins are dedicated pins
	JTAG TCK	16	I	JTAG pin	
PC3	TSTAT	14	I/O	General I/O port pin	
PC4	TERR_	9	I/O	General I/O port pin	
	JTAG TDI	7	I	JTAG pin	
	JTAG TDO	6	O	JTAG pin	
PC7		5	I/O	General I/O port pin	
PD1	CLKIN	3	I/O	General I/O port pin	PLD I/O Clock input to PLD and APD
PD2		1	I/O	General I/O port pin	PLD I/O Chip select to PSD module
Vcc		12			
Vcc		50			
GND		13			
GND		29			
GND		69			
	USB+	10			
NC		11			
NC		17			
NC		71			

1.1 52-pin package I/O port

The 52-pin package members of the UPSD323xx devices have the same port pins as those of the 80-pin package except:

- Port 0 (P0.0-P0.7, external address/data bus AD0-AD7)
- Port 2 (P2.0-P2.3, external address bus A8-A11)
- Port A (PA0-PA7)
- Port D (PD2)
- Bus control signal (RD,WR,PSEN,ALE)
- Pin 5 requires a pull-up resistor (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices) for all devices, with or without USB function.

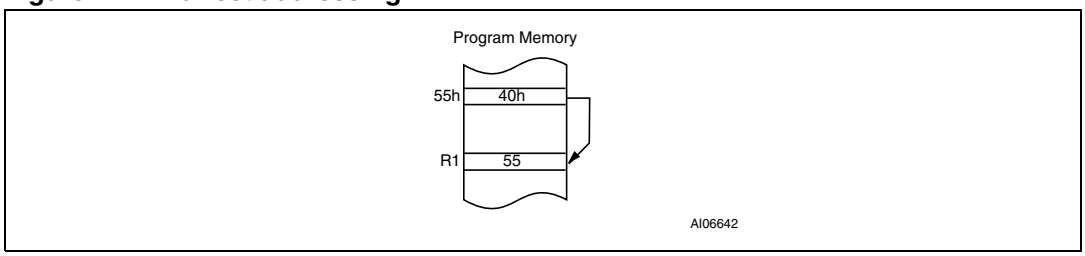
2.9.2 Indirect addressing

In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed. The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer. The address register for 16-bit addresses can only be the 16-bit “data pointer” register, DPTR.

Example:

```
mov @R1, #40 H ;[R1] <-----40H
```

Figure 11. Indirect addressing



2.9.3 Register addressing

The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient, since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the two bank select bits in the PSW.

Example:

```
mov PSW, #0001000B ; select Bank0
mov A, #30H
mov R1, A
```

2.9.4 Register-specific addressing

Some instructions are specific to a certain register. For example, some instructions always operate on the Accumulator, or Data Pointer, etc., so no address byte is needed to point it. The opcode itself does that.

2.9.5 Immediate constants addressing

The value of a constant can follow the opcode in Program memory.

Example:

```
mov A, #10H.
```

2.9.6 Indexed addressing

Only Program memory can be accessed with indexed addressing, and it can only be read. This addressing mode is intended for reading look-up tables in Program memory. A 16-bit base register (either DPTR or PC) points to the base of the table, and the Accumulator is set up with the table entry number. The address of the table entry in Program memory is formed by adding the Accumulator data to the base pointer.

Figure 13. State sequence in UPSD323xx devices

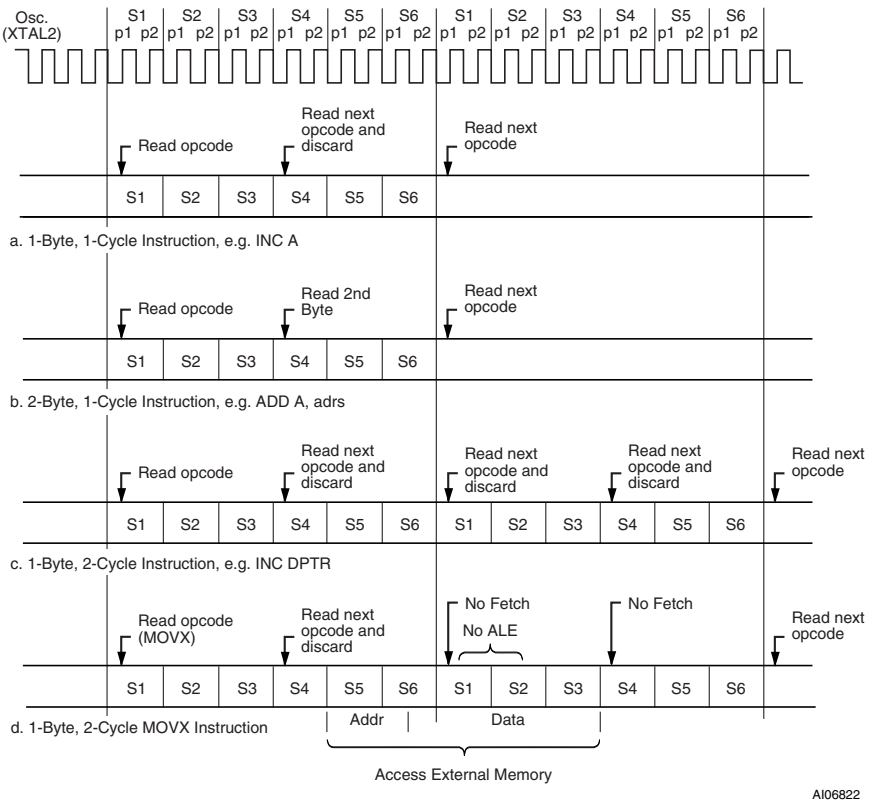


Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
A1	PWMCON	PWML	PWMP	PWME	CFG4	CFG3	CFG2	CFG1	CFG0	00	PWM Control Polarity
A2	PWM0									00	PWM0 Output Duty Cycle
A3	PWM1									00	PWM1 Output Duty Cycle
A4	PWM2									00	PWM2 Output Duty Cycle
A5	PWM3									00	PWM3 Output Duty Cycle
A6	WDRST									00	Watch Dog Reset
A7	IEA	EDDC			ES2			EI^{2}C	EUSB	00	Interrupt Enable (2nd)
A8	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00	Interrupt Enable
A9											
AA	PWM4P									00	PWM 4 Period
AB	PWM4W									00	PWM 4 Pulse Width
AE	WDKEY									00	Watch Dog Key Register
B0	P3									FF	Port 3
B1	PSCL0L									00	Prescaler 0 Low (8-bit)
B2	PSCL0H									00	Prescaler 0 High (8-bit)
B3	PSCL1L									00	Prescaler 1 Low (8-bit)
B4	PSCL1H									00	Prescaler 1 High (8-bit)
B7	IPA	PDDC			PS2			PI2C	PUSB	00	Interrupt Priority (2nd)
B8	IP			PT2	PS	PT1	PX1	PT0	PX0	00	Interrupt Priority
C0	P4									FF	New Port 4
C8	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00	Timer 2 Control

and set EXF2. Auto-reload mode is illustrated in the Standard Serial Interface (UART) *Figure 25*. The Baud Rate Generation mode is selected by (RCLK, RCLK1)=1 and/or (TCLK, TCLK1)=1. It is described in conjunction with the serial port.

Table 40. Timer/counter 2 control register (T2CON)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2

Table 41. Description of the T2CON bits

Bit	Symbol	Function
7	TF2	Timer 2 overflow flag. Set by a Timer 2 overflow, and must be cleared by software. TF2 will not be set when either (RCLK, RCLK1)=1 or (TCLK, TCLK)=1
6	EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2=1. When Timer 2 Interrupt is enabled, EXF2=1 will cause the CPU to vector to the Timer 2 Interrupt routine. EXF2 must be cleared by software
5	RCLK(1)	Receive clock flag (UART 1). When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in Modes 1 and 3. TCLK=0 causes Timer 1 overflow to be used for the receive clock
4	TCLK(1)	Transmit clock flag (UART 1). When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in Modes 1 and 3. TCLK=0 causes Timer 1 overflow to be used for the transmit clock
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2=0 causes Time 2 to ignore events at T2EX
2	TR2	Start/stop control for Timer 2. A logic 1 starts the timer
1	C/$\overline{T}$2	Timer or Counter select for Timer 2. Cleared for timer operation (input from internal system clock, t_{CPU}); set for external event counter operation (negative edge triggered)
0	CP/$\overline{RL}$2	Capture/reload flag. When set, capture will occur on negative transition of T2EX if EXEN2=1. When cleared, auto-reload will occur either with TImer 2 overflows, or negative transitions of T2EX when EXEN2=1. When either (RCLK, RCLK1)=1 or (TCLK, TCLK)=1, this bit is ignored, and timer is forced to auto-reload on Timer 2 overflow

1. The RCLK1 and TCLK1 Bits in the PCON Register control UART 2, and have the same function as RCLK and TCLK.

Table 52. Selection of the serial clock frequency SCL in Master mode (continued)

CR2	CR1	CR0	f_{OSC} divisor	Bit rate (kHz) at f_{OSC}			
				12 MHz	24 MHz	36 MHz	40 MHz
1	1	0	480	12.5	25	37.5	41
1	1	1	960	6.25	12.5	18.75	20

15.1 Serial status register (SxSTA: S1STA, S2STA)

SxSTA is a “Read-only” register. The contents of this register may be used as a vector to a service routine. This optimized the response time of the software and consequently that of the I²C-bus. The status codes for all possible modes of the I²C-bus interface are given Table *Table 54*.

This flag is set, and an interrupt is generated, after any of the following events occur.

1. Own slave address has been received during AA = 1: ack_int
2. The general call address has been received while GC(SxADR.0) = 1 and AA = 1:
3. A data byte has been received or transmitted in Master mode (even if arbitration is lost): ack_int
4. A data byte has been received or transmitted as selected slave: ack_int
5. A stop condition is received as selected slave receiver or transmitter: stop_int

15.2 Data shift register (SxDAT: S1DAT, S2DAT)

SxDAT contains the serial data to be transmitted or data which has just been received. The MSB (Bit 7) is transmitted or received first; that is, data shifted from right to left.

Table 53. Serial status register (SxSTA)

7	6	5	4	3	2	1	0
GC	STOP	INTR	TX_MODE	BBUSY	BLOST	/ACK_REP	SLV

1. Reset DDC1 enable (by default, DDC1 enable is cleared as LOW after Power-on Reset).
2. Set SWENB as high (the default value is zero.)
3. Depending on the data size of EDID data, set EX_DAT as LOW (128 bytes) or HIGH (256 bytes).
4. By using bulky moving commands (DDCADR, RAMBUF involved) to move the entire EDID data to RAM buffer.
5. Reset SWENB to LOW.
6. Reset DDCADR to 00h.
7. Set DDC1 enable as HIGH.

In case SWENB is set as high, interrupt service routine is finished within 133 machine cycle in 40MHz System clock.

The maximum V_{SYNC} (V_{CLK}) frequency is 25Khz (40µs). And the 9th clock of V_{SYNC} (V_{CLK}) is interrupt period.

So the machine cycle be needed is calculated as below. For example,

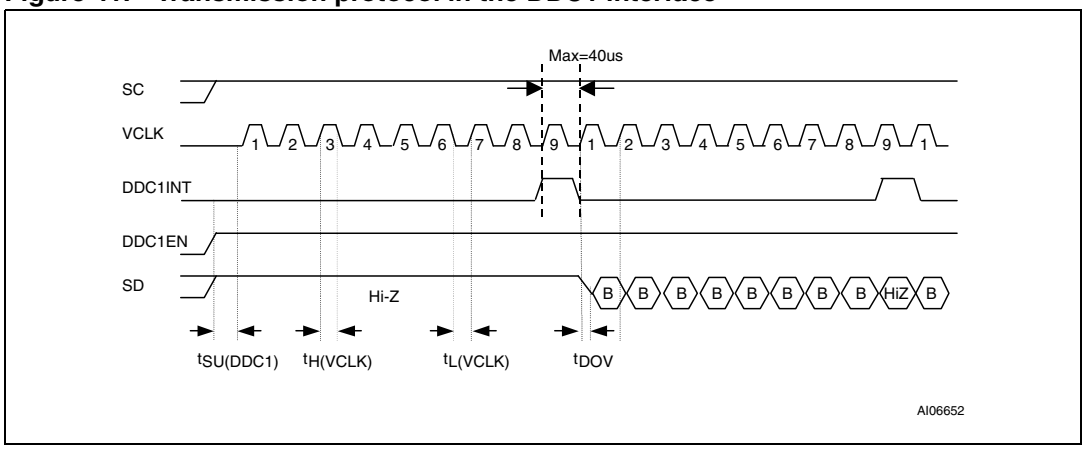
- When 40MHz system clock, 40µs = 133 x (25ns x 12); 133 machine cycle.
- 12MHz system clock, 40µs = 40 x (83.3ns x 12); 40 machine cycle.
- 8MHz system clock, 40µs = 26 x (125ns x 12); 26 machine cycle.

Note: If EX_DAT equals to LOW, it is meant the lower part is occupied by DDC1 operation and the upper part is still free to the system. Nevertheless, the effect of the post increment just applies to the part related to DDC1 operation. In other words, the system program is still able to address the locations from 128 to 255 in the RAM buffer through MOVX command but without the facility of the post increment. For example, the case of accessing 200 of the RAM Buffer:

MOV R0, #200, and

MOVX A, @R0

Figure 41. Transmission protocol in the DDC1 interface



22.5.4 Data polling flag (DQ7)

When erasing or programming in Flash memory, the Data Polling flag bit (DQ7) outputs the complement of the bit being entered for programming/writing on the DQ7 Bit. Once the Program instruction or the WRITE operation is completed, the true logic value is read on the Data Polling flag bit (DQ7) (in a READ operation).

- Data Polling is effective after the fourth WRITE pulse (for a Program instruction) or after the sixth WRITE pulse (for an Erase instruction). It must be performed at the address being programmed or at an address within the Flash memory sector being erased.
- During an Erase cycle, the Data Polling flag bit (DQ7) outputs a '0.' After completion of the cycle, the Data Polling flag bit (DQ7) outputs the last bit programmed (it is a '1' after erasing).
- If the byte to be programmed is in a protected Flash memory sector, the instruction is ignored.
- If all the Flash memory sectors to be erased are protected, the Data Polling flag bit (DQ7) is reset to '0' for about 100µs, and then returns to the previous addressed byte. No erasure is performed.

22.5.5 Toggle flag (DQ6)

The Flash memory offers another way for determining when the Program cycle is completed. During the internal WRITE operation and when either the FS0-FS7 or CSBOOT0-CSBOOT3 is true, the Toggle flag bit (DQ6) toggles from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory.

When the internal cycle is complete, the toggling stops and the data READ on the Data Bus D0-D7 is the addressed memory byte. The device is now accessible for a new READ or WRITE operation. The cycle is finished when two successive Reads yield the same output data.

- The Toggle flag bit (DQ6) is effective after the fourth WRITE pulse (for a Program instruction) or after the sixth WRITE pulse (for an Erase instruction).
- If the byte to be programmed belongs to a protected Flash memory sector, the instruction is ignored.
- If all the Flash memory sectors selected for erasure are protected, the Toggle flag bit (DQ6) toggles to '0' for about 100µs and then returns to the previous addressed byte.

22.5.6 Error flag (DQ5)

During a normal Program or Erase cycle, the Error flag bit (DQ5) is to '0.' This bit is set to '1' when there is a failure during Flash memory Byte Program, Sector Erase, or Bulk Erase cycle.

In the case of Flash memory programming, the Error flag bit (DQ5) indicates the attempt to program a Flash memory bit from the programmed state, '0', to the erased state, '1,' which is not valid. The Error flag bit (DQ5) may also indicate a Time-out condition while attempting to program a byte.

In case of an error in a Flash memory Sector Erase or Byte Program cycle, the Flash memory sector in which the error occurred or to which the programmed byte belongs must no longer be used. Other Flash memory sectors may still be used. The Error Flag bit (DQ5) is reset after a Reset Flash instruction.

23 PLDs

PLDs bring programmable logic functionality to the UPSD. After specifying the logic for the PLDs using PSDsoft Express, the logic is programmed into the device and available upon Power-up.

Table 90. DPLD and CPLD Inputs

Input Source	Input Name	Number of Signals
MCU Address Bus	A15-A0	16
MCU Control Signals	$\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$, ALE	4
RESET	$\overline{RST}$	1
Power-down	PDN	1
Port A Input Macrocells(1)	PA7-PA0	8
Port B Input Macrocells	PB7-PB0	8
Port C Input Macrocells	PC2-4, PC7	4
Port D Inputs	PD2-PD1	2
Page Register	PGR7-PGR0	8
Macrocell AB Feedback	MCELLAB.FB7-FB0	8
Macrocell BC Feedback	MCELLBC.FB7-FB0	8
Flash memory Program Status bit	Ready/$\overline{Busy}$	1

Note: 1. These inputs are not available in the 52-pin package.

The PSD module contains two PLDs: the Decode PLD (DPLD), and the Complex PLD (CPLD). The PLDs are briefly discussed in the next few paragraphs, and in more detail in *Section 23.2: Decode PLD (DPLD)*, and *Section 23.3: Complex PLD (CPLD)*. *Figure 57* shows the configuration of the PLDs.

The DPLD performs address decoding for Select signals for PSD module components, such as memory, registers, and I/O ports.

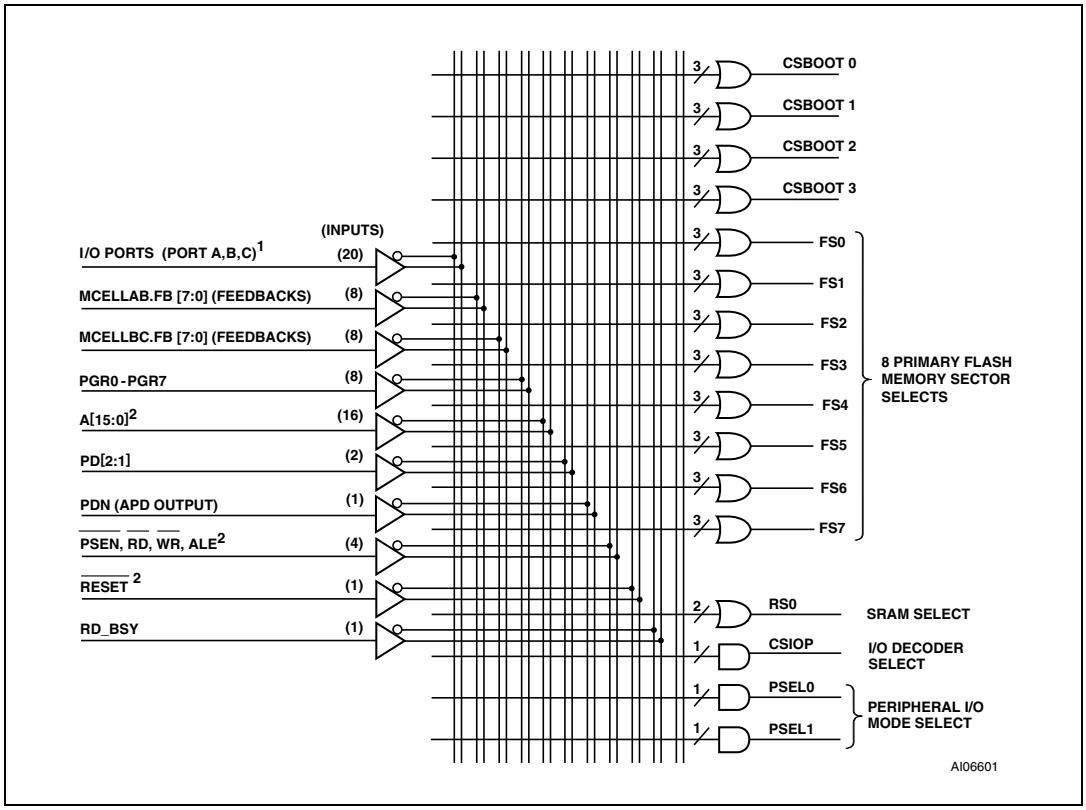
The CPLD can be used for logic functions, such as loadable counters and shift registers, state machines, and encoding and decoding logic. These logic functions can be constructed using the Output Macrocells (OMC), Input Macrocells (IMC), and the AND Array. The CPLD can also be used to generate External Chip Select (ECS1-ECS2) signals.

The AND Array is used to form product terms. These product terms are specified using PSDsoft. The PLD input signals consist of internal MCU signals and external inputs from the I/O ports. The input signals are shown in *Table 90*.

23.1 Turbo bit in PSD module

The PLDs can minimize power consumption by switching off when inputs remain unchanged for an extended time of about 70ns. Resetting the Turbo bit to '0' (Bit 3 of PMMR0) automatically places the PLDs into standby if no inputs are changing. Turning the Turbo mode off increases propagation delays while reducing power consumption.

Table 91. DPLD logic array



1. Port A inputs are not available in the 52-pin package
2. Inputs from the MCU module

23.3 Complex PLD (CPLD)

The CPLD can be used to implement system logic functions, such as loadable counters and shift registers, system mailboxes, handshaking protocols, state machines, and random logic. The CPLD can also be used to generate External Chip Select (ECS1-ECS2), routed to Port D.

Although External Chip Select (ECS1-ECS2) can be produced by any Output Macrocell (OMC), these External Chip Select (ECS1-ECS2) on Port D do not consume any Output Macrocells (OMC).

As shown in *Figure 58*, the CPLD has the following blocks:

- 20 Input Macrocells (IMC)
- 16 Output Macrocells (OMC)
- Macrocell Allocator
- Product Term Allocator
- AND Array capable of generating up to 137 product terms
- Four I/O Ports.

Each of the blocks are described in the sections that follow.

Figure 66. Port D external chip select signals

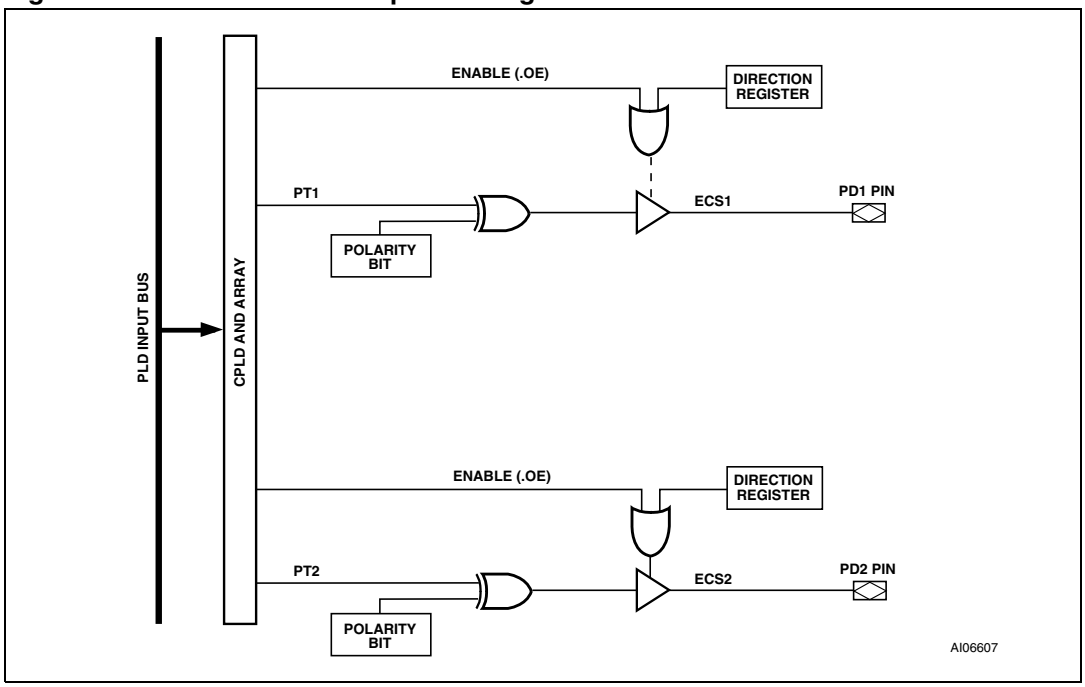


Figure 71. PLD I_{CC}/frequency consumption (3 V range)

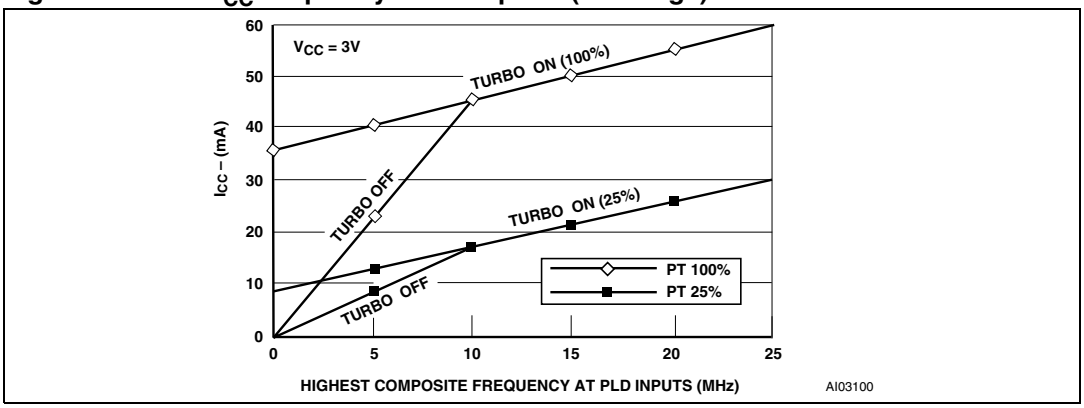


Table 108. PSD module example, typ. power calculation at V_{CC} = 5.0 V (Turbo mode off)

Conditions		
	MCU clock frequency	= 12 MHz
Highest Composite PLD input frequency		
	(Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)		= 2 MHz
	% Flash memory access	= 80%
	% SRAM access	= 15%
	% I/O access	= 5% (no additional power above base)
Operational modes		
	% Normal	= 40%
	% Power-down mode	= 60%
Number of product terms used		
	(from fitter report)	= 45 PT
	% of total product terms	= 45/182 = 24.7%
	Turbo mode	= Off

Table 118. DC characteristics (5 V devices) (continued)

Symbol	Parameter		Test conditions (in addition to those in *Table 113*)	Min.	Typ.	Max.	Unit
I_{FR}	XTAL feedback resistor current (XTAL1)		XTAL1 = V_{CC} XTAL2 = V_{SS}	–20		–50	µA
I_{LI}	Input leakage current		$V_{SS} < V_{IN} < V_{CC}$	–1		1	µA
I_{LO}	Output leakage current		$0.45 < V_{OUT} < V_{CC}$	–10		10	µA
I_{PD}(1)	Power-down mode		V_{CC} = 5.5 V LVD logic disabled			250	µA
			LVD logic enabled			380	µA
I_{CC_CPU} (2,3,6)	Active (12 MHz)		V_{CC} = 5 V		20	30	mA
	Idle (12 MHz)				8	10	mA
	Active (24 MHz)		V_{CC} = 5 V		30	38	mA
	Idle (24 MHz)				15	20	mA
	Active (40 MHz)		V_{CC} = 5 V		40	62	mA
	Idle (40 MHz)				20	30	mA
I_{CC_PSD} (DC)(6)	Operating supply current	PLD Only	PLD_TURBO = Off, f = 0 MHz(4)		0		µA/PT(5)
			PLD_TURBO = On, f = 0 MHz		400	700	µA/PT
		Flash memory	During Flash memory WRITE/Erase Only		15	30	mA
			Read-only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC_PSD} (AC)(6)	PLD AC Base			Note 5			
	Flash memory AC adder				2.5	3.5	mA/MHz
	SRAM AC adder				1.5	3.0	mA/MHz

1. I_{PD} (Power-down mode) is measured with:
XTAL1=V_{SS}; XTAL2=not connected; $\overline{\text{RESET}}$=V_{CC}; Port 0 =V_{CC}; all other pins are disconnected. PLD not in Turbo mode.
2. I_{CC_CPU} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS}+0.5 V, V_{IH} = Vcc – 0.5 V, XTAL2 = not connected; $\overline{\text{RESET}}$=V_{SS}; Port 0=V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (approximately 1mA).
3. I_{CC_CPU} (Idle mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS}+0.5 V, V_{IH} = V_{CC}– 0.5 V, XTAL2 = not connected; Port 0 = V_{CC};
4. $\overline{\text{RESET}}$=V_{CC}; all other pins are disconnected.
5. PLD is in non-Turbo mode and none of the inputs are switching.
6. See *Figure 70* for the PLD current calculation.
7. I/O current = 0 mA, all I/O pins are disconnected.

Table 124. External data memory AC characteristics (with the 5 V MCU module)

Symbol	Parameter[1]	40 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 24 to 40 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ pulse width	120		6 t_{CLCL} – 30		ns
t_{WLWH}	$\overline{WR}$ pulse width	120		6 t_{CLCL} – 30		ns
t_{LLAX2}	Address hold after ALE	10		t_{CLCL} – 15		ns
t_{RHDX}	$\overline{RD}$ to valid data in		75		5 t_{CLCL} – 50	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		38		2 t_{CLCL} – 12	ns
t_{LLDV}	ALE to valid data in		150		8 t_{CLCL} – 50	ns
t_{AVDV}	Address to valid data in		150		9 t_{CLCL} – 75	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	60	90	3 t_{CLCL} – 15	t_{CLCL} + 15	ns
t_{AVWL}	Address valid to $\overline{WR}$ or $\overline{RD}$	70		4 t_{CLCL} – 30		ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	10	40	t_{CLCL} – 15	t_{CLCL} + 15	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5		t_{CLCL} – 20		ns
t_{QVWH}	Data set-up before $\overline{WR}$	125		7 t_{CLCL} – 50		ns
t_{WHQX}	Data hold after $\overline{WR}$	5		t_{CLCL} – 20		ns
t_{RLAZ}	Address float after $\overline{RD}$		0		0	ns

1. Conditions (in addition to those in *Table 113*, V_{CC} = 4.5 to 5.5 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF; C_L for other outputs is 80 pF

Figure 76. Input to output disable / enable

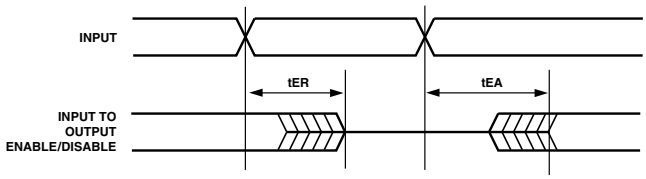


Table 127. CPLD combinatorial timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			20	+ 2	+ 10	– 2	ns
t_{EA}	CPLD input to CPLD output enable			21		+ 10	– 2	ns
t_{ER}	CPLD input to CPLD output disable			21		+ 10	– 2	ns
t_{ARP}	CPLD register clear or preset delay			21		+ 10	– 2	ns
t_{ARPW}	CPLD register clear or preset pulse width		10			+ 10		ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Table 128. CPLD combinatorial timing (3 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			40	+ 4	+ 20	– 6	ns
t_{EA}	CPLD input to CPLD output enable			43		+ 20	– 6	ns
t_{ER}	CPLD input to CPLD output disable			43		+ 20	– 6	ns
t_{ARP}	CPLD register clear or preset delay			40		+ 20	– 6	ns
t_{ARPW}	CPLD register clear or preset pulse width		25			+ 20		ns
t_{ARD}	CPLD array delay	Any macrocell		25	+ 4			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Figure 80. Input macrocell timing (product term clock)

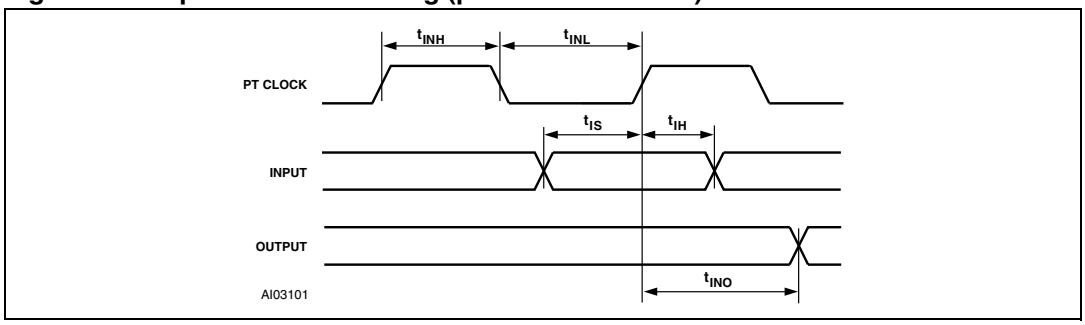


Table 133. Input macrocell timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo Off	Unit
t_{IS}	Input setup time	(Note 1)	0				ns
t_{IH}	Input hold time	(Note 1)	15			+ 10	ns
t_{INH}	NIB input high time	(Note 1)	9				ns
t_{INL}	NIB input low time	(Note 1)	9				ns
t_{INO}	NIB input to combinatorial delay	(Note 1)		34	+ 2	+ 10	ns

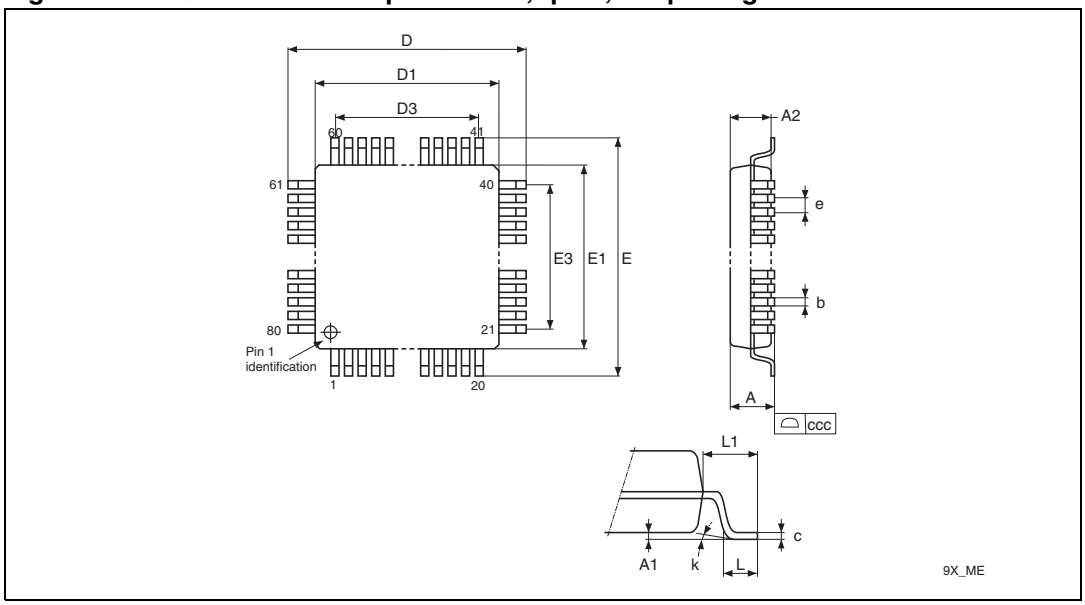
1. Inputs from Port A, B, and C relative to register/ latch clock from the PLD. ALE/AS latch timings refer to t_{AVLX} and t_{LXAX}.

Table 134. Input macrocell timing (3 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo Off	Unit
t_{IS}	Input setup time	(Note 1)	0				ns
t_{IH}	Input hold time	(Note 1)	25			+ 20	ns
t_{INH}	NIB input high time	(Note 1)	12				ns
t_{INL}	NIB input low time	(Note 1)	12				ns
t_{INO}	NIB input to combinatorial delay	(Note 1)		46	+ 4	+ 20	ns

1. Inputs from Port A, B, and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX}.

Figure 92. LQFP80 – 80-lead plastic thin, quad, flat package outline



1. Drawing is not to scale.

Table 147. LQFP80 – 80-lead plastic thin, quad, flat package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.090	0.200		0.0035	0.0079
D	14.000			0.5512		
D1	12.000			0.4724		
D3	9.500			0.3740		
E	14.000			0.5512		
E1	12.000			0.4724		
E3	9.500			0.3740		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k		0°	7°		0°	7°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.